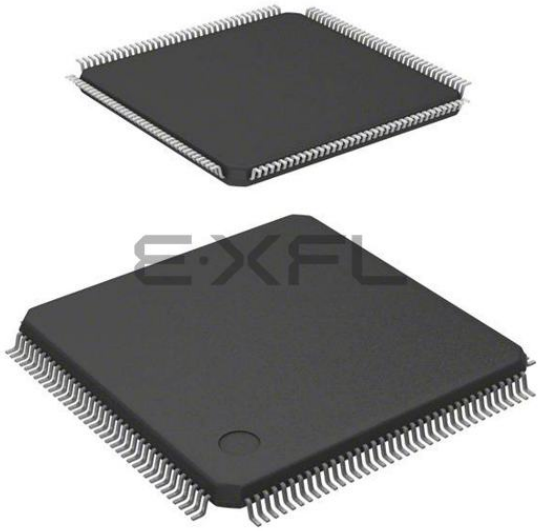

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	115
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 18x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302zdt6

List of figures

Table 2. STM32F302xD/E family device features and peripheral counts

Peripheral		STM32F302Rx		STM32F302Vx		STM32F302Zx	
Flash (Kbytes)		384	512	384	512	384	512
SRAM (Kbytes) on data bus		64					
FMC (flexible memory controller)		NO		YES			
Timers	Advanced control	1 (16-bit)					
	General purpose	5 (16-bit) 1 (32-bit)					
	Basic	1 (16-bit)					
	PWM channels (all) (1)	26					
	PWM channels (except complementary)	20					
Communication interfaces	SPI (I^2S)(2)	4(2)					
	I^2C	3					
	USART	3					
	UART	2					
	CAN	1					
	USB	1					
GPIOs	Normal I/Os (TC, TTa)	26		37 in WLCSP100,44 in LQFP100 and UFBGA100		45	
	5-volt tolerant I/Os (FT, FTf)	25		42 in LQFP100 40 in WLCSP100 and UFBGA100		70	
DMA channels		12					
Capacitive sensing channels		18		24			
12-bit ADCs		2 16 channels		2 17 channels		2 18 channels	
12-bit DAC channels		1					
Analog comparator		4					
Operational amplifiers		2					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP64		LQFP100 ,WLCSP100 UFBGA100		LQFP144	

1. This total number considers also the PWMs generated on the complementary output channels.
2. The SPI interfaces works in an exclusive way in either the SPI mode or the I^2S audio mode.

Table 5. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Note: TIM1/2/3/4/15/16/17 can have PLL as clock source, and therefore can be clocked at 144 MHz.

3.18.1 Advanced timers (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timer (described in *Section 3.18.2*) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.18.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xD/E (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, I^2C FM+ option
		TTa	3.3 V tolerant I/O
		TC	Standard 3.3V I/O
		B	Dedicated to BOOT0 pin
		RST	Bi-directional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F302xD/E pin definitions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
-	1	D6	1	PE2	I/O	FT	(1)	TRACECK, EVENTOUT, TIM3_CH1, TSC_G7_IO1, SPI4_SCK, FMC_A23	-
-	2	D7	2	PE3	I/O	FT	(1)	TRACED0, EVENTOUT, TIM3_CH2, TSC_G7_IO2, SPI4_NSS, FMC_A19	-
-	3	C8	3	PE4	I/O	FT	(1)	TRACED1, EVENTOUT, TIM3_CH3, TSC_G7_IO3, SPI4_NSS, FMC_A20	-
-	4	B9	4	PE5	I/O	FT	(1)	TRACED2, EVENTOUT, TIM3_CH4, TSC_G7_IO4, SPI4_MISO, FMC_A21	-
-	5	E7	5	PE6	I/O	FT	(1)	TRACED3, EVENTOUT, SPI4_MOSI, FMC_A22	WKUP3, RTC_TAMP3
1	6	D8	6	VBAT	S	-	-	-	-

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
21	30	H7	41	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TSC_G2_IO2, SPI1_SCK, EVENTOUT	ADC2_IN2(3), COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM, OPAMP1_VINP, OPAMP2_VINM,
22	31	H6	42	PA6	I/O	TTa	(5)	TIM16_CH1, TIM3_CH1, TSC_G2_IO3, SPI1_MISO, TIM1_BKIN, COMP1_OUT, EVENTOUT	ADC2_IN3(3), OPAMP2_VOUT
23	32	K7	43	PA7	I/O	TTa	-	TIM17_CH1, TIM3_CH2, TSC_G2_IO4, SPI1_MOSI, TIM1_CH1N, EVENTOUT	ADC2_IN4(3), COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
24	33	G6	44	PC4	I/O	TTa	-	EVENTOUT, TIM1_ETR, USART1_TX	ADC2_IN5(3)
25	34	F6	45	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM
26	35	J6	46	PB0	I/O	TTa	-	TIM3_CH3, TSC_G3_IO2, TIM1_CH2N, EVENTOUT	COMP4_INP, OPAMP2_VINP,
27	36	K6	47	PB1	I/O	TTa	(5)	TIM3_CH4, TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	-
28	37	K5	48	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	ADC2_IN12, COMP4_INM
-	-	-	49	PF11	I/O	FT	(1)	EVENTOUT	-
-	-	-	50	PF12	I/O	FT	(1)	EVENTOUT, FMC_A6	-
-	-	-	51	VSS	S	-	-	-	-
-	-	-	52	VDD	S	-	(1)	-	-
-	-	-	53	PF13	I/O	FT	(1)	EVENTOUT, FMC_A7	-
-	-	-	54	PF14	I/O	FT	(1)	EVENTOUT, FMC_A8	-
-	-	-	55	PF15	I/O	FT	(1)	EVENTOUT, FMC_A9	-
-	-	-	56	PG0	I/O	FT	(1)	EVENTOUT, FMC_A10	-
-	-	-	57	PG1	I/O	FT	(1)	EVENTOUT, FMC_A11	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port D	PD5	-	EVENT OUT	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	-
	PD6	-	EVENT OUT	TIM2_CH4	-	-	-	-	USART2_RX	-	-	-	-	FMC_NWAIT	-	-	-
	PD7	-	EVENT OUT	TIM2_CH3	-	-	-	-	USART2_CK	-	-	-	-	FMC_NE1/FMC_NCE2	-	-	-
	PD8	-	EVENT OUT	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	-
	PD9	-	EVENT OUT	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	-
	PD10	-	EVENT OUT	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	-	-
	PD11	-	EVENT OUT	-	-	-	-	-	USART3_CTS	-	-	-	-	FMC_A16	-	-	-
	PD12	-	EVENT OUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS	-	-	-	-	FMC_A17	-	-	-
	PD13	-	EVENT OUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-	-	-	-	-	FMC_A18	-	-	-
	PD14	-	EVENT OUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-	-	-	-	-	FMC_D0	-	-	-
	PD15	-	EVENT OUT	TIM4_CH4	TSC_G8_IO4	-	-	SPI2_NSS	-	-	-	-	-	FMC_D1	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE0	-	EVENT OUT	TIM4_ETR	-	TIM16_CH1	-	-	USART1_TX	-	-	-	-	FMC_NBL0	-	-	-
	PE1	-	EVENT OUT	-	-	TIM17_CH1	-	-	USART1_RX	-	-	-	-	FMC_NBL1	-	-	-
	PE2	TRACECK	EVENT OUT	TIM3_CH1	TSC_G7_IO1	-	SPI4_SCK	-	-	-	-	-	-	FMC_A23	-	-	-
	PE3	TRACED0	EVENT OUT	TIM3_CH2	TSC_G7_IO2	-	SPI4_NSS	-	-	-	-	-	-	FMC_A19	-	-	-
	PE4	TRACED1	EVENT OUT	TIM3_CH3	TSC_G7_IO3	-	SPI4_NSS	-	-	-	-	-	-	FMC_A20	-	-	-
	PE5	TRACED2	EVENT OUT	TIM3_CH4	TSC_G7_IO4	-	SPI4_MISO	-	-	-	-	-	-	FMC_A21	-	-	-
	PE6	TRACED3	EVENT OUT	-	-	-	SPI4_MOSI	-	-	-	-	-	-	FMC_A22	-	-	-
	PE7	-	EVENT OUT	TIM1_ETR	-	-	-	-	-	-	-	-	-	FMC_D4	-	-	-
	PE8	-	EVENT OUT	TIM1_CH1N	-	-	-	-	-	-	-	-	-	FMC_D5	-	-	-
	PE9	-	EVENT OUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	FMC_D6	-	-	-
	PE10	-	EVENT OUT	TIM1_CH2N	-	-	-	-	-	-	-	-	-	FMC_D7	-	-	-
	PE11	-	EVENT OUT	TIM1_CH2	-	-	SPI4_NSS	-	-	-	-	-	-	FMC_D8	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

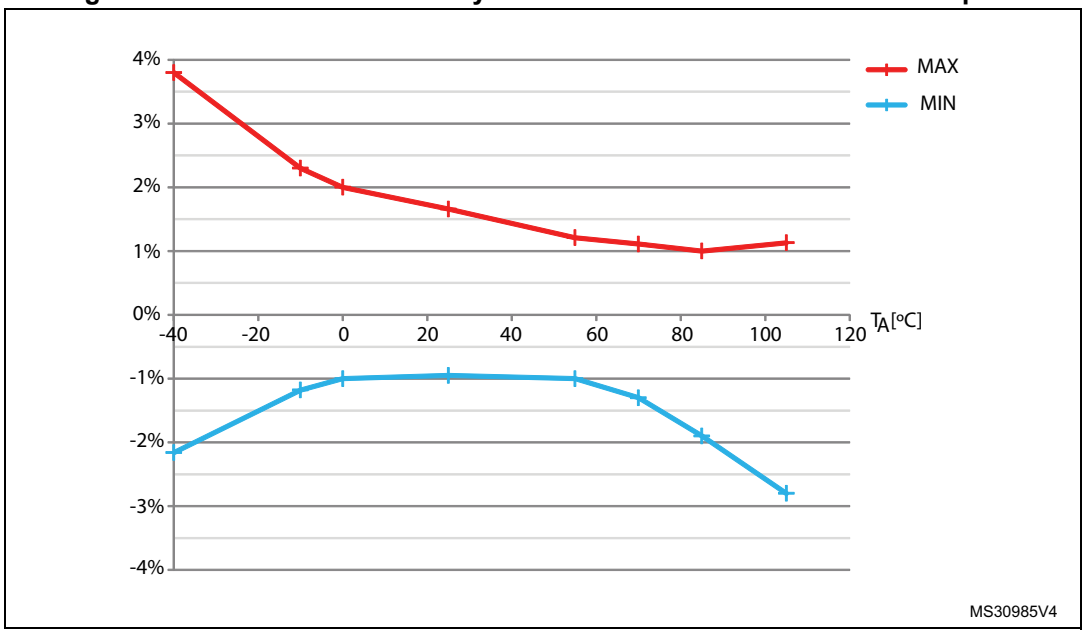
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port F	PF8	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NIOWR	-	-	-
	PF9	-	EVENT OUT	-	TIM15_CH1	-	SPI2_SCK	-	-	-	-	-	-	FMC_CD	-	-	-
	PF10	-	EVENT OUT	-	TIM15_CH2	-	SPI2_SCK	-	-	-	-	-	-	FMC_INTR	-	-	-
	PF11	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PF12	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	-
	PF13	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	-
	PF14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	-
	PF15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	-
Port G	PG0	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	-
	PG1	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	-
	PG2	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	-
	PG3	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	-
	PG4	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A14	-	-	-

Table 31. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	43.0	7.4	mA
			64 MHz	38.3	6.8	
			48 MHz	29.0	5.29	
			32 MHz	19.7	3.91	
			24 MHz	15.2	3.19	
			16 MHz	10.8	2.46	
			8 MHz	5.85	1.55	
			4 MHz	3.80	1.45	
			2 MHz	2.67	1.32	
			1 MHz	2.12	1.22	
			500 kHz	1.83	1.19	
			125 kHz	1.60	0.83	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.7		µA
			64 MHz	210.5		
			48 MHz	155.6		
			32 MHz	105.5		
			24 MHz	81.9		
			16 MHz	58.6		
			8 MHz	1.16		
			4 MHz	1.16		
			2 MHz	1.16		
			1 MHz	1.16		
			500 kHz	1.16		
			125 kHz	1.16		

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

Table 51. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	4THCLK-1	4THCLK+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK	THCLK+0.5	
$t_{w(NWE)}$	FMC_NWE low time	2THCLK-0.5	2THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	1	2.5	
$t_{w(NADV)}$	FMC_NADV low time	THCLK-2	THCLK+2	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	THCLK-2	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	THCLK +3.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK +0.5	-	

1. Based on characterization, not tested in production.

Table 52. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9THCLK	9THCLK+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	6THCLK	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK+6	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	5THCLK-5	-	

1. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 24 and *Figure 27* present the synchronous waveforms and *Table 53* to *Table 56* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 2 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the THCLK is the HCLK clock period (with maximum FMC_CLK = 36 MHz).

Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings

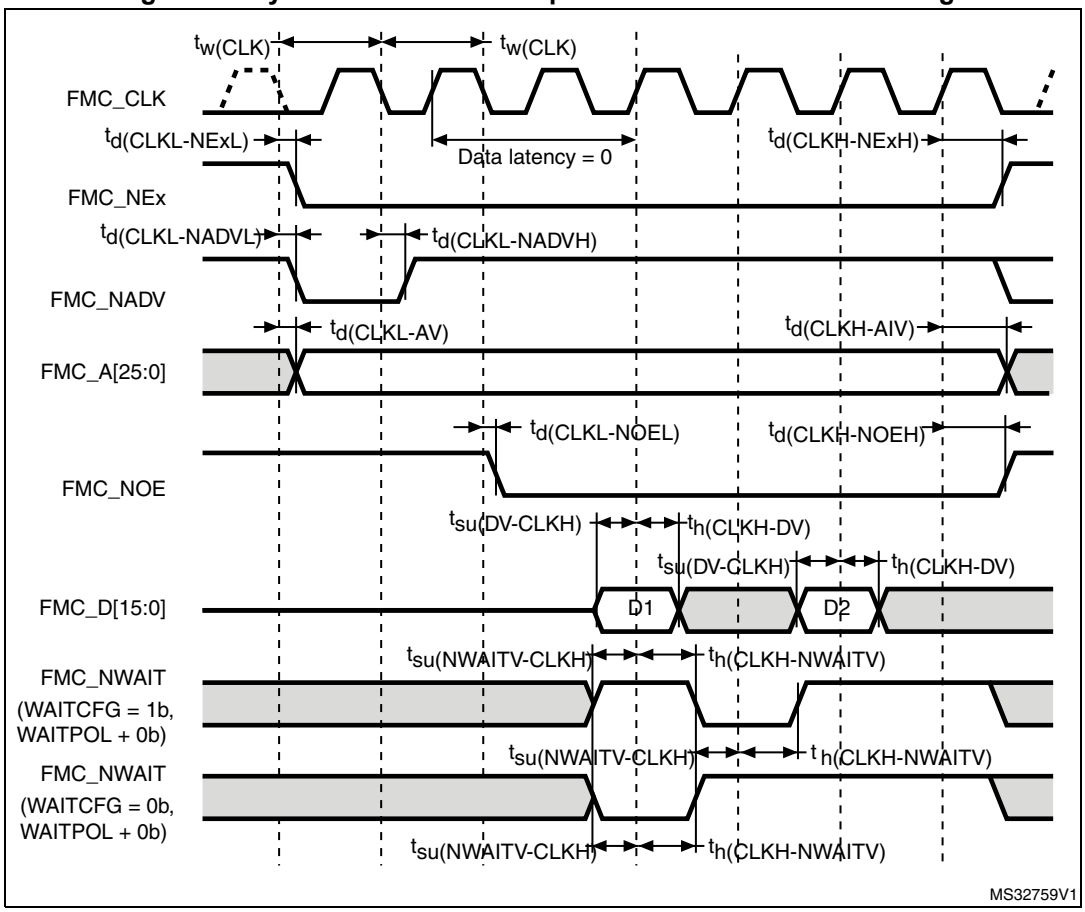


Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	7	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	THCLK	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	

Table 56. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	6	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	6.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	0	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+2	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	7.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	7	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

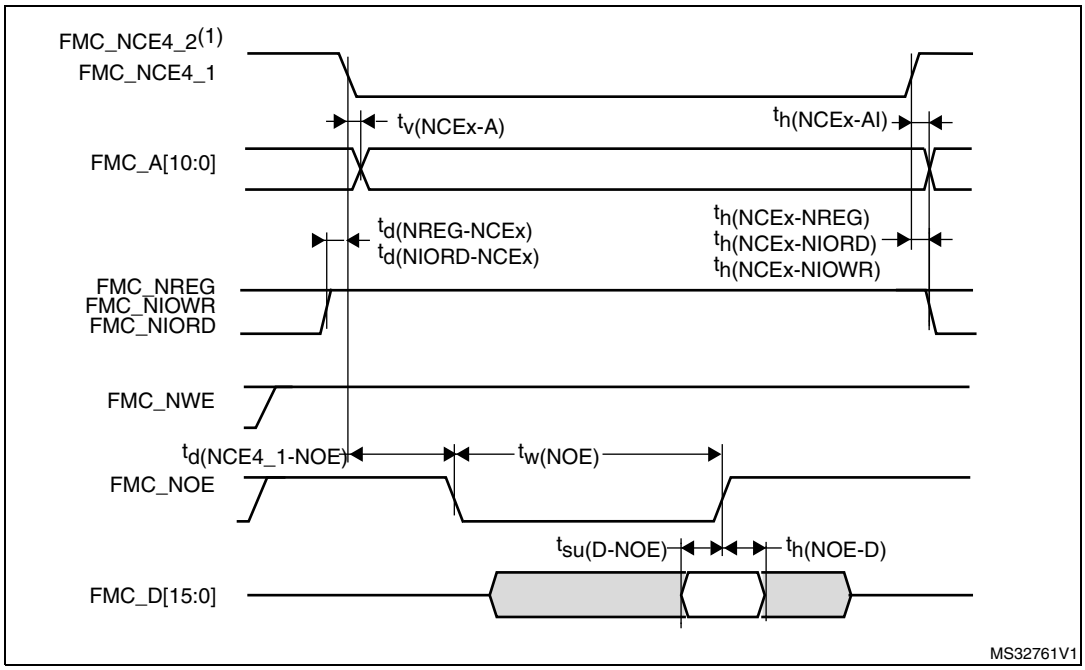
PC Card/CompactFlash controller waveforms and timings

Figure 28 to *Figure 33* present the PC Card/Compact Flash controller waveforms, and *Table 57* to *Table 58* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FMC_SetupTime = 0x04;
- COM.FMC_WaitSetupTime = 0x07;
- COM.FMC_HoldSetupTime = 0x04;
- COM.FMC_HiZSetupTime = 0x05;
- ATT.FMC_SetupTime = 0x04;
- ATT.FMC_WaitSetupTime = 0x07;
- ATT.FMC_HoldSetupTime = 0x04;
- ATT.FMC_HiZSetupTime = 0x05;
- IO.FMC_SetupTime = 0x04;
- IO.FMC_WaitSetupTime = 0x07;
- IO.FMC_HoldSetupTime = 0x04;
- IO.FMC_HiZSetupTime = 0x05;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the THCLK is the HCLK clock period.

Figure 28. PC Card/CompactFlash controller waveforms for common memory read access



1. FMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 29. PC Card/CompactFlash controller waveforms for common memory write access

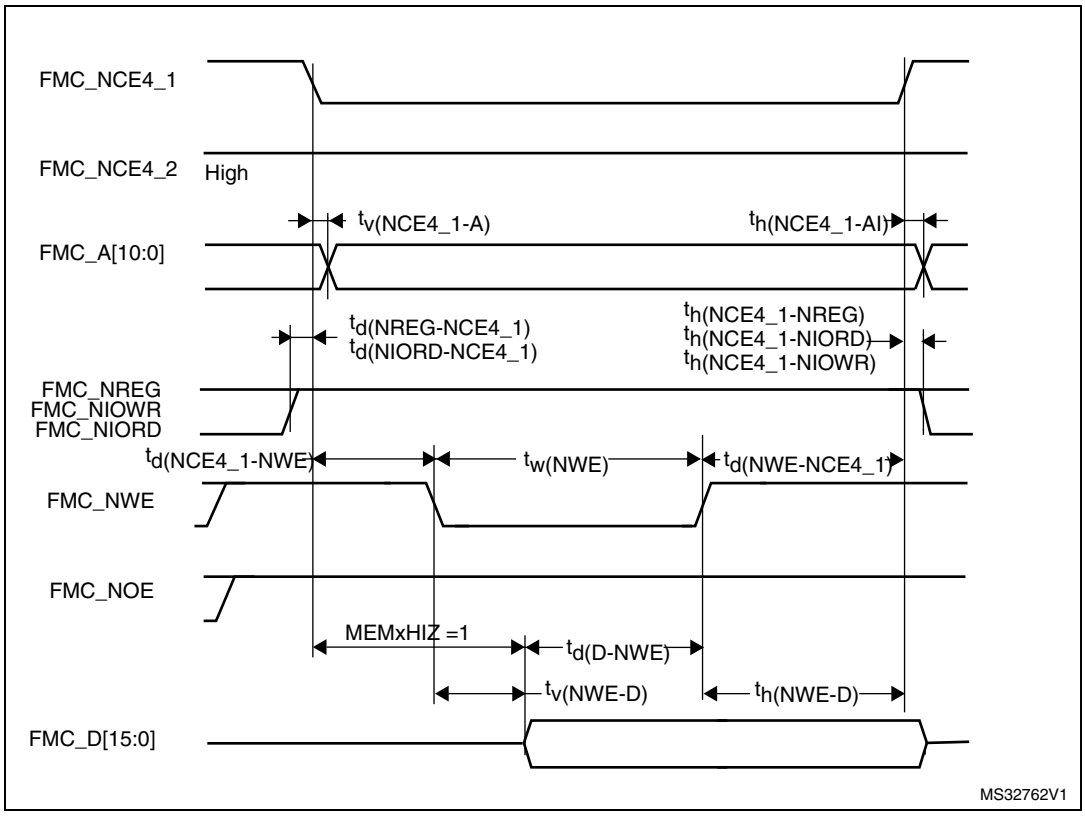


Table 73. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 74* for SPI or in *Table 75* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 19*.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 74. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V<V_{DD}<3.6 V, SPI1/4	-	-	24	MHz
		Master mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/4			24	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode transmitter/full duplex 2 V<V_{DD}<3.6 V, SPI1/2/3/4			16.5(2)	
		Slave mode transmitter/full duplex 2.7 V<V_{DD}<3.6 V, SPI1/4			22.5(2))	-
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	30	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	7	

Table 74. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V<V_{DD}<3.6 V	-	15	22	
		Slave mode 2 V<V_{DD}<3.6 V	-	15	30	
$t_{v(MO)}$		Master mode	-	2	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode	9	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while $Duty_{(SCK)}$ = 50%.

Figure 42. SPI timing diagram - slave mode and CPHA = 0

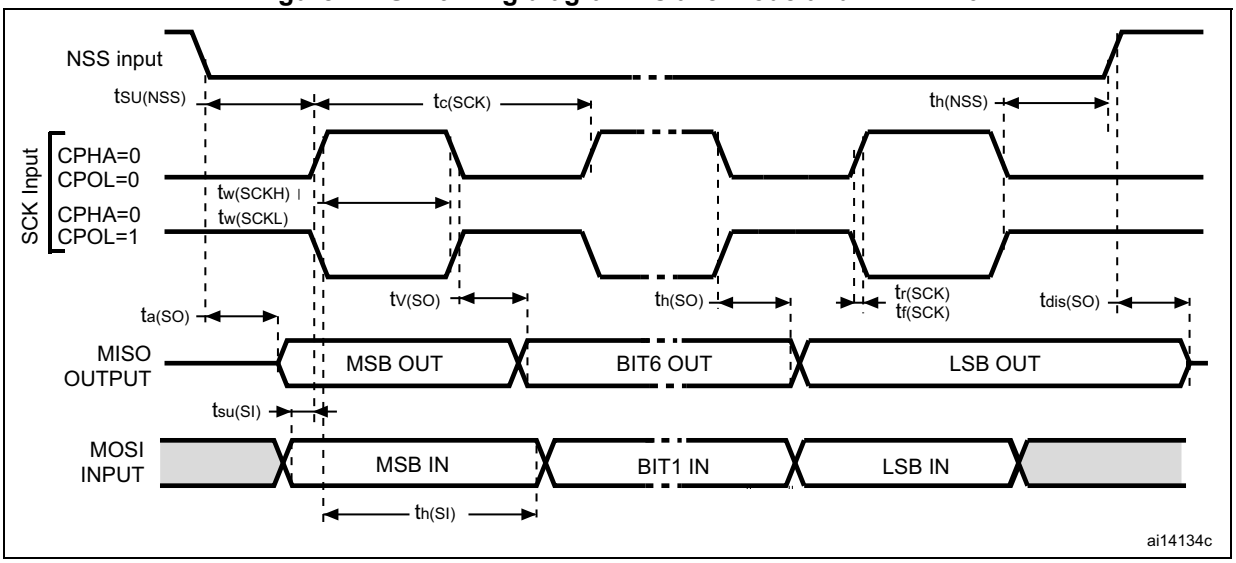
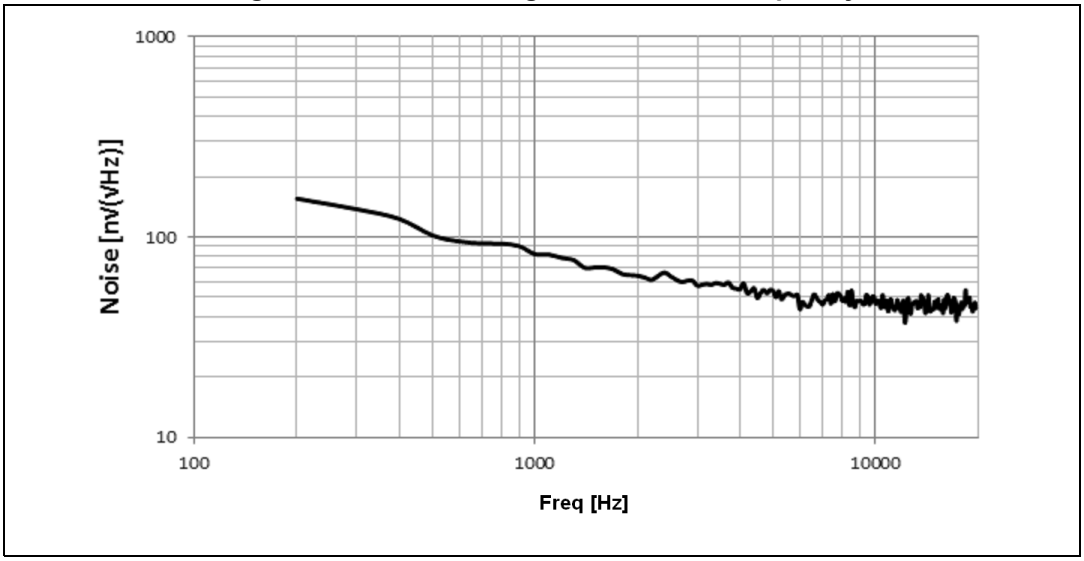


Table 84. ADC accuracy, 64-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
EL	Integral linearity error	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, 2.0 V ≤ V_{DDA} ≤ 3.6 V 64-pin package	Single ended	Fast channel 5.1 Ms	-	±3	LSB
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB (5)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Figure 53. OPAMP voltage noise versus frequency



6.3.23 Temperature sensor characteristics

Table 89. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 90. Temperature sensor calibration values

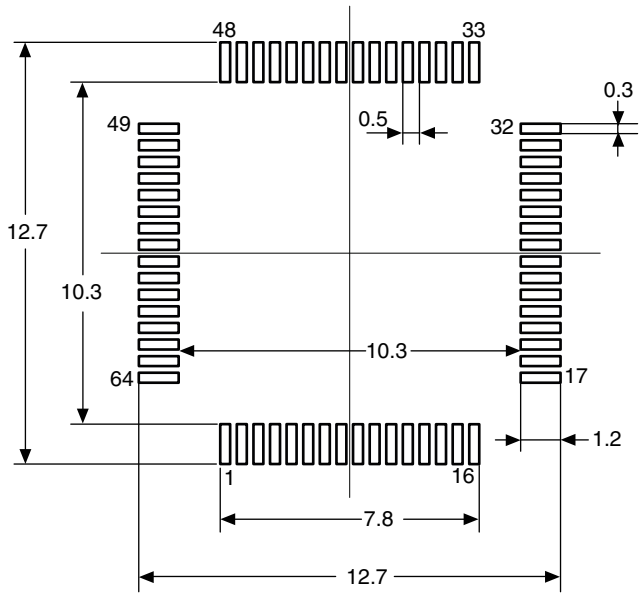
Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 98. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. Recommended footprint for the LQFP64 package



1. Dimensions are expressed in millimeters.