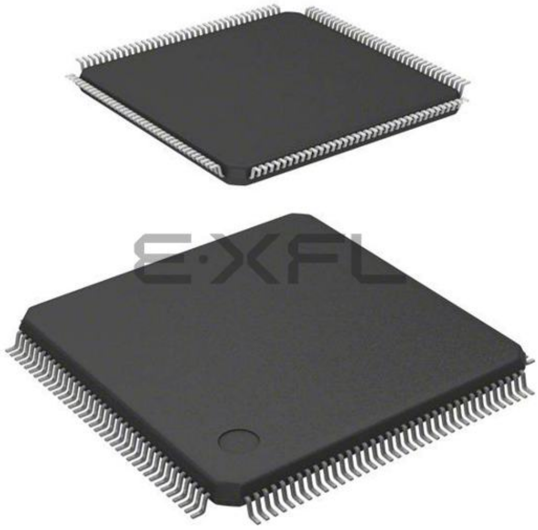

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	115
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 18x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302zet6

List of tables

2 Description

The STM32F302xD/E family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (512-Kbyte Flash memory, 64-Kbyte SRAM), a flexible memory controller (FSMC) for static memories (SRAM, PSRAM, NOR and NAND), and an extensive range of enhanced I/Os and peripherals connected to an AHB and two APB buses.

The devices offer two fast 12-bit ADCs (5 Msps), four comparators, two operational amplifiers, one DAC channel, a low-power RTC, up to two general-purpose 16-bit timers, one general-purpose 32-bit timer, and one timer dedicated to motor control. They also feature standard and advanced communication interfaces: up to three I^2Cs, up to four SPIs (two SPIs are with multiplexed full-duplex I^2Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I^2S peripherals can be clocked via an external PLL.

The STM32F302xD/E family operates in the -40 to +85°C and -40 to +105°C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302xD/E family offers devices in different packages ranging from 64 to 144 pins.

Depending on the device chosen, different sets of peripherals are included.

3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA is used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.12 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller,
- The NAND/PC Card memory controller.

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM),
  - NOR Flash memory/OneNAND Flash memory,
  - PSRAM (four memory banks),
  - NAND Flash memory with ECC hardware to check up to 8 Kbyte of data,
  - 16-bit PC Card compatible devices.
- 8-,16-bit data bus width,
- Independent Chip Select control for each memory bank,
- Independent configuration for each memory bank,
- Write FIFO,
- LCD parallel interface.

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost

Table 10. Capacitive sensing GPIOs available on STM32F302xD/E devices (continued)

Group	Capacitive sensing signal name	Pin name	-	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC5	-	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0	-		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1	-		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2	-		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	-	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10	-		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13	-		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14	-		TSC_G8_IO4	PD15

Table 11. Number of capacitive sensing channels available on STM32F302xD/E devices

Analog I/O group	Number of capacitive sensing channels	
	STM32F302VE/ZE	STM32F302RE
G1	3	3
G2	3	3
G3	3	3
G4	3	3
G5	3	3
G6	3	3
G7	3	0
G8	3	0
Number of capacitive sensing channels	24	18

3.28 Development support

3.28.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.28.2 Embedded Trace Macrocell

The ARM embedded trace macrocell (ETM™) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F302xD/E through a small number of ETM™ pins to an external hardware trace

Figure 8. STM32F302xD/E UFBGA100 ballout

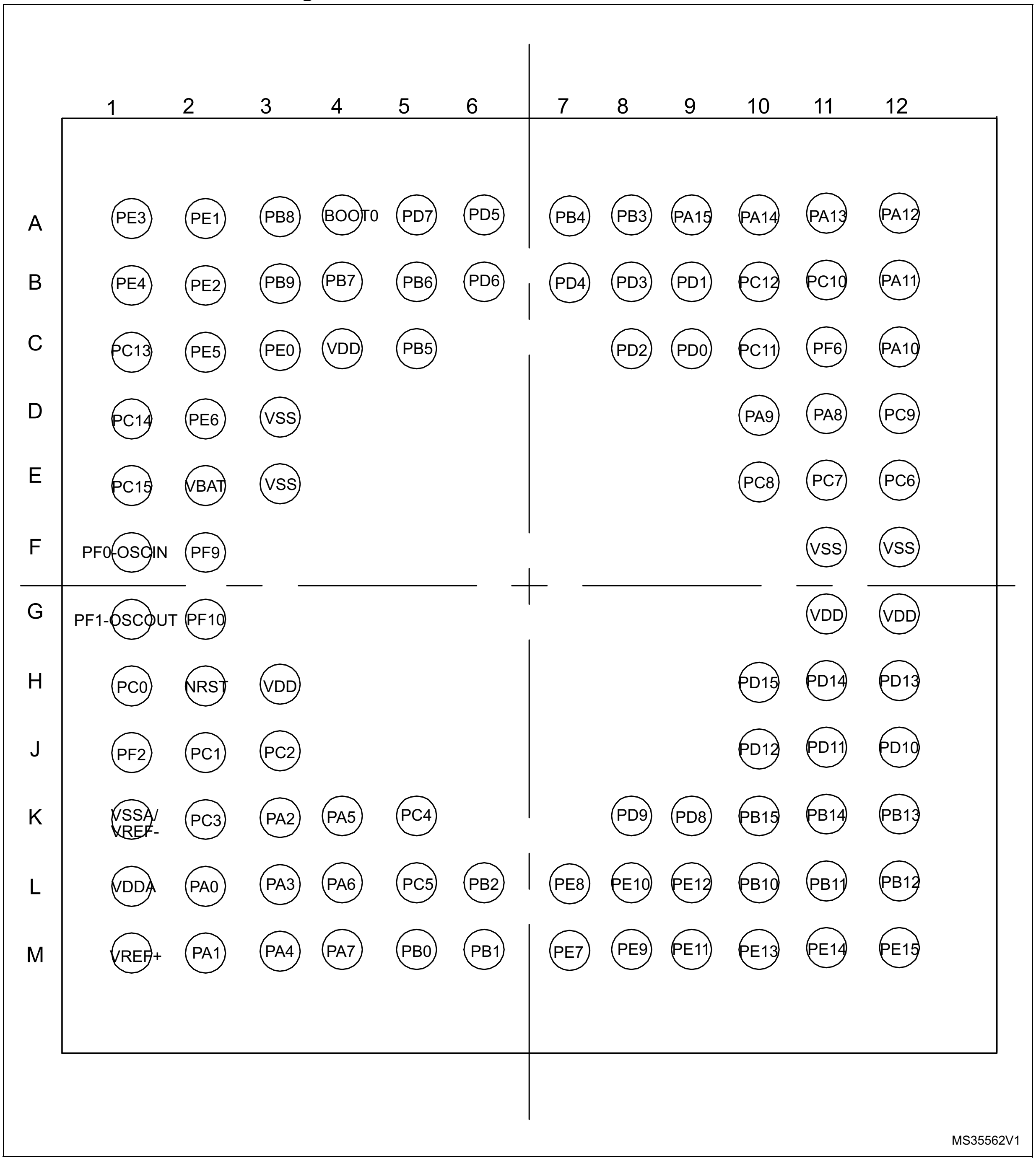


Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
34	52	J3	74	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	-
35	53	J2	75	PB14	I/O	TTa	-	TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS, EVENTOUT	OPAMP2_VINP
36	54	H4	76	PB15	I/O	TTa	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	COMP6_INM
-	55	-	77	PD8	I/O	TTa	(1)	EVENTOUT, USART3_TX, FMC_D13	-
-	56	G4	78	PD9	I/O	TTa	(1)	EVENTOUT, USART3_RX, FMC_D14	-
-	57	H3	79	PD10	I/O	TTa	(1)	EVENTOUT, USART3_CK, FMC_D15	COMP6_INM
-	58	H2	80	PD11	I/O	TTa	(1)	EVENTOUT, USART3_CTS, FMC_A16	-
-	59	H1	81	PD12	I/O	TTa	(1)	EVENTOUT, TIM4_CH1, TSC_G8_IO1, USART3_RTS, FMC_A17	-
-	60	G3	82	PD13	I/O	TTa	(1)	EVENTOUT, TIM4_CH2, TSC_G8_IO2, FMC_A18	-
-	-	-	83	VSS	S	-	(1)	-	-
-	-	-	84	VDD	S	-	(1)	-	-
-	61	G2	85	PD14	I/O	TTa	(1)	EVENTOUT, TIM4_CH3, TSC_G8_IO3, FMC_D0	OPAMP2_VINP
-	62	G1	86	PD15	I/O	TTa	(1)	EVENTOUT, TIM4_CH4, TSC_G8_IO4, SPI2_NSS, FMC_D1	-
-	-	-	87	PG2	I/O	FT	(1)	EVENTOUT, FMC_A12	-
-	-	-	88	PG3	I/O	FT	(1)	EVENTOUT, FMC_A13	-
-	-	-	89	PG4	I/O	FT	(1)	EVENTOUT, FMC_A14	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port B	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	SPI2_MISO/I2S2ext_SD	TIM1_CH2N	USART3_RTS	-	-	-	-	-	-	-	EVENT OUT
Port B	PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT
Port C	PC0	-	EVENT OUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
Port C	PC1	-	EVENT OUT	TIM1_CH2	-	-	-	-	-	-	-	-	-	-	-	-	-
Port C	PC2	-	EVENT OUT	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
Port C	PC3	-	EVENT OUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
Port C	PC4	-	EVENT OUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
Port C	PC5	-	EVENT OUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
Port C	PC6	-	EVENT OUT	TIM3_CH1	-	-	-	I2S2_MCK	COMP6_OUT	-	-	-	-	-	-	-	-
Port C	PC7	-	EVENT OUT	TIM3_CH2	-	-	-	I2S3_MCK	-	-	-	-	-	-	-	-	-
Port C	PC8	-	EVENT OUT	TIM3_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
Port C	PC9	-	EVENT OUT	TIM3_CH4	I2C3_SDA	-	I2SCKIN	-	-	-	-	-	-	-	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port F	PF8	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NIOWR	-	-	-
	PF9	-	EVENT OUT	-	TIM15_CH1	-	SPI2_SCK	-	-	-	-	-	-	FMC_CD	-	-	-
	PF10	-	EVENT OUT	-	TIM15_CH2	-	SPI2_SCK	-	-	-	-	-	-	FMC_INTR	-	-	-
	PF11	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PF12	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	-
	PF13	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	-
	PF14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	-
	PF15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	-
Port G	PG0	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	-
	PG1	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	-
	PG2	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	-
	PG3	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	-
	PG4	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A14	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port G	PG5	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A15	-	-	-
	PG6	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT2	-	-	-
	PG7	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT3	-	-	-
	PG8	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PG9	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE2/FMC_NCE3	-	-	-
	PG10	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_1/FMC_NE3	-	-	-
	PG11	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_2	-	-	-
	PG12	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE4	-	-	-
	PG13	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A24	-	-	-
	PG14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A25	-	-	-
	PG15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 20* are derived from tests performed under the ambient temperature condition summarized in *Table 19*.

Table 20. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 21. Embedded reset and power control block characteristics

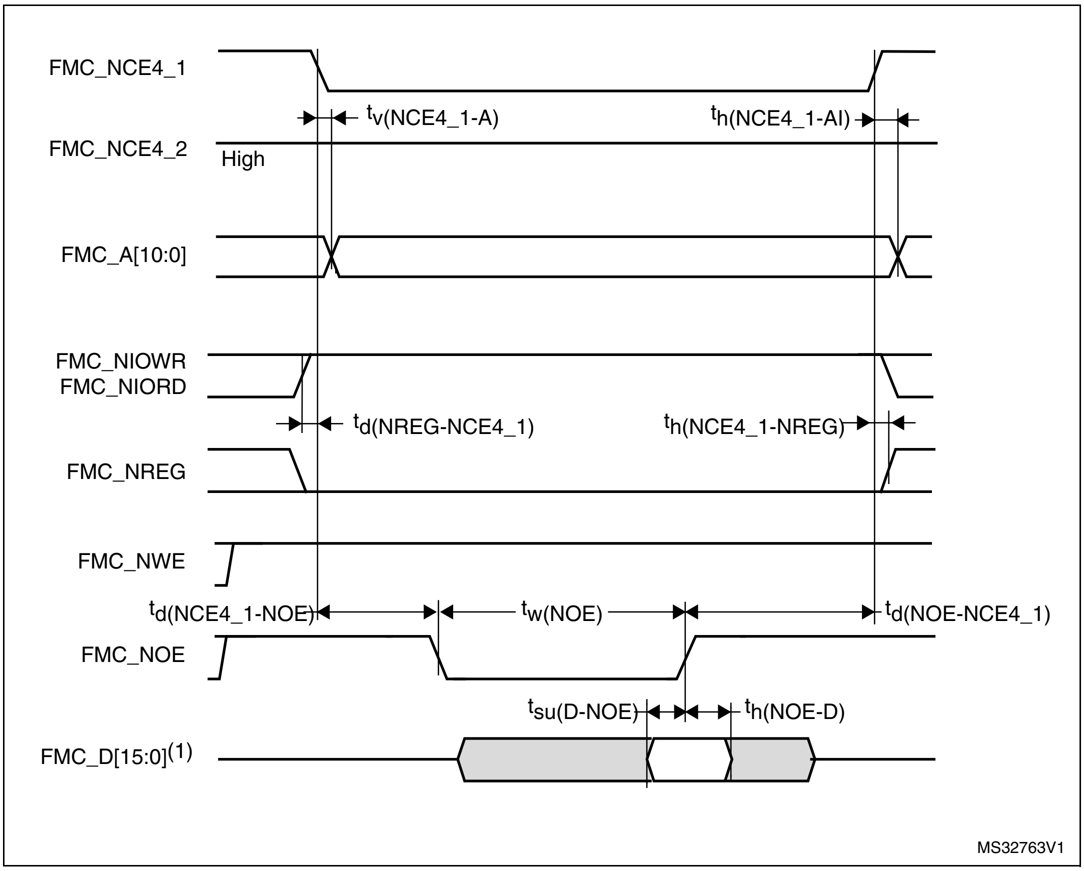
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

Table 22. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	

Figure 30. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Pre qualification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 62. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package compliant with IEC 61967-2	0.1 to 30 MHz	7	dBµV
			30 to 130 MHz	15	
			130 MHz to 1GHz	31	
			SAE EMI Level	4	-

6.3.13 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 63. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Data based on characterization results, not tested in production.

Table 79. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{REF}	Current on VREF+ pin (see *Figure 49*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}(1)	Power-up time	-	0	0	1	µs
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz		1.56		µs
		-		112		$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$

Table 83. ADC accuracy - limited test conditions, 64-pin packages(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 84. ADC accuracy, 64-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2.0 V ≤ V_{DDA} ≤ 3.6 V 64-pin package	Single ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	

Table 85. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.15: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 50. ADC accuracy characteristics

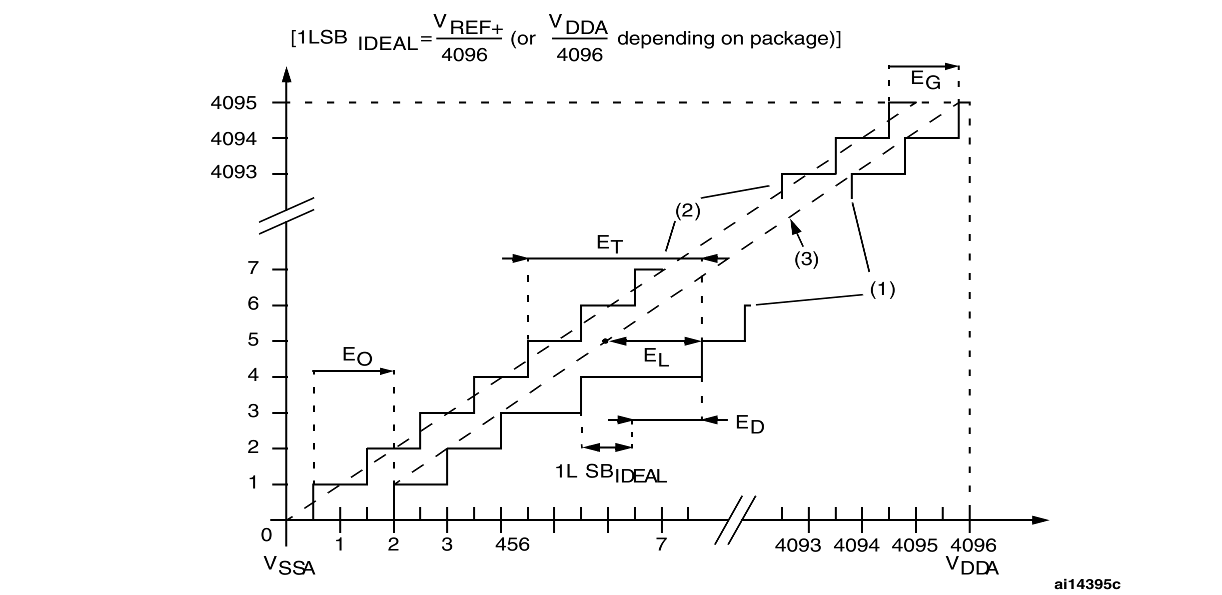


Table 87. Comparator characteristics[1] (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
I_{DDA}	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.

Table 93. UFBGA100 package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 58. Recommended footprint for the UFBGA100 package

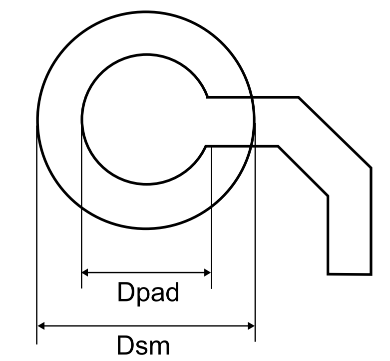


Table 94. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

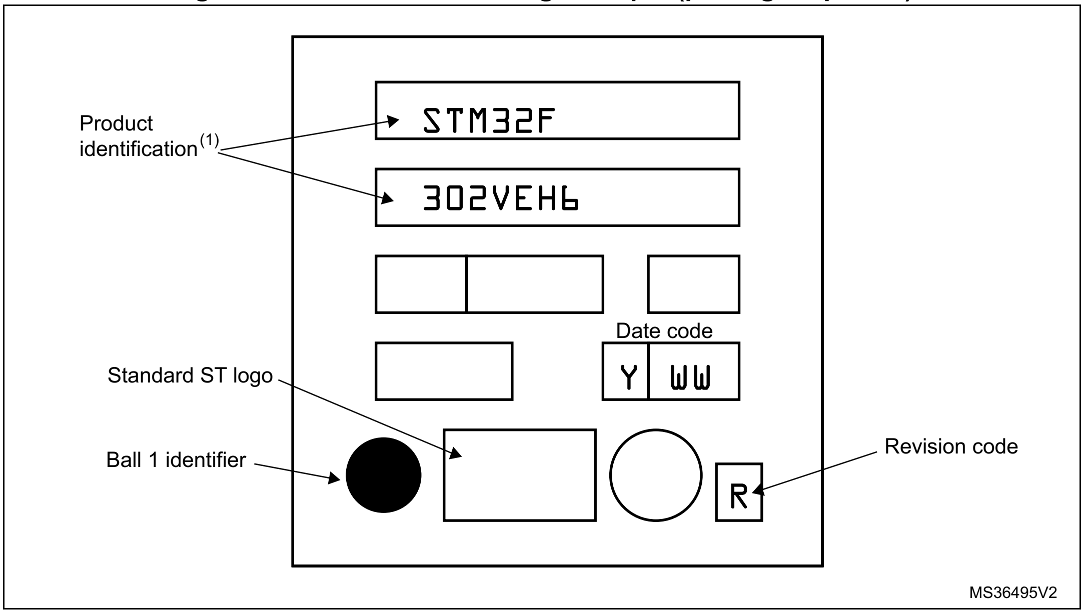
Note: 4 to 6 mils solder paste screen printing process.

Device marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. UFBGA100 marking example (package top view)

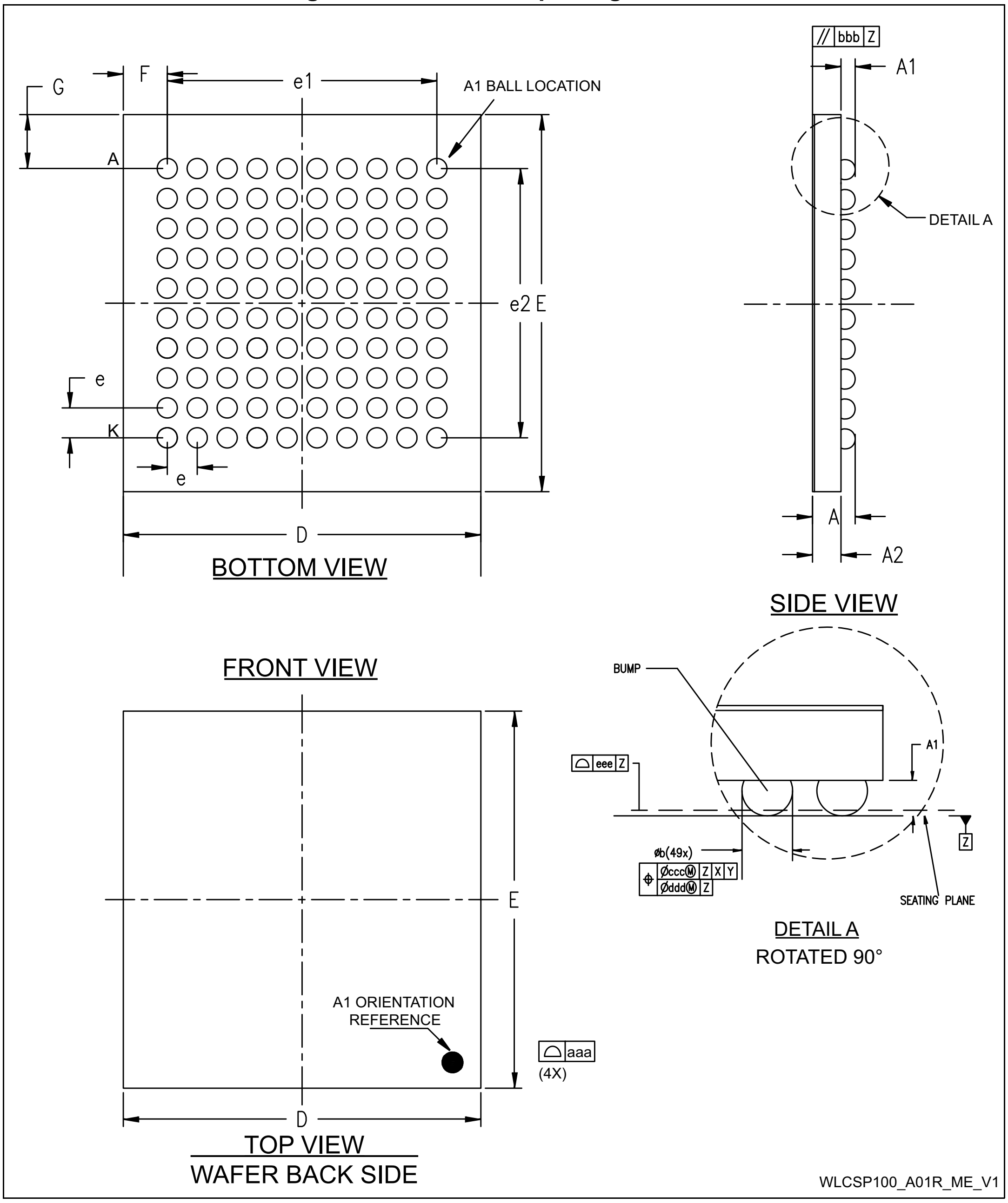


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 WLCSP100 package information

WLCSP100 is a 100-ball, 4.775 x 5.041 mm, 0.4 mm pitch wafer level chip scale package.

Figure 63.WLCSP100 package outline



1. Drawing is not to scale.