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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Security
Core Processor	-
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	ISO14443-3 Type A, NFC Forum Type 2
Number of I/O	-
Voltage - Supply	-
Operating Temperature	-25°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	Die
Supplier Device Package	Wafer
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sle66r01pnnbx1sa2

List of Tables

Features

Intelligent 1216 bit EEPROM with Contactless Interface compliant to ISO/IEC 14443-3 Type A and support of NFC Forum™ Type 2 Tag Operation

Contactless Interface

- Physical Interface and Anticollision compliant to ISO/IEC 14443-3 Type A
  - Operation frequency 13.56 MHz
  - Data rate 106 kbit/s in both direction
  - Contactless transmission of data and supply energy
  - Anticollision logic: several cards may be operated in the field simultaneously
- Unique IDentification number (7-byte double-size UID) according to ISO/IEC 14443-3 Type A
- Read and Write Distance up to 10 cm and more (influenced by external circuitry i.e. reader and inlay design)

152 byte EEPROM

- Organized in 38 blocks of 4 bytes each
- 128 bytes freely programmable User Memory
- 24 bytes of Service Area reserved for UID, Configuration, LOCK Bytes, OTP Block and Manufacturer Data
- Read and Write of 128 bytes of User Memory in less than 100 ms
- Programming time per block < 4 ms
- Endurance minimum 10,000 erase/write cycles[1)]
- Data Retention minimum 5 years[1)]

Privacy Features

- 32 bit of One Time Programmable (OTP) memory area
- Locking mechanism for each block
- Block Lock mechanism
- Optional 32 bit Password for Read/Write or Write access
- Optional Password Retry Counter
- Optional 16 bit Value Counter

Data Protection

- Data Integrity supported by 16 bit CRC, parity bit, command length check
- Anti-tearing mechanism for OTP, Password Retry Counter and Value Counter

NFC Forum™ Operation

- Compliant to NFC Forum™ Type 2 Tag Operation
- Support of Static and Dynamic Memory Structure according to NFC Forum™ Type 2 Tag Operation
- SLE 66R01PN: pre-configured NFC memory with empty NDEF message (INITIALIZED state, non-reversible)
- SLE 66R01P: UNINITIALIZED state, may be configured to INITIALIZED state

Electrical Characteristics

- On-Chip capacitance 17 pF $\pm$ 5%
- ESD protection minimum 2 kV
- Ambient Temperature -25℃ … +70℃ (for the chip)

1) Values are temperature dependent

1 Ordering and packaging information

Table 1 Ordering information

Type	Package	Total Memory / User Memory[1)]	Ordering code
SLE 66R01P C	wafer sawn / unsawn	152 / 128 bytes	on request
SLE 66R01P NB	NiAu Bumped (sawn wafer)		SP000911428
SLE 66R01PN C	wafer sawn / unsawn		on request
SLE 66R01PN NB	NiAu Bumped (sawn wafer)		SP000953914

1) Total memory size includes the service area whereas user memory size is freely programmable for user data.

For more ordering information about the form of delivery please contact your local Infineon sales office.

1.1 Pin description

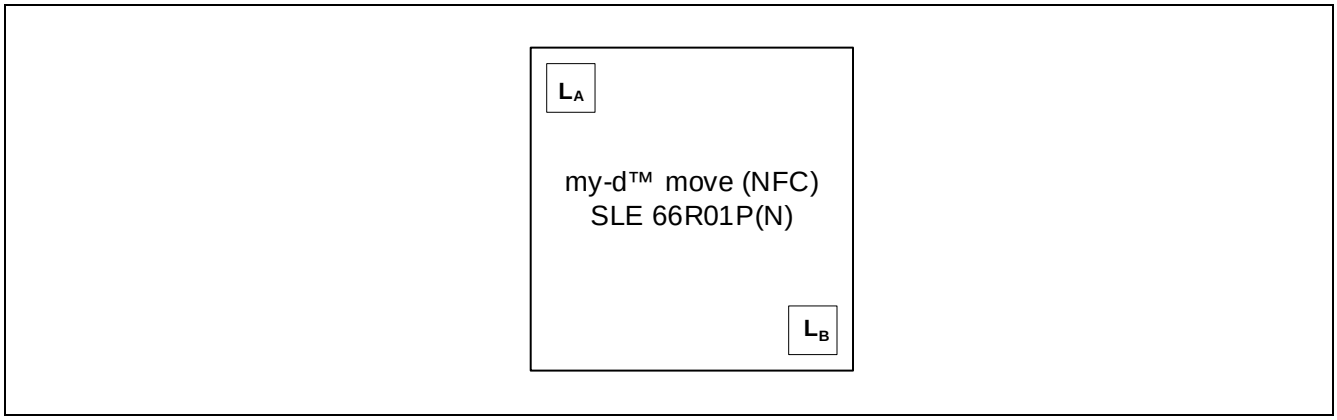

Figure 1 Pin configuration die

Table 2 Pin description and function

Symbol	Function
L_A	Antenna Connection
L_B	Antenna Connection

2.2 Application Segments

my-d™ products are optimized for personal and object identification. Please find in the following table some dedicated examples

Table 3 my-d™ family product overview

Product	Application
my-d™ move - SLE 66R01P	Public Transport, Smart Posters, NFC Device Pairing
my-d™ move NFC - SLE 66R01PN	Public Transport, Smart Posters, NFC Device Pairing, NFC INITIALIZED state
my-d™ move lean - SLE 66R01L	Public Transport, Smart Posters, NFC Device Pairing
my-d™ NFC - SLE 66RxxP	Smart Posters and Maps, NFC Device Pairing, Loyalty Schemes, Consumer Good Information, Healthcare Monitoring
my-d™ proximity 2 - SLE 66RxxS	Access Control, Entertainment, Public Transport, Customer Loyalty Schemes, Micro Payment
my-d™ proximity enhanced - SLE 55RxxE	Access Control, Gaming, Entertainment, Customer Loyalty Schemes
my-d™ light - SRF 55V01P	Libraries, Laundry, Factory Automation, Media Management, Event Ticketing, Leisure Park Access
my-d™ vicinity plain - SRF 55VxxP	Factory Automation, Healthcare, Ticketing, Access Control
my-d™ vicinity plain HC - SRF 55VxxP HC	Ticketing, Brand Protection, Loyalty Schemes, Ski passes
my-d™ vicinity secure - SRF 55VxxS	Ticketing, Brand protection, Loyalty Schemes, Access Control

4.2 Service Area 1 and 2

The Service Area 1 (block address 00_H to 03_H) contains

- 7-byte double-size UID (plus two bytes of UID BCC information)
- Configuration Byte
- LOCK0 and LOCK1 to lock the OTP block and blocks in User Area 1
- 32 bit OTP memory

The Service Area 2 (block address 24_H to 25_H) contains

- LOCK2 - LOCK5 to lock blocks in User Area 2
- Manufacturer Data

4.2.1 Unique Identifier (UID)

The 9 bytes of the UID (7 byte UID + 2 bytes BCC information) are allocated in Block 00_H, Block 01_H and Byte 1 of Block 02_H of the my-d™ move and my-d™ move NFC memory. All bytes are programmed and locked during the manufacturing process. These bytes cannot be changed.

For the content of the UID the following definitions apply:

- SLE 66R01P and SLE 66R01PN support Cascade Level 2 UID according to the ISO/IEC 14443-3 Type A which is a 7 byte unique number

The table below describes the content of the UID including the BCC information.

Table 5 UID Description

Cascade Level 2 - double-size UID										
UID Byte	CT[1)]	uid0[2)]	uid1[3)]	uid2	BCC0[4)]	uid3	uid4	uid5	uid6	BCC1[4)]

1) CT is the Cascade Tag and designates CL2. It has a value of 88_H. Please note that CT is hardwired and not stored in the memory.

2) uid0 is the Manufacturer Code: 05_H according to ISO/IEC 7816-6

3) uid1 is the Chip Family Identifier.
The higher significant nibble identifies a my-d™ move and my-d™ move NFC chip (0011_B).
The lower significant nibble of uid1 is part of the serial number.

4) BCCx are the UID CLn checkbytes calculated as Exclusive-OR over the four previous bytes (as described in ISO/IEC 14443-3 Type A). BCCx is stored in the memory and read-out during the anti-collision.

  - LOCK2 - LOCK5 set to 00_H
  - Manufacturer Data; read-only
- Password set to 00_H 00_H 00_H 00_H
- Password Retry Counter
  - deactivated by the setting of the CONFIG byte

The SLE 66R01P may be configured to INITIALIZED state according to the definition to the NFC Forum™ Type 2 Tag life cycle by writing

- Capability Container bytes (see **Table 9**) to Block 03_H
- empty NDEF message TLV incl. Terminator TLV (see **Table 10**) to Block 04_H

4.4.2 Transport Configuration my-d™ move NFC

SLE 66R01PN is delivered in INITIALIZED state (life cycle) according to the NFC Forum™ Type 2 Tag specification.

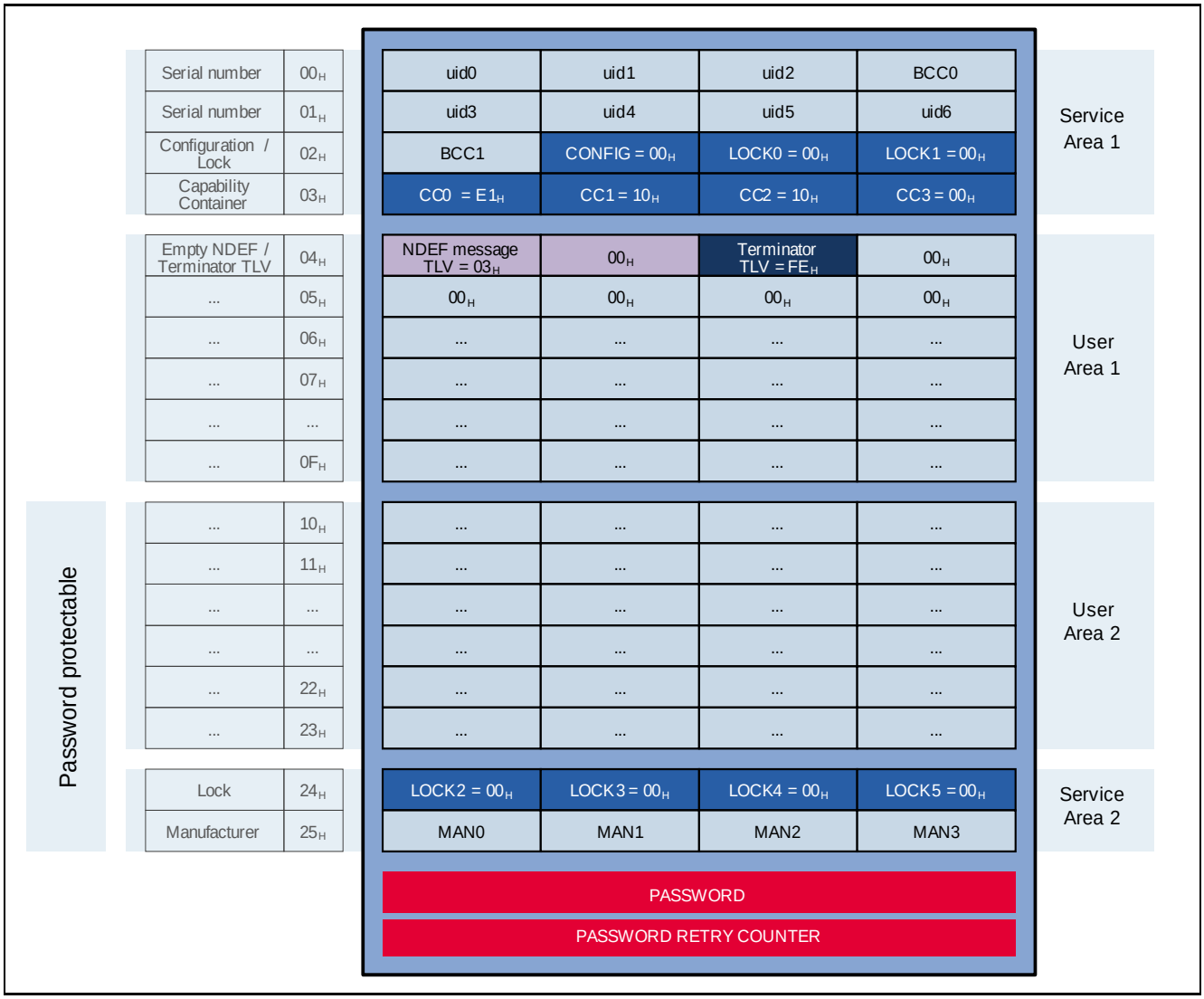

Figure 14 my-d™ move NFC Transport Configuration

- Service Area 1 contains
  - predefined UID, read-only
  - CONFIG, LOCK0 and LOCK1 set to 00_H

5 Password

An issuer can protect the blocks above address $0F_H$ with a 32 bit Write and/or Read/Write Password by enabling the password functionality.

The issuer can enable the password functionality by setting the Bit 1 (SP-W) of the Configuration Byte[1)] for Write Password access and/or bit 2 (SP-WR) of the Configuration Byte for Read/Write Password access (see **Chapter 4.2.2**).

The new configuration is activated after the next transition to IDLE/HALT state is executed.

The my-d™ move and my-d™ move NFC is delivered without Password protection i.e. default value of the SP-W and SP-WR bits is 0_B.

Table 11 Access Rights

SP-WR	SP-W	Access Right
0_B	0_B	Read Plain / Write Plain (default setting)
0_B	1_B	Read Plain / Write Protected
1_B	x_B	Read Protected / Write Protected

There is only one 32-bit Password value for both read and/or read/write access.

5.1 Password Block

The Password Block holds 32 bit of Password data and is stored in a memory location which is accessible with dedicated commands only. The initial value of the Password Block is 00_H 00_H 00_H 00_H and should be changed after delivery. The Set Password SPWD[2)] command is used to change the content of the Password Block.

- If the my-d™ move and my-d™ move NFC is not configured for a password protection i.e. bits for SP-W or SP-WR are not set, the Password Block will be overwritten with new Password data.
- If the my-d™ move and my-d™ move NFC is configured for password protection i.e. if SP-W and/or SP-WR bits are set, the Password Block will be overwritten with new Password data only after the chip has been successfully verified with the Access ACS[3)] command.

5.2 Password Retry Counter

A Password Retry Counter counts the number of incorrect accesses to a password protected my-d™ move and my-d™ move NFC. The number of incorrect accesses can be predefined by setting the bits [6:4] of the Configuration Byte. This number is called the initial value of the Password Retry Counter.

The Password Retry Counter is active if the number of incorrect accesses is higher than 0_D i.e. bit[6:4] of the Configuration Byte are NOT all set to zero. The Write One Block (WR1B) command should be used to overwrite the Password Retry Counter value. The Initial value of the Password Retry Counter is active immediately after it is written.

To prevent any further changes on a predefined Password Retry Counter value it is recommended to lock the Configuration Byte. Once the Configuration Byte is locked, the status of an initial counter value is locked, i.e. are no further changes to these bits are possible.

The my-d™ move and my-d™ move NFC is delivered with a disabled Password Retry Counter i.e. the Initial value of the Password Retry Counter is equal to 000_b. The maximum value of the Password Retry Counter is 7_D, and valid values which activate the usage of the Password Retry Counter are in the range from 1_D to 7_D.

1) For more information about Configuration Byte see **Section 4.2.2**.
2) For more information about SPWD command see **Section 8.2.6**
3) For more information about ACS command see **Section 8.2.7**

Figure 15 shows how to configure the Password functionality on the my-d™ move and my-d™ move NFC.

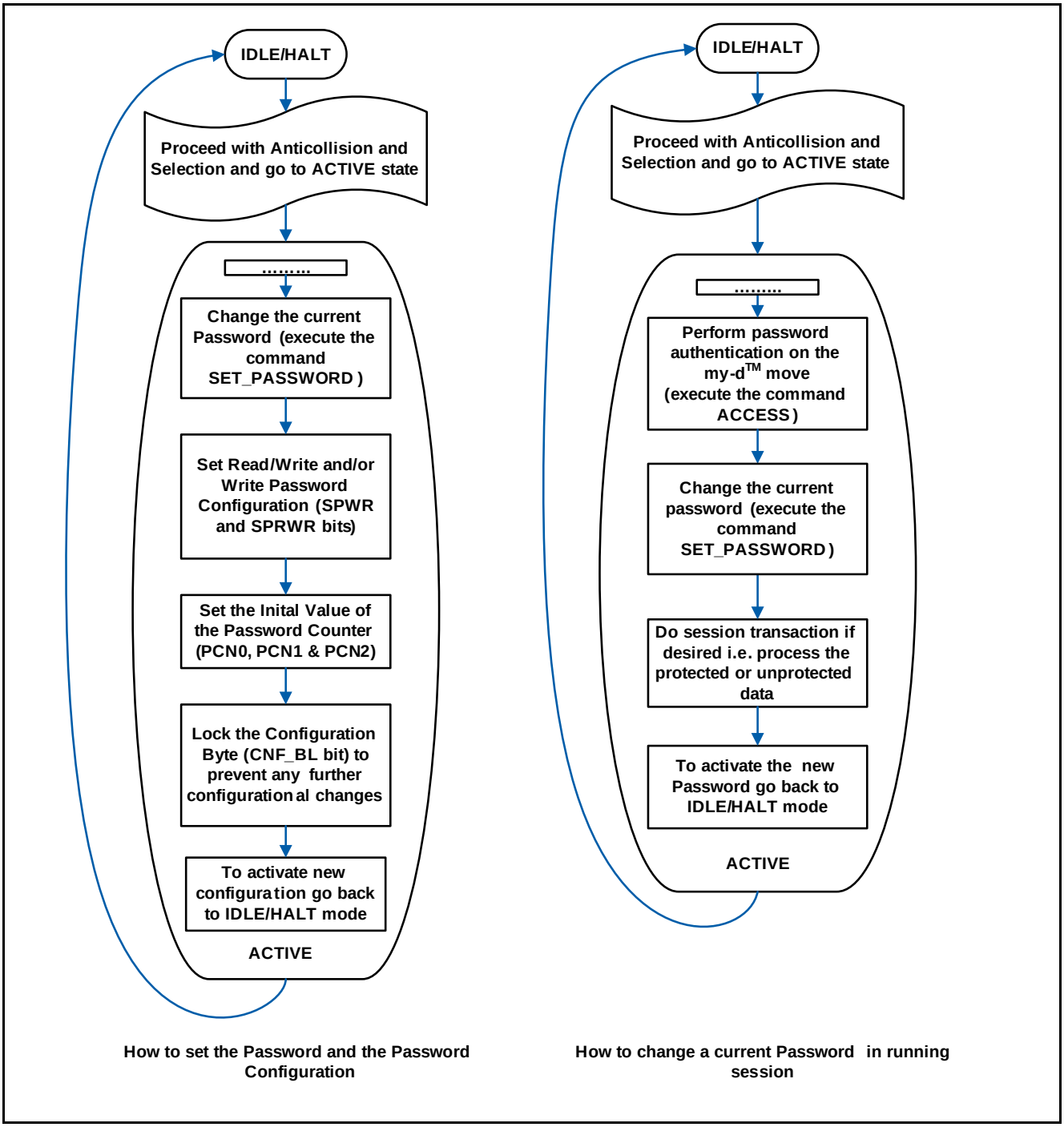

Figure 15 Password and Password Retry Counter configuration

5.3 Anti-tearing Mechanism for Password Retry Counter

The Password Retry Counter block is stored in the non-directly accessible part of the memory and for data protection reasons stored redundantly (anti-tearing). This mechanism prevents a stored value of being lost in case of a tearing event. This increases the level of data integrity and is transparent to the customer.

During the execution of the Access command the my-d™ move and my-d™ move NFC performs the following actions:

- compares the incoming Password and the Password stored in the my-d™ move and my-d™ move NFC
- Pass Retry Counter enabled:
  - resets the Password Retry Counter if the password matches. The my-d™ move and my-d™ move NFC responds with an ACK
  - increments the Password Retry Counter if the passwords do not match and if the Password Counter has not reached the highest possible value and my-d™ move and my-d™ move NFC responds with a NACK
  - if the Password Retry Counter has already reached the highest possible value (Initial Password Retry Counter value), then no further increase is done. The my-d™ move and my-d™ move NFC responds with a NACK.
    Depending on the setting of the access bits the access to the memory above block $0F_H$ is granted:
    SP-W = 1_B: read access only, no write access
    SP-RW = 1_B: no read and no write access

However the SLE 66R01P and SLE 66R01PN can directly transit from READY2/READY2* state to ACTIVE/ACTIVE* state if a read command RD2B or RD4B is executed. Any valid block address can be used in the read command. Note if more than one SLE 66R01P and SLE 66R01PN is in the reader field, all ICs are selected after the execution of the read command, although all of them have different UIDs.

Any other command or any other interruption is interpreted as an error and the SLE 66R01P and SLE 66R01PN returns back to IDLE or HALT state without any response, depending from which part it has come from.

7.2.4 ACTIVE/ACTIVE* State

In the ACTIVE/ACTIVE* state memory access commands can be executed.

If a SLE 66R01P and SLE 66R01PN is configured to have read/write or write password protection, a password verification is required to access the protected memory pages. In case of a successful password verification, read/write access to the whole memory is possible. If no verification is done or the password verification fails, the memory area above block $0F_H$ is locked according to the access rights in the Configuration Byte.

The ACTIVE/ACTIVE* state is left if the HLTA command is executed properly; the SLE 66R01P and SLE 66R01PN then transits to HALT state and waits until a WUPA command is received.

If any error command is received, the SLE 66R01P and SLE 66R01PN sends “No Response” (NR) or “Not Acknowledge” (NACK) and transits to IDLE or HALT state, depending from which state it has come from.

7.2.5 HALT State

The HLTA command sets the SLE 66R01P and SLE 66R01PN in the HALT state. The SLE 66R01P and SLE 66R01PN sends no response to the HLTA command. In the HALT state the IC can be activated again by a Wake-UP command (WUPA).

Any other data received is interpreted as an error, the SLE 66R01P and SLE 66R01PN sends no response and remains in HALT state.

The exact behavior of a particular command in any of the states above is also described in the specific command description.

Note: The response timing of a particular SLE 66R01P and SLE 66R01PN command is given in the specific command description. However, the timing values are rounded and are not on a grid according the ISO/IEC 14443-3 Type A.

7.5 Error Handling

The SLE 66R01P and SLE 66R01PN responds to valid frames only. The table below describes the behavior for different error cases.

Table 12 Behavior in case of an Error

Current States	Command or Error	Response SLE 66R01P and SLE 66R01PN	Next State
IDLE/HALT READY1/READY1* READY2/READY2*	Invalid Opcode	NR[1)]	IDLE/HALT[2)]
	Parity, Miller Error, CRC	NR	IDLE/HALT
	Command too short or too long	NR	IDLE/HALT
	Invalid Address	NR	IDLE/HALT
	Other Errors	NR	IDLE/HALT
ACTIVE/ACTIVE*	Invalid Opcode	NR	IDLE/HALT
	Parity, Miller Error, CRC	NACK1	IDLE/HALT
	Command too short or too long	NR	IDLE/HALT
	Invalid Address	NACK0	IDLE/HALT
	Other Errors	NACK0	IDLE/HALT

1) RD4B and RD2B commands in READY1/READY1* and READY2/READY2* exceptionally behave as in ACTIVE/ACTIVE* state.

2) The SLE 66R01P and SLE 66R01PN returns to IDLE or HALT state depending on the state where it has come from.

8 Command Set

8.1 Supported ISO/IEC 14443-3 Type A Command Set

The following table describes the ISO/IEC 14443-3 Type A command set which is supported by the SLE 66R01P and SLE 66R01PN.

For a detailed command description refer to the ISO/IEC 14443-3 Type A functional specification.

Table 13 ISO/IEC 14443-3 Type A Command Set

Command	Abbreviation	Op-Code	Description
Request A	REQA	26_H	Short Frame Command Type A request to all ISO/IEC 14443-3 Type A compatible chips in IDLE State
Wake Up A	WUPA	52_H	Short Frame Command,Type A Wake Up request to all ISO/IEC 14443-3 Type A compatible chips
Anticollision	AC	93_H NVB_H 95_H NVB_H	Cascade level 1 with the Number of Valid Bits Cascade level 2 with the Number of Valid Bits
Select	SELA	93_H 70_H, 95_H 70_H	Select the UID of Cascade level 1 Select the UID of Cascade level 2
HaltA	HLTA	50_H	Set a chip to a HALT State Important remark: The parameter field of the HLTA command represents the valid address range which is 00_H -25_H.

8.2 Memory Access Command Set

The command set of the SLE 66R01P and SLE 66R01PN comprises the NFC Forum™ Type 2 Tag commands as well as proprietary commands which are additionally implemented to increase data transaction time and increase the protection of the data stored in the memory.

The following table lists the memory access command set of the SLE 66R01P and SLE 66R01PN.

Table 14 my-d™ move and my-d™ move NFC memory access command set

Command	Abbreviation	Op-Code	Description
Read 4 Blocks[1)]	RD4B	30_H	This command reads 16 bytes data out of the memory starting from the specified address. A Roll-Back mechanism is implemented: - if block $0F_H$ is reached the read continues from block 00_H - if block 25_H is reached the read continues from block 00_H
Write 1 Block[2)]	WR1B	$A2_H$	If write access is granted, this command programs 4 bytes data to the specified memory address.
Compatibility Write Command	CPTWR	$A0_H$	This command sends 16 bytes to the SLE 66R01P and SLE 66R01PN but writes only the first 4 bytes of the incoming data to the specified memory address.
Read 2 Blocks[3)]	RD2B	31_H	This command reads 8 bytes out of the memory, starting from the specified address. A Roll-Back mechanism is implemented: - if block $0F_H$ is addressed, the read continues from block 00_H - if block 25_H is addressed, the read continues from block 00_H

8.2.4 Read 2 Blocks (RD2B)

RD2B command reads 8 bytes out of the memory, starting from the specified address.

The Valid Address Range is from 00_H to 25_H. If any other address is specified the SLE 66R01P and SLE 66R01PN responds with a NACK. A roll back mechanism is implemented:

- if e.g. block $0F_H$ is addressed blocks $0F_H$ and 00_H are replied.
- if e.g. block 25_H is addressed blocks 25_H and 00_H are replied.

Table 18 Read 2 Block (RD2B)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
4 bytes	31_H	Valid Address Range 00_H - 25_H	n.a.	2 bytes CRC (1 parity bit per byte)	8 bytes data + 2 bytes data CRC or NACK

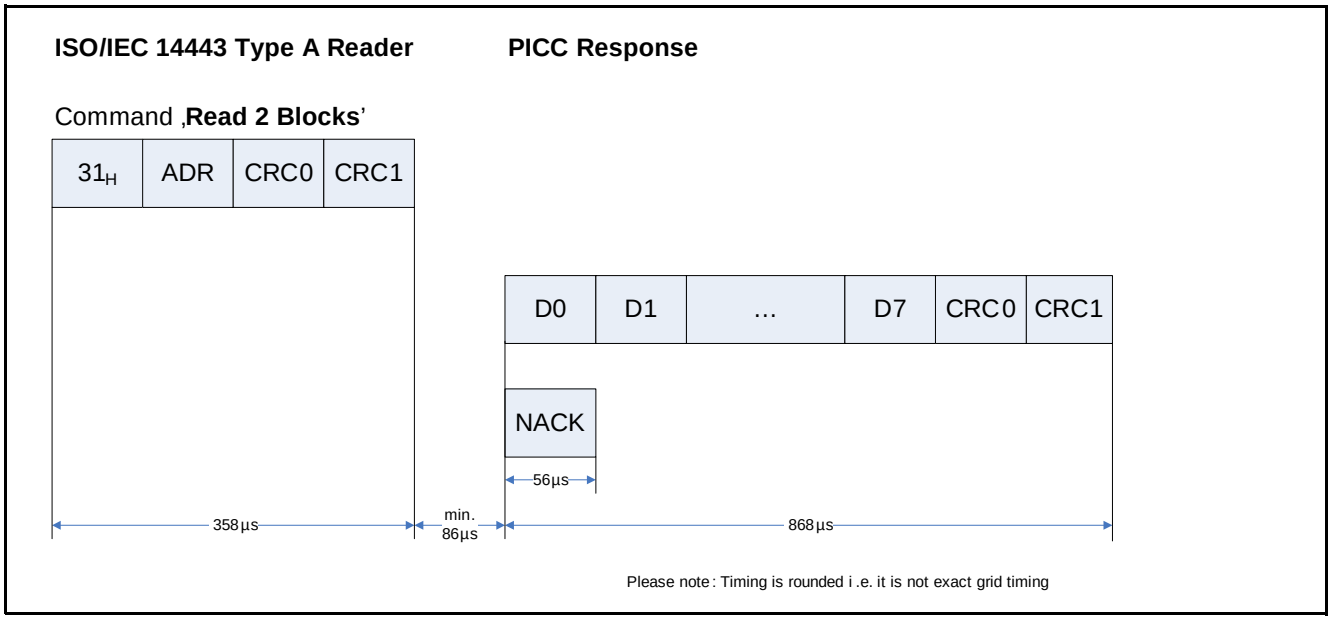

Figure 22 Read 2 Blocks Command

8.2.5 Write 2 Blocks (WR2B)

If write access is granted, i.e. if both addressed blocks are writable, the WR2B command is used to program two blocks (8 bytes of data) to the specified address in the memory.

The Valid Address Range is 04_H-22_H. Only even start addresses are allowed. If any other address is specified, the SLE 66R01P and SLE 66R01PN responds with a NACK.

The WR2B command has the same programming time (approximately 4ms) for writing 8 bytes as the WR1B command which writes 4 bytes of data to the specified memory.

Table 19 Write 2 Block (WR2B)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
12 bytes	$A1_H$	Valid Address Range 04_H - 22_H; only even start addresses allowed	8 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

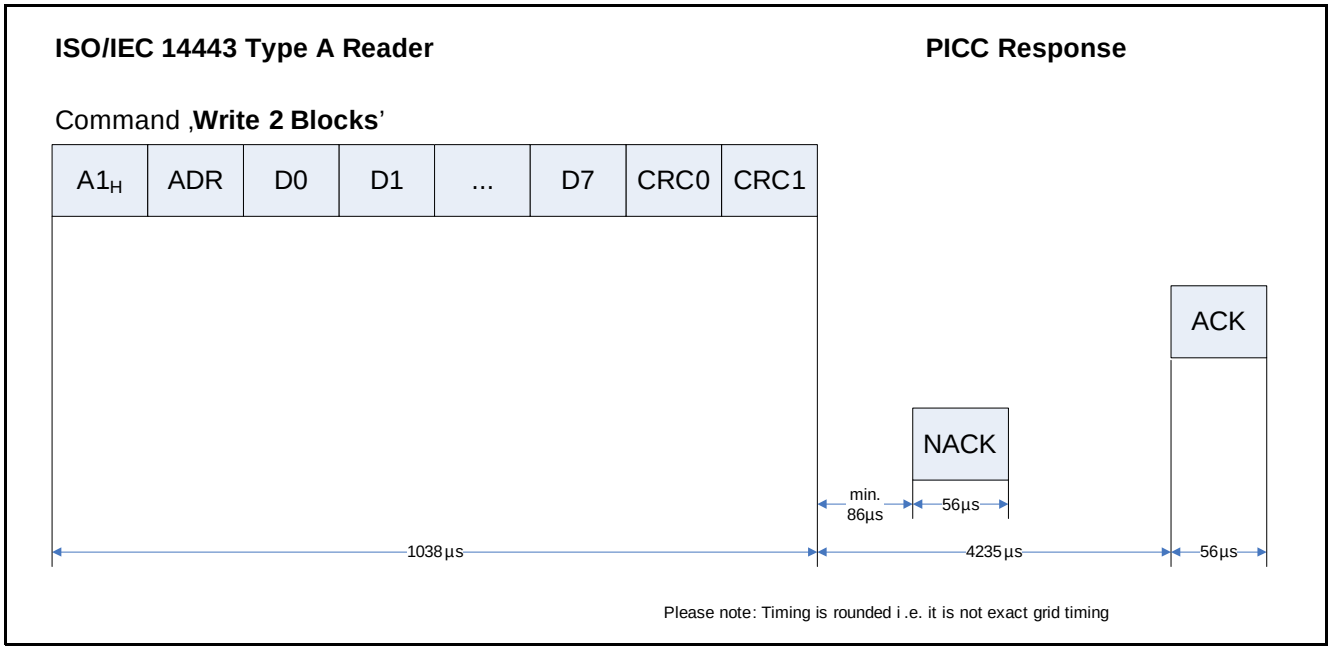

Figure 23 Write 2 Blocks Command

8.2.7 Access (ACS)

If the my-d™ move and my-d™ move NFC is configured for password protection[1)] the ACS command is used to perform a password verification. If the password verification is successful, memory access to blocks above block $0F_H$ is granted according to the access rights given in the Configuration Byte.

Additionally, if the password counter is enabled, the number of unsuccessful password verifications is counted. The ACS command is always active independently on the Password and the Password Retry Counter configuration.

- If the Password Retry Counter is not enabled, the my-d™ move responds with ACK or NACK depending on the result of password comparison.
- If the Password Retry Counter is enabled, then depending on the result of password comparison the my-d™ move and my-d™ move NFC performs the following actions:
  - If the passwords do not match and the Password Retry Counter holds a lower value than its Initial value, the my-d™ move increments the Password Retry Counter and responds with a NACK.
  - If the passwords match and the Password Retry Counter holds a lower value then its Initial value, the my-d™ move resets the Password Retry Counter and responds with a ACK.
  - In any other case the my-d™ move responds with a NACK and limits access to blocks above block $0F_H$ according to access rights stored in the Configuration Byte.

Table 22 Access (ACS)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
7 bytes	$B2_H$	n.a.	4 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

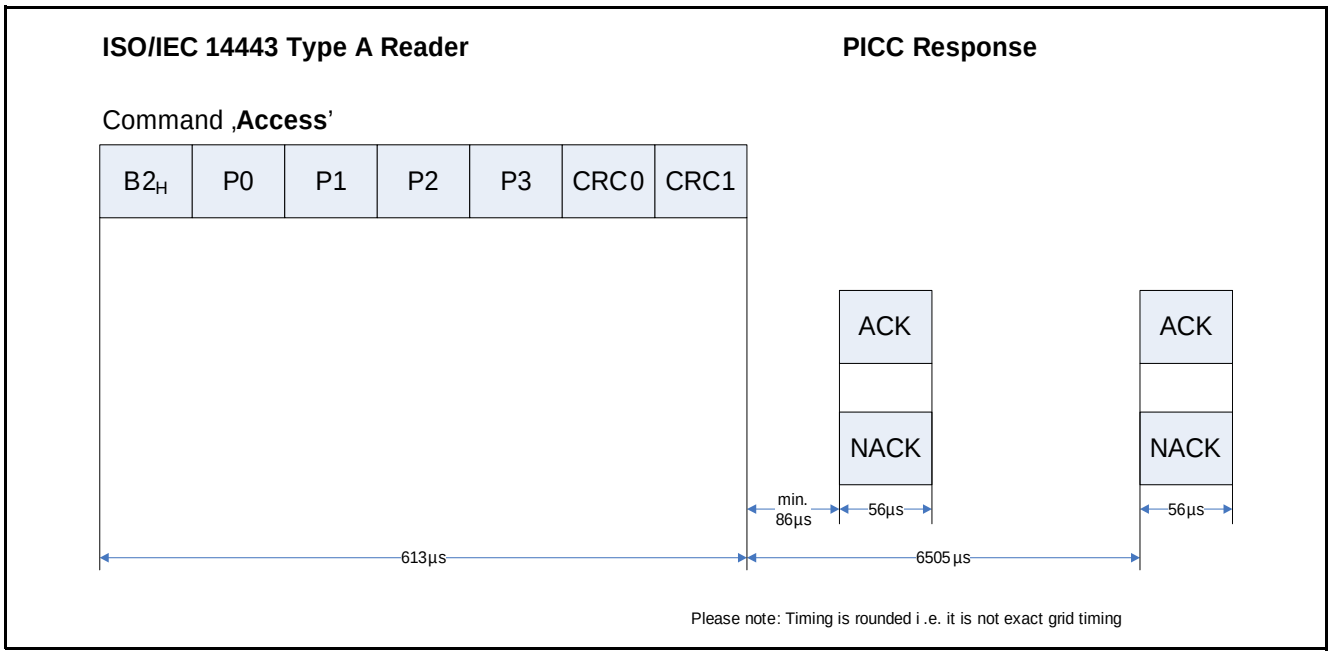

Figure 25 Access Command

1) For more information about password please read **Chapter 5**.

The figure below shows the flow diagram of the Access command.

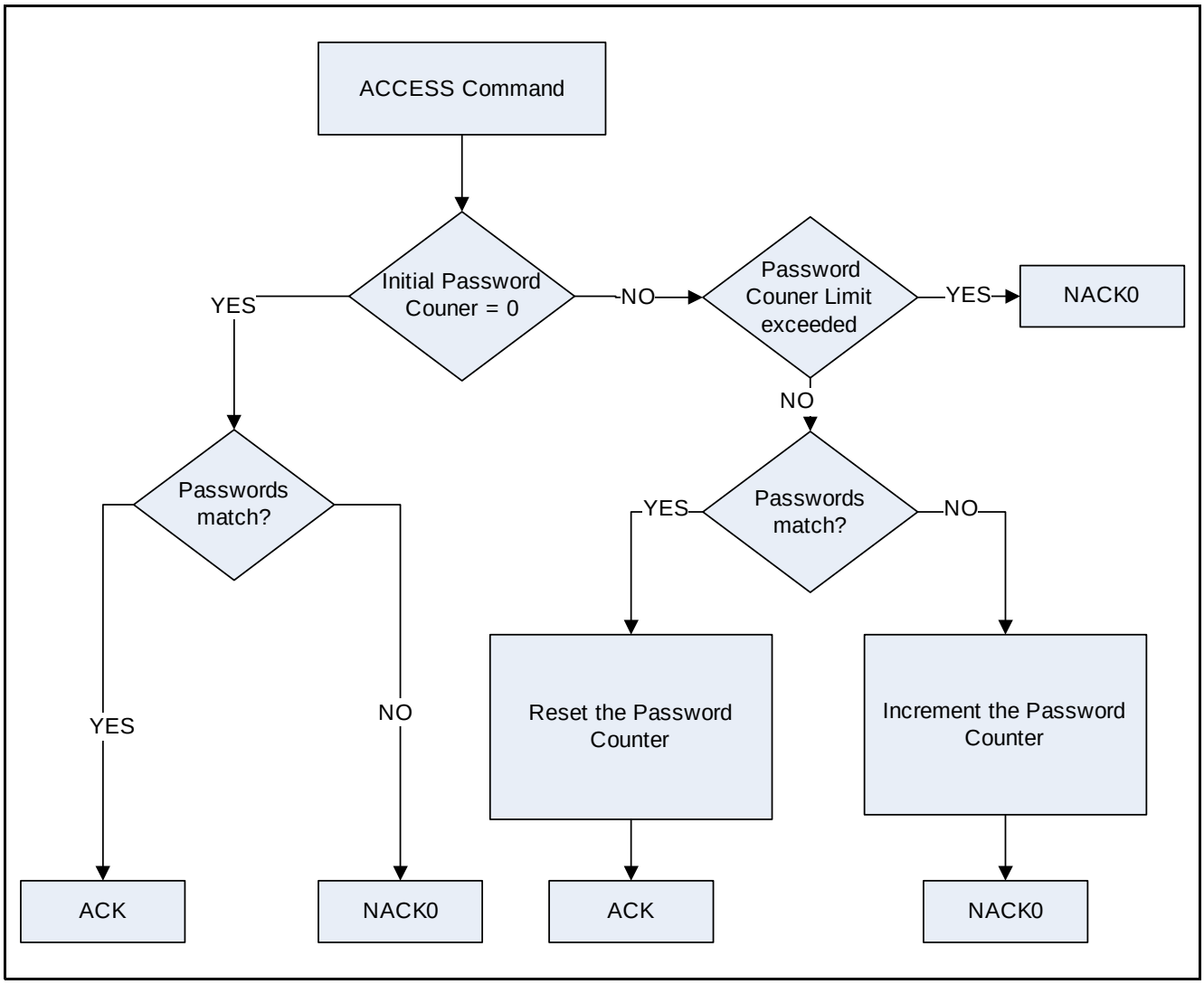

Figure 26 Flow Diagram of the ACS Command

Table 23 ACS - behaviour in error case

Error / State	Idle/Halt	Ready	Active	Protected
Invalid Opcode	NR	NR	NR	NR
Parity, Miller	NR	NR	NACK1	NACK1
Command Length	NR	NR	NR	NR
CRC	NR	NR	NACK1	NACK1
Password Counter limit exceeded	NR	NR	NACK0	NACK0
Passwords do not match	NR	NR	NACK0	n.a.
HV not OK	NR	NR	NR	NR

8.2.8 Decrement Command (DCR16)

The DCR16 command decrements the current Value Counter value by the received parameter and writes the new value to the Value Counter block. If this command is executed properly, the my-d™ move and my-d™ move NFC responds the new written value. Note that the parameter has to be lower or equal to the current Value Counter value.

Table 24 Decrement (DCR16)

Command Length	Code	Parameter	Data	Integrity Mechanism	Response
5 bytes	$D0_H$	2 bytes; LSByte = CNT0 MSByte = CNT1	n.a.	2 bytes CRC 1 parity bit per byte	• If the parameter is lower or equal to the current Value Counter Value, the response is the new decremented value: 2 bytes data + 2 bytes CRC • If the parameter is 0000_H the response is the current Value Counter value • If the parameter is higher than the current Value Counter value the response is a NACK

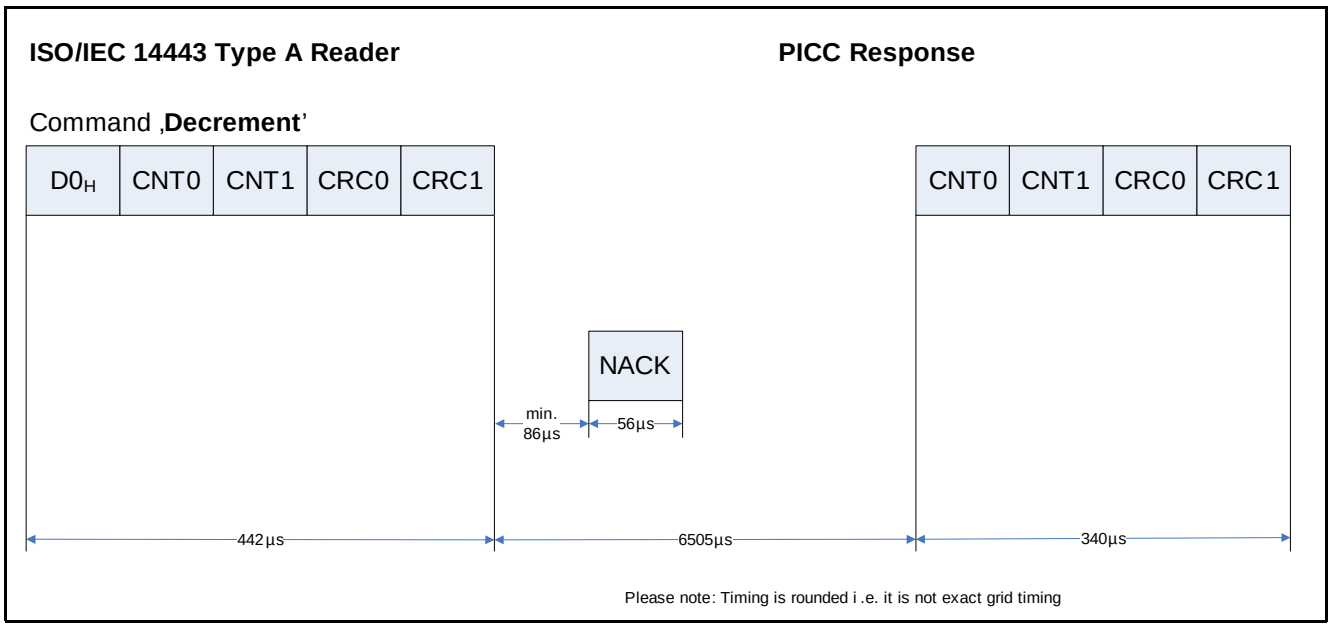

Figure 27 Decrement Command

After receiving the correct DCR16 command, the my-d™ move and my-d™ move NFC performs the following actions:

- checks the format of the current Value Counter by reading blocks 22_H and 23_H;
- determines the valid and the invalid Value Counter value;
- decrements the current valid value by the received parameter;
- expands the result to the correct Value Counter format;
- writes the new Value Counter value, in the correct format, to the previously determined invalid block
- erases the current valid Value Counter value to FF_H FF_H FF_H FF_H

In case of a successful programming of a Value Counter value, the my-d™ move and my-d™ move NFC sends the new written value of the Value Counter block back. If the programming was unsuccessful (due to insufficient power) “No Response” is replied.

8.3 my-d™ move and my-d™ move NFC responses

Following sections list valid responses of the SLE 66R01P and SLE 66R01PN

8.3.1 Command responses

The Acknowledge (ACK) and Not-Acknowledge (NACK) are command responses of the SLE 66R01P and SLE 66R01PN.

Table 27 ACK and NACK as responses

Response	Code (4 bits)	Integrity Mechanism
ACK	A_H	n.a.
NACK0	0_H	n.a.
NACK1	1_H	n.a.
NR[1)]	n.a.	n.a.

1) Depending on the current state, the SLE 66R01P and SLE 66R01PN does not respond to some errors.

The response code is A_H for ACK and 0_H or 1_H for NACK. The ACK and NACK are sent as 4 bit response with no CRC and/or parity.

8.3.2 my-d™ move and my-d™ move NFC identification data

During the anti-collision the SLE 66R01P and SLE 66R01PN sends responses to the REQA and SEL commands.

Table 28 Summary of SLE 66R01P and SLE 66R01PN identification data

Code	Data	Description
ATQA	0044_H	Answer to Request, response to REQA and WUPA command, hard coded 2 bytes. Indicates a double-size UID.
SAK (cascade level 1)	04_H	Select Acknowledge answer to selection of 1st cascade level. Indicates that the UID is incomplete.
SAK (cascade level 2)	00_H	Select Acknowledge answer to selection of 2nd cascade level. Indicates that the UID is complete.
CT	88_H	Cascade Tag Indicates that UID is not single size UID.

9 Operational Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_{ambient}$ = 25°C and the given supply voltage.

9.1 Electrical Characteristics

f_{CAR} = 13.56 MHz sinusoidal waveform, voltages refer to VSS.

Table 29 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Chip input capacitance L_A-L_B	C_{IN}	16.15	17	17.85	pF	$V_{AB\ peak}$ = 3.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 ℃
Chip load resistance L_A-L_B	R_{IN}	3	4.5	6	kΩ	$V_{AB\ peak}$ = 3.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 ℃
Endurance (erase/write cycles)[1)]		10^4				–
Data retention[1)]		5			years	
EEPROM Erase and Write time	t_{prog}			3.8	ms	Combined erase + write; excluding time for command / response transfer between interrogator and chip, $T_{ambient}$ = 25 ℃
ESD Protection voltage (L_A, L_B pins)	V_{ESD}	2			kV	JEDEC STD EIA / JESD22 A114-B
Ambient temperature	$T_{ambient}$	-25		+70	℃	for chip
Junction temperature	$T_{junction}$	-25		+110	℃	for chip

1) Values are temperature dependent