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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFLGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0500afc-aa3-a

(1) Port functions (2/2): 78K0/KC2

Function Name	I/O	Function	After Reset	Alternate Function
P120	I/O	Port 12. 5-bit I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121				X1/OCD0A[Note 1]
P122				X2/EXCLK/OCD0B[Note 1]
P123				XT1
P124				XT2/EXCLKS
P130[Note 2]	Output	Port 13. 1-bit output-only port.	Output port	–
P140[Note 2]	I/O	Port 14. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCL/INTP6[Note 2]

Notes 1. μPD78F0513D, 78F0513DA, 78F0515D and 78F0515DA (product with on-chip debug function) only

2. 48-pin products only

(2) Non-port functions (1/2): 78K0/KC2

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI5	Input	A/D converter analog input	Analog input	P20 to P25
ANI6[Note 1], ANI7[Note 1]				P26[Note 1], P27[Note 1]
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
EXSCL0	Input	External clock input for serial interface. To input an external clock, input a clock of 6.4 MHz.	Input port	P62
FLMD0	–	Flash memory programming mode setting	–	–
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P30
INTP2				P31/OCD1A[Note 2]
INTP3				P32/OCD1B[Note 2]
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
INTP6[Note 3]				P140/PCL[Note 3]
KR0, KR1	Input	Key interrupt input	Input port	P70, P71
KR2[Note 1], KR3[Note 1]				P72[Note 1], P73[Note 1]
PCL[Note 3]	Output	Clock output (for trimming of high-speed system clock, subsystem clock)	Input port	P140/INTP6[Note 3]

Notes 1. 44-pin and 48-pin products only
For the 38-pin products, be sure to set bits 6 and 7 of PM2 to “1”, and bits 2 and 3 of PM7, bits 6 and 7 of P2, and bits 2 and 3 of P7 to “0”.

2. μPD78F0513D, 78F0513DA, 78F0515D and 78F0515DA (product with on-chip debug function) only

3. 48-pin products only

3.1.1 Internal program memory space

The internal program memory space stores the program and table data. Normally, it is addressed with the program counter (PC).

78K0/Kx2 microcontrollers incorporate internal ROM (flash memory), as shown below.

Table 3-4. Internal ROM Capacity

78K0/KB2	78K0/KC2		78K0/KD2	78K0/KE2	78K0/KF2	Internal ROM (Flash memory)
30/36 Pins	38/44 Pins	48 Pins	52 Pins	64 Pins	80 Pins	
μPD78F0500, PD78F0500A	–	–	–	–	–	8192 × 8 bits (0000H to 1FFFH)
μPD78F0501, 78F0501A	μPD78F0511, 78F0511A	μPD78F0511, 78F0511A	μPD78F0521, 78F0521A	μPD78F0531, 78F0531A	–	16384 × 8 bits (0000H to 3FFFH)
μPD78F0502, 78F0502A	μPD78F0512, 78F0512A	μPD78F0512, 78F0512A	μPD78F0522, 78F0522A	μPD78F0532, 78F0532A	–	24576 × 8 bits (0000H to 5FFFH)
μPD78F0503D, 78F0503DA	μPD78F0513D, 78F0513DA	μPD78F0513, 78F0513A	μPD78F0523, 78F0523A	μPD78F0533, 78F0533A	–	32768 × 8 bits (0000H to 7FFFH)
μPD78F0503, 78F0503A	μPD78F0513, 78F0513A					
–	–	μPD78F0514, 78F0514A	μPD78F0524, 78F0524A	μPD78F0534, 78F0534A	μPD78F0544, 78F0544A	49152 × 8 bits (0000H to BFFFH)
–	–	μPD78F0515D, 78F0515DA	μPD78F0525, 78F0525A	μPD78F0535, 78F0535A	μPD78F0545, 78F0545A	61440 × 8 bits (0000H to EFFFH)
		μPD78F0515, 78F0515A				
–	–	–	μPD78F0526, 78F0526A	μPD78F0536, 78F0536A	μPD78F0546, 78F0546A	98304 × 8 bits (0000H to 7FFFH (common area: 32 KB) + 8000H to BFFFH (bank area: 16 KB) × 4)
–	–	–	μPD78F0527D, 78F0527DA	μPD78F0537D, 78F0537DA	μPD78F0547D, 78F0547DA	131072 × 8 bits (0000H to 7FFFH (common area: 32 KB) + 8000H to BFFFH (bank area: 16 KB) × 6)
			μPD78F0527, 78F0527A	μPD78F0537, 78F0537A	μPD78F0547, 78F0547A	

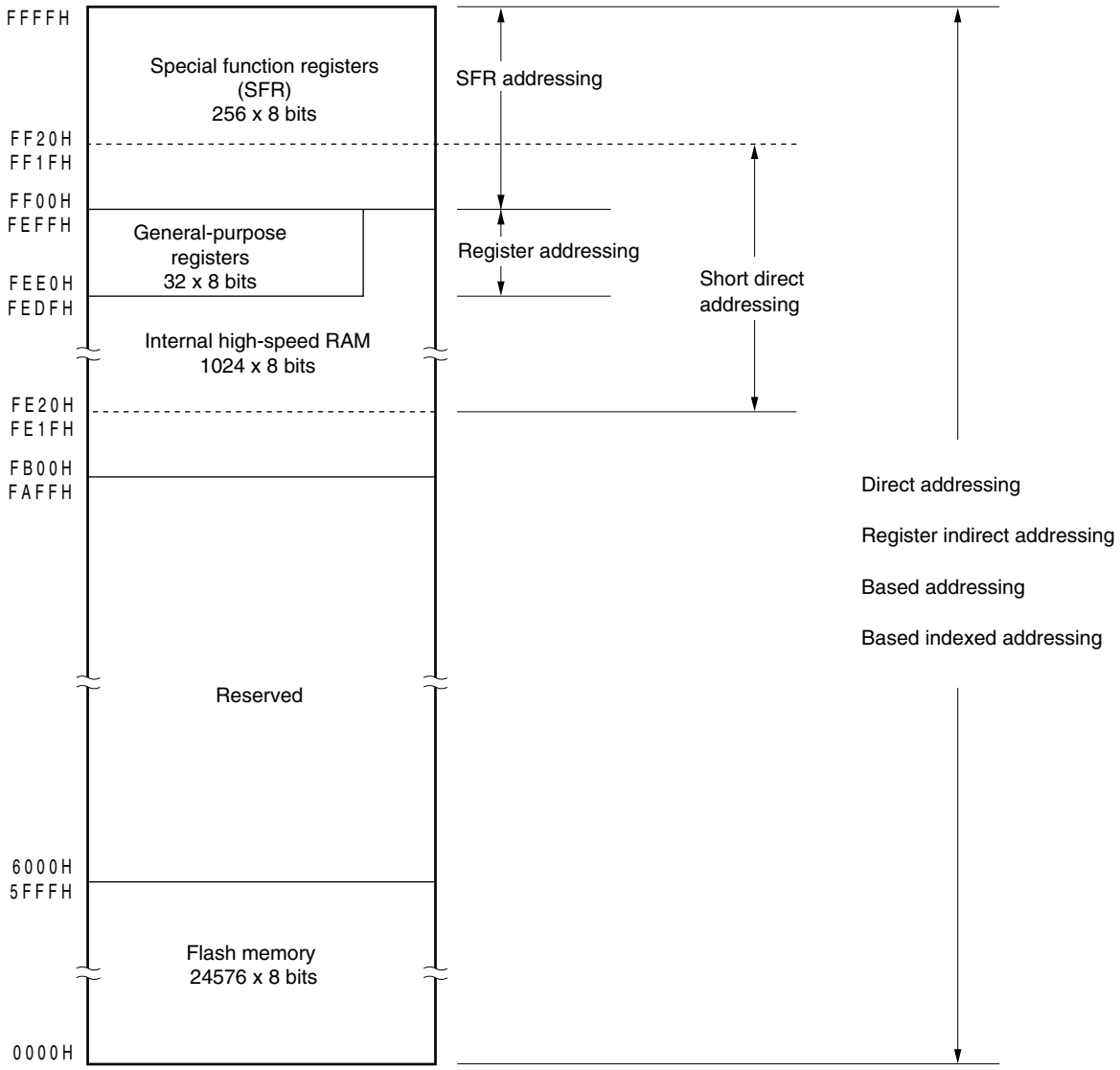
The internal program memory space is divided into the following areas.

(1) Vector table area

The 64-byte area 0000H to 003FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

Figure 3-14. Correspondence Between Data Memory and Addressing
(μPD78F0502, 78F0502A, 78F0512, 78F0512A, 78F0522, 78F0522A, 78F0532, and 78F0532A)



5.2.5 Port 4

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P40	–	√Note	√	√		√
P41	–	√Note	√	√		√
P42	–	–		√		√
P43	–	–		√		√
P44	–	–		–		√
P45	–	–		–		√
P46	–	–		–		√
P47	–	–		–		√

Note This is not mounted onto 38-pin products of the 78K0/KC2. For the 38-pin products, be sure to set bits 0 and 1 of PM4 and P4 to “0”.

Remark √: Mounted, –: Not mounted

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P47 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4).

Reset signal generation sets port 4 to input mode.

Figure 5-15 shows a block diagram of port 4.

Figure 5-30. Format of Port Mode Register (78K0/KC2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	1	1	PM01	PM00	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM4	1	1	1	1	1	1	PM41	PM40	FF24H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	PM75[Note]	PM74[Note]	PM73	PM72	PM71	PM70	FF27H	FFH	R/W
PM12	1	1	1	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W
PM14[Note]	1	1	1	1	1	1	1	PM140[Note]	FF2EH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 4, 6, 7, 12, 14; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note 48-pin products only

Caution For the 38-pin products, be sure to set bits 2 to 7 of PM0, bits 6 and 7 of PM2, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 4 to 7 of PM7, and bits 5 to 7 of PM12 to "1". Also, be sure to set bits 0 and 1 of PM4, and bits 2 and 3 of PM7 to "0".
For the 44-pin products, be sure to set bits 2 to 7 of PM0, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 4 to 7 of PM7, and bits 5 to 7 of PM12 to "1".
For the 48-pin products, be sure to set bits 2 to 7 of PM0, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 6 and 7 of PM7, bits 5 to 7 of PM12, and bits 1 to 7 of PM14 to "1".

Table 5-6. Settings of Port Mode Register and Output Latch When Using Alternate Function (1/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P00	TI000	Input	1	×
P01	TI010	Input	1	×
	TO00	Output	0	0
P02	SO11	Output	0	0
P03	SI11	Input	1	×
P04	$\overline{SCK11}$	Input	1	×
		Output	0	1
P05	$\overline{SSI11}$	Input	1	×
	TI001	Input	1	×
P06	TI011	Input	1	×
	TO01	Output	0	0
P10	$\overline{SCK10}$	Input	1	×
		Output	0	1
	TxD0	Output	0	1
P11	SI10	Input	1	×
	RxD0	Input	1	×
P12	SO10	Output	0	0
P13	TxD6	Output	0	1
P14	RxD6	Input	1	×
P15	TOH0	Output	0	0
P16	TOH1	Output	0	0
	INTP5	Input	1	×
P17	TI50	Input	1	×
	TO50	Output	0	0
P20 to P27[Note]	ANI0 to ANI7[Note]	Input	1	×

Note The function of the ANI0/P20 to ANI7/P27 pins can be selected by using the A/D port configuration register (ADPC), the analog input channel specification register (ADS), and PM2.

ADPC	PM2	ADS	ANI0/P20 to ANI7/P27 Pins
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output

Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

Table 5-6. Settings of Port Mode Register and Output Latch When Using Alternate Function (2/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P30 to P32	INTP1 to INTP3	Input	1	×
P33	INTP4	Input	1	×
	TI51	Input	1	×
	TO51	Output	0	0
P60	SCL0	I/O	0	0
P61	SDA0	I/O	0	0
P62	EXSCL0	Input	1	×
P70 to P77	KR0 to KR7	Input	1	×
P120	INTP0	Input	1	×
	EXLVI	Input	1	×
P121	X1[Note]	–	×	×
P122	X2[Note]	–	×	×
	EXCLK[Note]	Input	×	×
P123	XT1[Note]	–	×	×
P124	XT2[Note]	–	×	×
	EXCLKS[Note]	Input	×	×
P140	PCL	Output	0	0
	INTP6	Input	1	×
P141	BUZ	Output	0	0
	INTP7	Input	1	×
	BUSY0	Input	1	×
P142	$\overline{\text{SCKA0}}$	Input	1	×
		Output	0	1
P143	SIA0	Input	1	×
P144	SOA0	Output	0	0
P145	STB0	Output	0	0

Note When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK) or subsystem clock (EXCLKS), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **6.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are I/O port pins). At this time, setting of PM121 to PM124 and P121 to P124 is not necessary.

Remarks 1. ×: Don't care
PM××: Port mode register
P××: Port output latch

2. X1, X2, P31, and P32 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A, OCD0B, OCD1A, and OCD1B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD AND 78F05xxDA ONLY).**

5.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0/Kx2 microcontrollers.

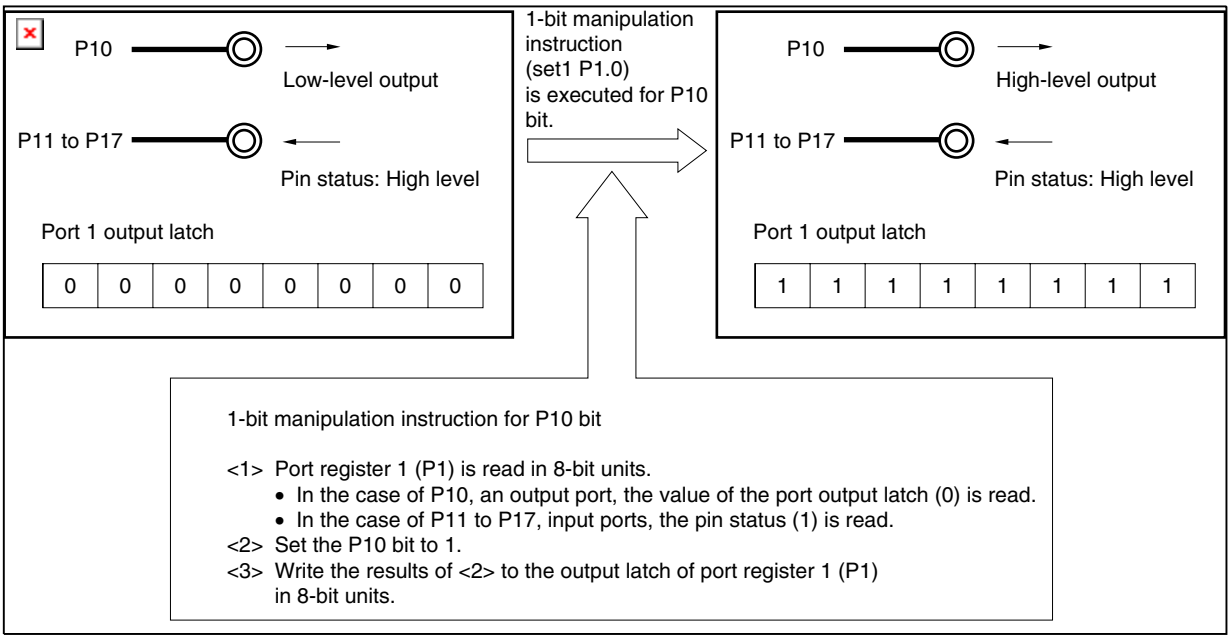
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 5-45. Bit Manipulation Instruction (P10)



6.6.4 Example of controlling internal low-speed oscillation clock

The internal low-speed oscillation clock cannot be used as the CPU clock.

Only the following peripheral hardware can operate with this clock.

- Watchdog timer
- 8-bit timer H1 (if f_{RL} is selected as the count clock)

In addition, the following operation modes can be selected by the option byte.

- Internal low-speed oscillator cannot be stopped
- Internal low-speed oscillator can be stopped by software

The internal low-speed oscillator automatically starts oscillation after a reset release, and the watchdog timer is driven (240 kHz (TYP.)) if the watchdog timer operation has been enabled by the option byte.

(1) Example of setting procedure when stopping the internal low-speed oscillation clock

<1> Setting LSRSTOP to 1 (RCM register)

When LSRSTOP is set to 1, the internal low-speed oscillation clock is stopped.

(2) Example of setting procedure when restarting oscillation of the internal low-speed oscillation clock

<1> Clearing LSRSTOP to 0 (RCM register)

When LSRSTOP is cleared to 0, the internal low-speed oscillation clock is restarted.

Caution If "Internal low-speed oscillator cannot be stopped" is selected by the option byte, oscillation of the internal low-speed oscillation clock cannot be controlled.

7.4.2 Square-wave output operation

When 16-bit timer/event counter 0n operates as an interval timer (see **7.4.1**), a square wave can be output from the TO0n pin by setting the 16-bit timer output control register 0n (TOC0n) to 03H.

When TMC0n3 and TMC0n2 are set to 11 (count clear & start mode entered upon a match between TM0n and CR00n), the counting operation is started in synchronization with the count clock.

When the value of TM0n later matches the value of CR00n, TM0n is cleared to 0000H, an interrupt signal (INTTM00n) is generated, and TO0n output is inverted. This TO0n output that is inverted at fixed intervals enables TO0n to output a square wave.

Remarks 1. For the setting of I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 7-20. Block Diagram of Square-Wave Output Operation

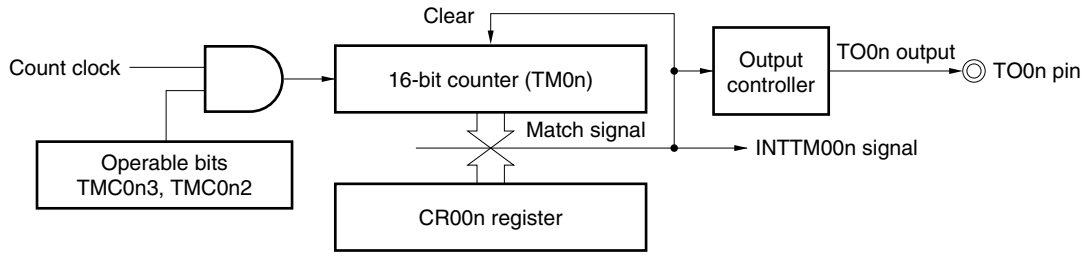
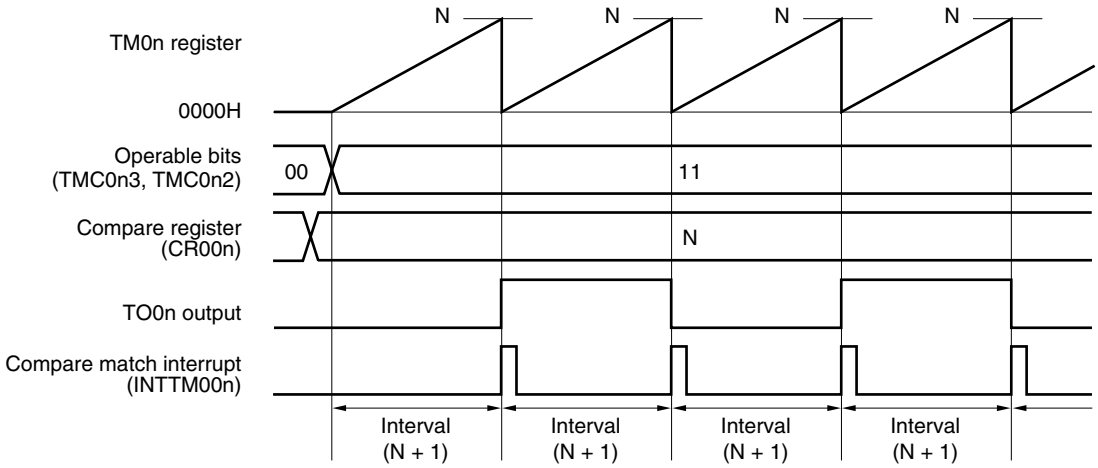


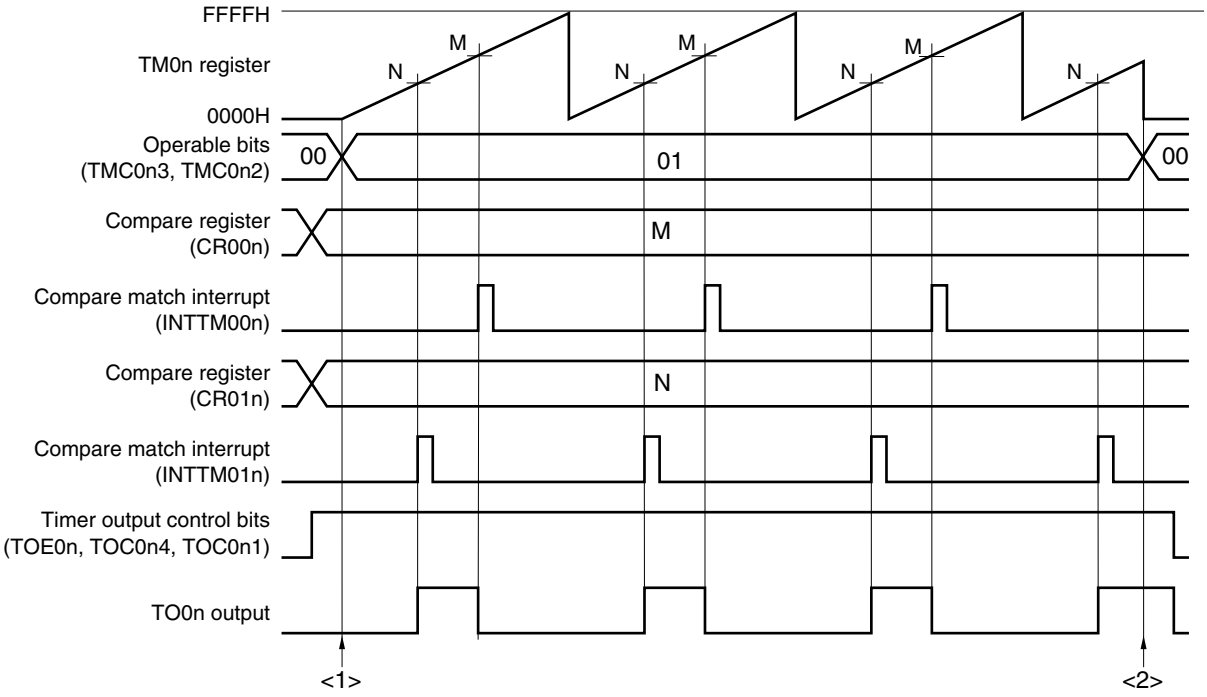
Figure 7-21. Basic Timing Example of Square-Wave Output Operation



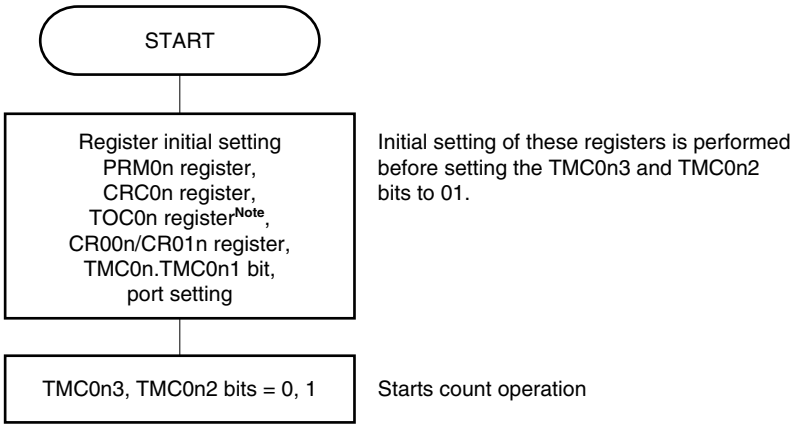
Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

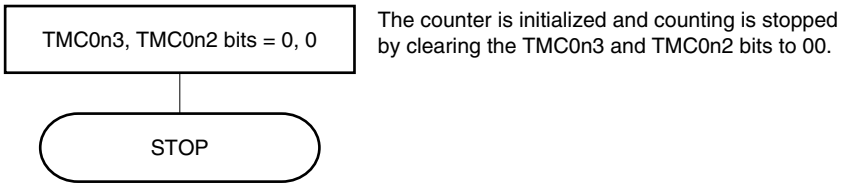
Figure 7-44. Example of Software Processing in Free-Running Timer Mode



<1> Count operation start flow



<2> Count operation stop flow



Note Care must be exercised when setting TOC0n. For details, see **7.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

9.4.3 Carrier generator operation (8-bit timer H1 only)

In the carrier generator mode, the 8-bit timer H1 is used to generate the carrier signal of an infrared remote controller, and the 8-bit timer/event counter 51 is used to generate an infrared remote control signal (time count).

The carrier clock generated by the 8-bit timer H1 is output in the cycle set by the 8-bit timer/event counter 51.

In carrier generator mode, the output of the 8-bit timer H1 carrier pulse is controlled by the 8-bit timer/event counter 51, and the carrier pulse is output from the TOH1 output.

(1) Carrier generation

In carrier generator mode, the 8-bit timer H compare register 01 (CMP01) generates a low-level width carrier pulse waveform and the 8-bit timer H compare register 11 (CMP11) generates a high-level width carrier pulse waveform.

Rewriting the CMP11 register during the 8-bit timer H1 operation is possible but rewriting the CMP01 register is prohibited.

(2) Carrier output control

Carrier output is controlled by the interrupt request signal (INTTM51) of the 8-bit timer/event counter 51 and the NRZB1 and RMC1 bits of the 8-bit timer H carrier control register (TMCYC1). The relationship between the outputs is shown below.

RMC1 Bit	NRZB1 Bit	Output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- $\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 2.5 MHz = 2,500,000 Hz
Set value of MDL04 to MDL00 bits of BRGC0 register = 10000B (k = 16)
Target baud rate = 76,800 bps

Baud rate = 2.5 M/(2 × 16)
= 2,500,000/(2 × 16) = 78,125 [bps]

Error = (78,125/76,800 − 1) × 100
= 1.725 [%]

(3) Example of setting baud rate

Table 14-5. Set Data of Baud Rate Generator

Baud Rate [bps]	f_{PRS} = 2.0 MHz				f_{PRS} = 5.0 MHz				f_{PRS} = 10.0 MHz				f_{PRS} = 20.0 MHz			
	TPS01, TPS00	k	Calculated Value	ERR [%]	TPS01, TPS00	k	Calculated Value	ERR [%]	TPS01, TPS00	k	Calculated Value	ERR [%]	TPS01, TPS00	k	Calculated Value	ERR [%]
4800	2H	26	4808	0.16	3H	16	4883	1.73	–	–	–	–	–	–	–	–
9600	2H	13	9615	0.16	3H	8	9766	1.73	3H	16	9766	1.73	–	–	–	–
10400	2H	12	10417	0.16	2H	30	10417	0.16	3H	15	10417	0.16	3H	30	10417	0.16
19200	1H	26	19231	0.16	2H	16	19531	1.73	3H	8	19531	1.73	3H	16	19531	1.73
24000	1H	21	23810	−0.79	2H	13	24038	0.16	2H	26	24038	0.16	3H	13	24038	0.16
31250	1H	16	31250	0	2H	10	31250	0	2H	20	31250	0	3H	10	31250	0
33600	1H	15	33333	−0.79	2H	9	34722	3.34	2H	19	32895	−2.1	3H	9	34722	3.34
38400	1H	13	38462	0.16	2H	8	39063	1.73	2H	16	39063	1.73	3H	8	39063	1.73
56000	1H	9	55556	−0.79	1H	22	56818	1.46	2H	11	56818	1.46	2H	22	56818	1.46
62500	1H	8	62500	0	1H	20	62500	0	2H	10	62500	0	2H	20	62500	0
76800	–	–	–	–	1H	16	78125	1.73	2H	8	78125	1.73	2H	16	78125	1.73
115200	–	–	–	–	1H	11	113636	−1.36	1H	22	113636	−1.36	2H	11	113636	−1.36
153600	–	–	–	–	1H	8	156250	1.73	1H	16	156250	1.73	2H	8	156250	1.73
312500	–	–	–	–	–	–	–	–	1H	8	312500	0	1H	16	312500	0
625000	–	–	–	–	–	–	–	–	–	–	–	–	1H	8	625000	0

Remark TPS01, TPS00: Bits 7 and 6 of baud rate generator control register 0 (BRGC0) (setting of base clock (f_{XCLK0}))
k: Value set by the MDL04 to MDL00 bits of BRGC0 (k = 8, 9, 10, ..., 31)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

(14) Bus status detector

This circuit detects whether or not the bus is released by detecting start conditions and stop conditions.

However, as the bus status cannot be detected immediately following operation, the initial status is set by the STCEN bit.

Remark STT0 bit: Bit 1 of IIC control register 0 (IICC0)
SPT0 bit: Bit 0 of IIC control register 0 (IICC0)
IICRSV bit: Bit 0 of IIC flag register 0 (IICF0)
IICBSY bit: Bit 6 of IIC flag register 0 (IICF0)
STCF bit: Bit 7 of IIC flag register 0 (IICF0)
STCEN bit: Bit 1 of IIC flag register 0 (IICF0)

18.3 Registers to Control Serial Interface IIC0

Serial interface IIC0 is controlled by the following seven registers.

- IIC control register 0 (IICC0)
- IIC flag register 0 (IICF0)
- IIC status register 0 (IICS0)
- IIC clock selection register 0 (IICCL0)
- IIC function expansion register 0 (IICX0)
- Port mode register 6 (PM6)
- Port register 6 (P6)

(1) IIC control register 0 (IICC0)

This register is used to enable/stop I^2C operations, set wait timing, and set other I^2C operations.

IICC0 register is set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIE0, WTIM0, and ACKE0 bits while IICE0 bit = 0 or during the wait period. These bits can be set at the same time when the IICE0 bit is set from “0” to “1”.

Reset signal generation clears IICC0 to 00H.

(5) Setting STT0 and SPT0 bits (bits 1 and 0 of IICC0 register) again after they are set and before they are cleared to 0 is prohibited.

(6) When transmission is reserved, set SPIE0 bit (bit 4 of IICL0 register) to 1 so that an interrupt request is generated when the stop condition is detected. Transfer is started when communication data is written to IIC status register 0 (IICS0) after the interrupt request is generated. Unless the interrupt is generated when the stop condition is detected, the device stops in the wait state because the interrupt request is not generated when communication is started. However, it is not necessary to set SPIE0 bit to 1 when MSTS0 bit (bit 7 of IIC status register 0 (IICS0) is detected by software.

18.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the 78K0/Kx2 microcontrollers as the master in a single master system is shown below.
This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the 78K0/Kx2 microcontrollers takes part in a communication with bus released state.
This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the 78K0/Kx2 microcontrollers looses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

An example of when the 78K0/Kx2 microcontrollers is used as the I^2C bus slave is shown below.
When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIIC0 interrupt occurrence (communication waiting). When an INTIIC0 interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.
By checking the flags, necessary communication processing is performed.

Figure 20-10. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KE2)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	SREMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK010	TMMK000	TMMK50	TMMKH0	TMMKH1	DUALMK0 CSIMK10 STMK0	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	PMK7	PMK6	WTMK	KRMK	TMMK51	WTIMK	SRMK0	ADMK

Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
MK1H	1	1	1	1	TMMK011[Note]	TMMK001[Note]	CSIMK11[Note]	IICMK0 DMUMK[Note]

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note Products whose flash memory is at least 48 KB only.

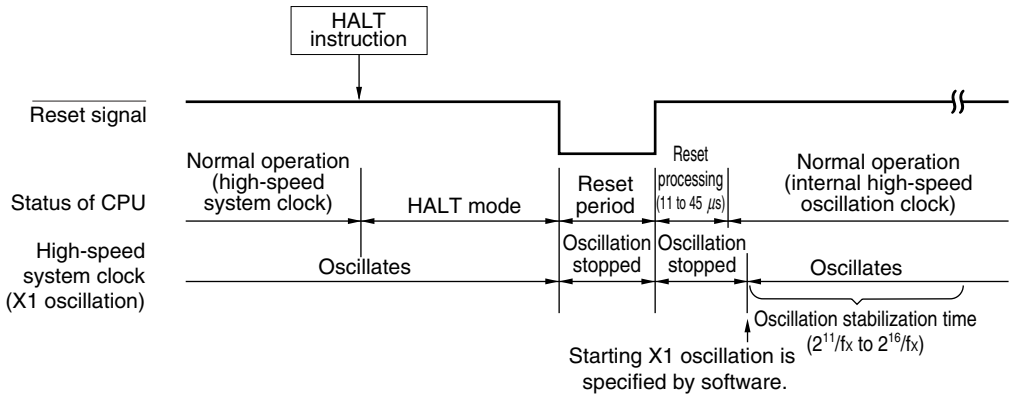
Caution Be sure to set bits 1 to 7 of MK1H to 1 for the products whose flash memory is less than 32 KB. Be sure to set bits 4 to 7 of MK1H to 1 for the products whose flash memory is at least 48 KB.

(b) Release by reset signal generation

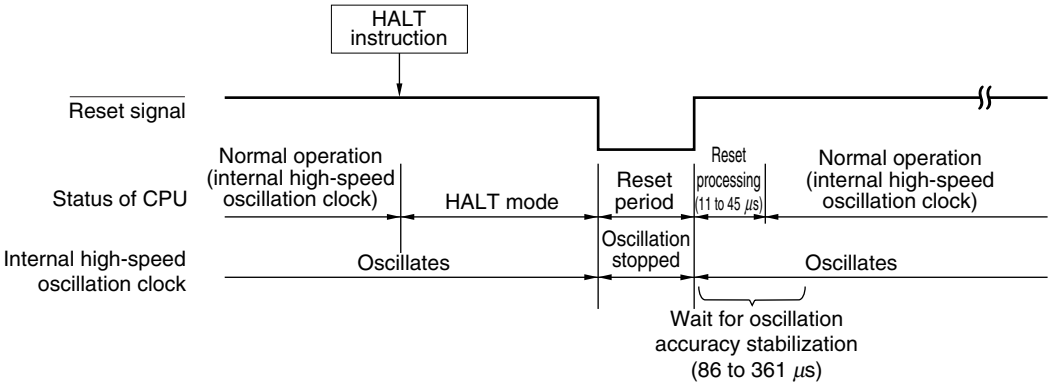
When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 22-4. HALT Mode Release by Reset

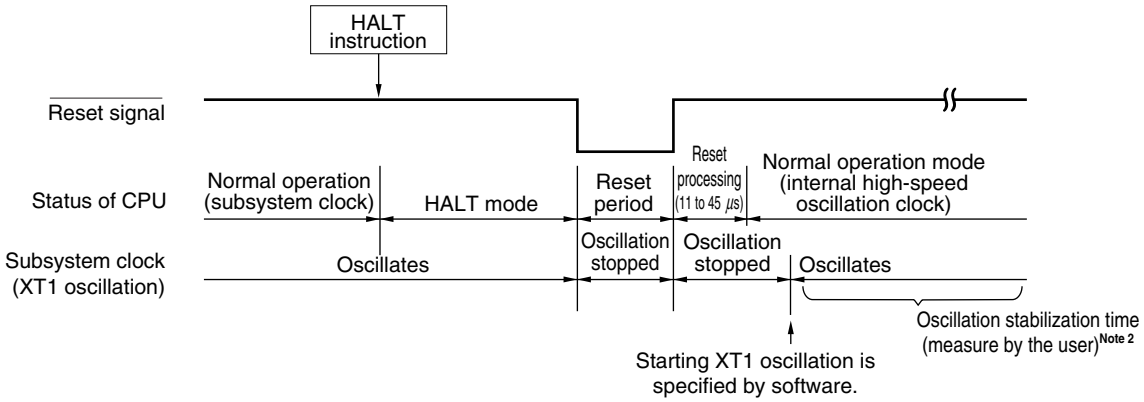
(1) When high-speed system clock is used as CPU clock



(2) When internal high-speed oscillation clock is used as CPU clock



(3) When subsystem clock is used as CPU clock[Note 1]



Notes 1. The 78K0/KB2 is not provided with a subsystem clock.

<R> **2.** Oscillation stabilization time is not required when using the external subsystem clock (f_{EXCLKS}) as the subsystem clock.

Remark fx: X1 clock oscillation frequency

Figure 25-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFBEH After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
LVIM	LVION	0	0	0	0	LVISEL	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVISEL[Note 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from external input pin (EXLVI)

LVIMD[Note 3]	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when operation is disabled • LVISEL = 1: Input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI}), or when operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI})

Notes 1. This bit is cleared to 00H upon a reset other than an LVI reset.

2. Bit 0 is read-only.

3. LVION, LVIMD, and LVISEL are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

4. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to wait for an operation stabilization time (10 μs (MIN.)) from when LVION is set to 1 until operation is stabilized. After operation has stabilized, the external input of 200 μs (MIN.) (Minimum pulse width: 200 μs (MIN.)) is required from when a state below LVI detection voltage has been entered, until LVIF is set (1).

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.