Renesas Electronics America Inc - UPD78F0500AMC-CAB-AX Datasheet

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Applications of "Embedded - Microcontrollers"

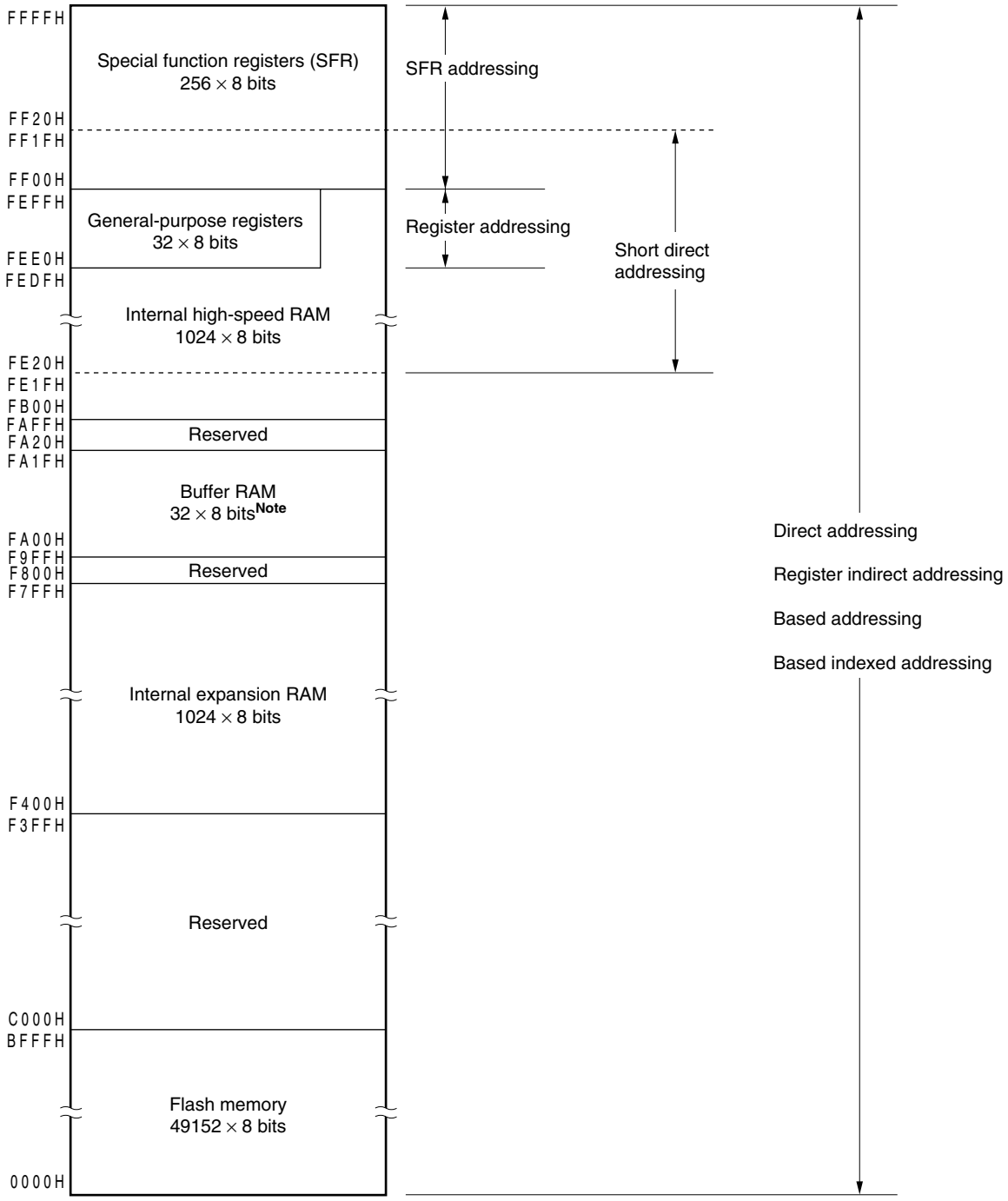
Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0500amc-cab-ax

(2) Non-port functions (2/2): 78K0/KD2

	Function Name	I/O	Function	After Reset	Alternate Function
	TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00
	TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P01/TO00
	TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50
	TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
	TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TI010
	TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50
	TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
	TOH0		8-bit timer H0 output		P15
	TOH1		8-bit timer H1 output		P16/INTP5
<R>	X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A[Note]
	X2	–			P122/EXCLK/OCD0B[Note]
	EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B[Note]
<R>	XT1	–	Connecting resonator for subsystem clock	Input port	P123
	XT2	–		Input port	P124/EXCLKS
	EXCLKS	Input	External clock input for subsystem clock	Input port	P124/XT2
	V_{DD}	–	Positive power supply for pins other than P20 to P27	–	–
<R>	AV_{REF}	–	A/D converter reference voltage input and positive power supply for P20 to P27 and A/D converter	–	–
	V_{SS}	–	Ground potential for pins other than P20 to P27	–	–
	AV_{SS}	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–
	OCD0A[Note]	Input	Connection for on-chip debug mode setting pins (μPD78F0527D and 78F0527DA only)	Input port	P121/X1
	OCD1A[Note]				P31/INTP2
	OCD0B[Note]	–			P122/X2/EXCLK
	OCD1B[Note]				P32/INTP3

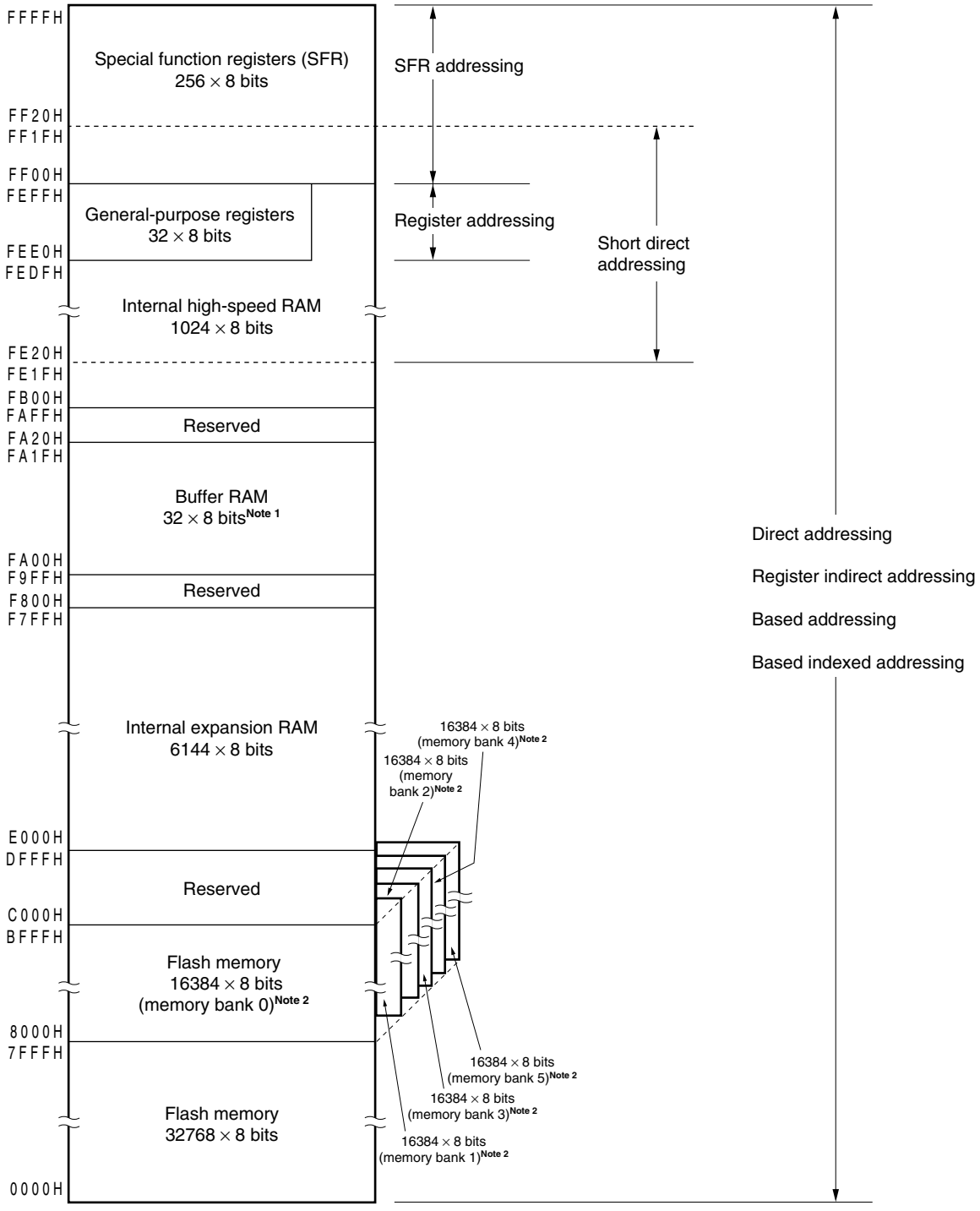
Note μPD78F0527D and 78F0527DA (product with on-chip debug function) only

Figure 3-16. Correspondence Between Data Memory and Addressing
(μPD78F0514, 78F0514A, 78F0524, 78F0524A, 78F0534, 78F0534A, 78F0544, and 78F0544A)



Note The buffer RAM is incorporated only in the μPD78F0544 and 78F0544A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0514, 78F0514A, 78F0524, 78F0524A, 78F0534, and 78F0534A.

Figure 3-19. Correspondence Between Data Memory and Addressing
(μPD78F0527, 78F0527A, 78F0537, 78F0537A, 78F0547, 78F0547A, 78F0527D, 78F0527DA, 78F0537D, 78F0537DA, 78F0547D and 78F0547DA)



Notes 1. The buffer RAM is incorporated only in the μPD78F0547, 78F0547A, 78F0547D and 78F0547DA (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0527, 78F0527A, 78F0537, 78F0537A, 78F0527D, 78F0527DA, 78F0537D and 78F0537DA.

2. To branch to or address a memory bank that is not set by the memory bank select register (BANK), change the setting of the memory bank by using BANK.

Table 3-8. Special Function Register List (4/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset	KB2	KC2	KD2	KE2	KF2
					1 Bit	8 Bits	16 Bits						
FFA5H	IIC shift register 0	IIC0		R/W	–	√	–	00H	√	√	√	√	√
FFA6H	IIC control register 0	IICC0		R/W	√	√	–	00H	√	√	√	√	√
FFA7H	Slave address register 0	SVA0		R/W	–	√	–	00H	√	√	√	√	√
FFA8H	IIC clock selection register 0	IICCL0		R/W	√	√	–	00H	√	√	√	√	√
FFA9H	IIC function expansion register 0	IICX0		R/W	√	√	–	00H	√	√	√	√	√
FFAAH	IIC status register 0	IICS0		R	√	√	–	00H	√	√	√	√	√
FFABH	IIC flag register 0	IICF0		R/W	√	√	–	00H	√	√	√	√	√
FFACH	Reset control flag register	RESF		R	–	√	–	00H Note 1	√	√	√	√	√
FFB0H FFB1H	16-bit timer counter 01	TM01		R	–	–	√	0000H	–	–	–	Note 2	√
FFB2H FFB3H	16-bit timer capture/compare register 001	CR001		R/W	–	–	√	0000H	–	–	–	Note 2	√
FFB4H FFB5H	16-bit timer capture/compare register 011	CR011		R/W	–	–	√	0000H	–	–	–	Note 2	√
FFB6H	16-bit timer mode control register 01	TMC01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFB7H	Prescaler mode register 01	PRM01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFB8H	Capture/compare control register 01	CRC01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFB9H	16-bit timer output control register 01	TOC01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFBAH	16-bit timer mode control register 00	TMC00		R/W	√	√	–	00H	√	√	√	√	√
FFBBH	Prescaler mode register 00	PRM00		R/W	√	√	–	00H	√	√	√	√	√
FFBCH	Capture/compare control register 00	CRC00		R/W	√	√	–	00H	√	√	√	√	√
FFBDH	16-bit timer output control register 00	TOC00		R/W	√	√	–	00H	√	√	√	√	√
FFBEH	Low-voltage detection register	LVIM		R/W	√	√	–	00H Note 3	√	√	√	√	√
FFBFH	Low-voltage detection level selection register	LVIS		R/W	√	√	–	00H Note 3	√	√	√	√	√
FFE0H	Interrupt request flag register 0L	IF0	IF0L	R/W	√	√	√	00H	√	√	√	√	√
FFE1H	Interrupt request flag register 0H		IF0H	R/W	√	√		00H	√	√	√	√	√
FFE2H	Interrupt request flag register 1L	IF1	IF1L	R/W	√	√	√	00H	√	√	√	√	√
FFE3H	Interrupt request flag register 1H		IF1H	R/W	√	√		00H	√	√	√	√	√
FFE4H	Interrupt mask flag register 0L	MK0	MK0L	R/W	√	√	√	FFH	√	√	√	√	√
FFE5H	Interrupt mask flag register 0H		MK0H	R/W	√	√		FFH	√	√	√	√	√
FFE6H	Interrupt mask flag register 1L	MK1	MK1L	R/W	√	√	√	FFH	√	√	√	√	√
FFE7H	Interrupt mask flag register 1H		MK1H	R/W	√	√		FFH	√	√	√	√	√

Notes 1. The reset value of RESF varies depending on the reset source.

2. This register is incorporated only in products whose flash memory is at least 48 KB.

3. The reset values of LVIM and LVIS vary depending on the reset source.

- Software example

```
RAMD      DSEG    SADDR
R_BNKA:   DS      2                          ; Secures RAM for specifying an address at the calling destination.
R_BNKN:   DS      1                          ; Secures RAM for specifying a memory bank number at the calling destination.
R_BNKRN:  DS      1                          ; Secures RAM for saving a memory bank number at the calling source.
RSAVEAX:  DS      2                          ; Secures RAM for saving the AX register.
-------------------------------------------------------------------------------------------------------------------
ETRC      CSEG    UNIT
ENTRY:
          MOV     R_BNKN,#BANKNUM  TEST      ; Store the memory bank number at the calling destination in RAM.
          MOVW    R_BNKA,#TEST               ; Stores the address at the calling destination in RAM.
          CALL    !BNKCAL                    ; Branches to an inter-memory bank calling processing routine.
                  :
                  :
-------------------------------------------------------------------------------------------------------------------
BNKC      CSEG    AT       7000H
BNKCAL:                                      ; Inter-memory bank calling processing routine
          MOVW    RSAVEAX,AX                 ; Saves the AX register.
          MOV     A,R_BNKN                   ; Acquires the memory bank number at the calling destination.
          XCH     A,BANK                     ; Changes the bank and acquires the memory bank number at the calling source.
          MOV     R_BNKRN,A                  ; Saves the memory bank number at the calling source to RAM.
          CALL    !BNKCALS                   ; Calls a subroutine to branch to the calling destination.

          MOVW    RSAVEAX,AX                 ; Saves the AX register.
          XCH     A,R_BNKRN                  ; Acquires the memory bank number at the calling source.
          MOV     BANK,A                     ; Specifies the memory bank number at the calling source.
          MOVW    AX,RSAVEAX                 ; Restores the AX register.
          RET                                ; Returns to the calling source.

BNKCALS:
          MOVW    AX,R_BNKA                  ; Specifies the address at the calling destination.
          PUSH    AX                         ; Sets the address at the calling destination to stack.
          MOVW    AX,RSAVEAX                 ; Restores source AX register.
          RET                                ; Branches to the calling destination.
-------------------------------------------------------------------------------------------------------------------
BN3       CSEG    BANK3
TEST:                                        ;
          MOV ···
              :
              :
          RET
END
```

Remark In the software example above, multiplexed processing is not supported.

Figure 5-36. Format of Port Register (78K0/KD2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	0	0	0	P03	P02	P01	P00	FF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P3	0	0	0	0	P33	P32	P31	P30	FF03H	00H (output latch)	R/W
P4	0	0	0	0	0	0	P41	P40	FF04H	00H (output latch)	R/W
P6	0	0	0	0	P63	P62	P61	P60	FF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FF07H	00H (output latch)	R/W
P12	0	0	0	P124Note	P123Note	P122Note	P121Note	P120	FF0CH	00H (output latch)	R/W
P13	0	0	0	0	0	0	0	P130	FF0DH	00H (output latch)	R/W
P14	0	0	0	0	0	0	0	P140	FF0EH	00H (output latch)	R/W

Pmn	m = 0 to 4, 6, 7, 12 to 14; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

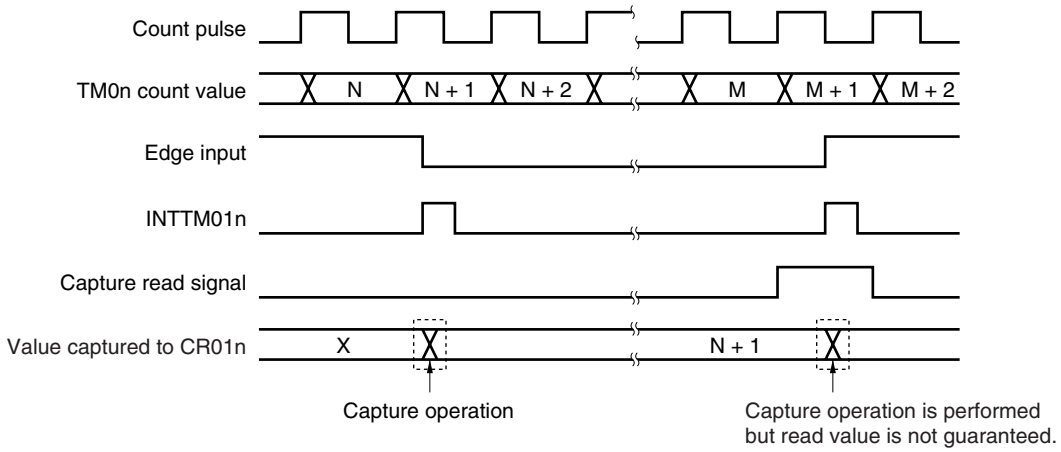
Note “0” is always read from the output latch of P121 to P124 if the pin is in the external clock input mode.

(4) Timing of holding data by capture register

(a) When the valid edge is input to the TI00n/TI01n pin and the reverse phase of the TI00n pin is detected while CR00n/CR01n is read, CR01n performs a capture operation but the read value of CR00n/CR01n is not guaranteed. At this time, an interrupt signal (INTTM00n/INTTM01n) is generated when the valid edge of the TI00n/TI01n pin is detected (the interrupt signal is not generated when the reverse-phase edge of the TI00n pin is detected).

When the count value is captured because the valid edge of the TI00n/TI01n pin was detected, read the value of CR00n/CR01n after INTTM00n/INTTM01n is generated.

Figure 7-61. Timing of Holding Data by Capture Register



(b) The values of CR00n and CR01n are not guaranteed after 16-bit timer/event counter 0n stops.

(5) Setting valid edge

Set the valid edge of the TI00n pin while the timer operation is stopped (TMC0n3 and TMC0n2 = 00). Set the valid edge by using ES0n0 and ES0n1.

(6) Re-triggering one-shot pulse

Make sure that the trigger is not generated while an active level is being output in the one-shot pulse output mode. Be sure to input the next trigger after the current active level is output.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

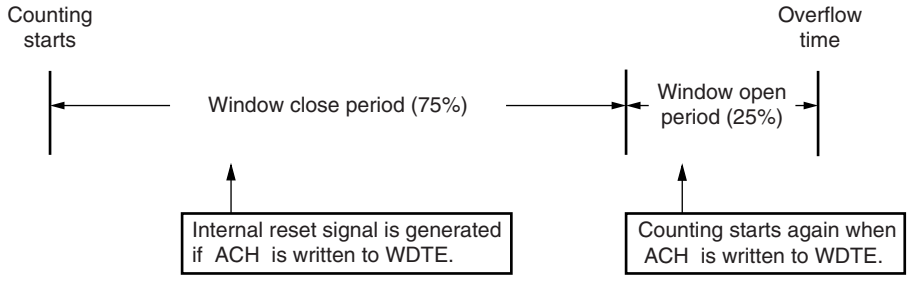
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

11.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (0080H). The outline of the window is as follows.

- If “ACH” is written to WDTE during the window open period, the watchdog timer is cleared and starts counting again.
- Even if “ACH” is written to WDTE during the window close period, an abnormality is detected and an internal reset signal is generated.

Example: If the window open period is 25%



Caution The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.

The window open period to be set is as follows.

Table 11-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	25%
0	1	50%
1	0	75%
1	1	100%

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. Setting WINDOW1 = WINDOW0 = 0 is prohibited when using the watchdog timer at 1.8 V ≤ V_{DD} < 2.7 V.

3. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

CHAPTER 17 SERIAL INTERFACE CSIA0

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2
Serial interface CSIA0	–				√

Remark √: Mounted, –: Not mounted

17.1 Functions of Serial Interface CSIA0

Serial interface CSIA0 has the following three modes.

(1) Operation stop mode

This mode is used when serial communication is not performed and can enable a reduction in the power consumption.

For details, see **17.4.1 Operation stop mode**.

(2) 3-wire serial I/O mode (MSB/LSB-first selectable)

This mode is to communicate data successively in 8-bit units, by using three lines: serial clock ($\overline{\text{SCKA0}}$) and serial data (SIA0 and SOA0) lines.

The processing time of data communication can be shortened in the 3-wire serial I/O mode because transmission and reception can be simultaneously executed.

In addition, whether 8-bit data is communicated MSB or LSB first can be specified, so this interface can be connected to any device.

For details, see **17.4.2 3-wire serial I/O mode**.

(3) 3-wire serial I/O mode with automatic transmit/receive function (MSB/LSB-first selectable)

This mode is used to communicate data continuously in 8-bit units using three lines: a serial clock line ($\overline{\text{SCKA0}}$) and two serial data lines (SIA0 and SOA0).

The processing time of data communication can be shortened in the 3-wire serial I/O mode with automatic transmit/receive function because transmission and reception can be simultaneously executed.

In addition, whether 8-bit data is communicated MSB or LSB first can be specified, so this interface can be connected to any device.

Data can be communicated to/from a display driver etc. without using software since a 32-byte transfer buffer RAM is incorporated. Also, the incorporation of handshake pins (STB0, BUSY0) used in the master mode has made connection to peripheral ICs easy.

For details, see **17.4.3 3-wire serial I/O mode with automatic transmit/receive function**.

Figure 17-3. Format of Serial Status Register 0 (CSIS0) (2/2)

BUSYE0	Busy signal detection enable/disable
0	Busy signal detection disabled (input via BUSY0 pin is ignored)
1	Busy signal detection enabled and communication wait by busy signal is executed

BUSYLV0Note 1	Busy signal active level setting
0	Low level
1	High level

ERRE0Note 2	Bit error detection enable/disable
0	Error detection disabled
1	Error detection enabled

ERRF0	Bit error detection flag
0	• Bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) = 0 • At reset input • When communication is started by setting bit 0 (ATSTA0) of serial trigger register 0 (CSIT0) to 1 or writing to SIOA0.
1	Bit error detected (when ERRE0 = 1, the level specified by BUSYLV0 during the data bit transfer period is detected via BUSY0 pin input).

TSF0	Transfer status detection flag
0	• Bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) = 0 • At reset input • At the end of the specified transfer • When transfer is stopped by setting bit 1 (ATSTP0) of serial trigger register 0 (CSIT0) to 1
1	From the transfer start to the end of the specified transfer

Notes 1. In bit error detection by busy input, the active level specified by BUSYLV0 is detected.

2. The ERRE0 setting is valid even when BUSYE0 = 0.

Caution During transfer (TSF0 = 1), rewriting serial operation mode specification register 0 (CSIMA0), serial status register 0 (CSIS0), divisor selection register 0 (BRGCA0), automatic data transfer address point specification register 0 (ADTP0), automatic data transfer interval specification register 0 (ADTI0), and serial I/O shift register 0 (SIOA0) are prohibited. However, these registers can be read and re-written to the same value. In addition, the buffer RAM can be rewritten during transfer.

(4) Synchronization control

Busy control and strobe control are functions used to synchronize transmission/reception between the master device and a slave device.

By using these functions, a shift in bits being transmitted or received can be detected.

(a) Busy control option

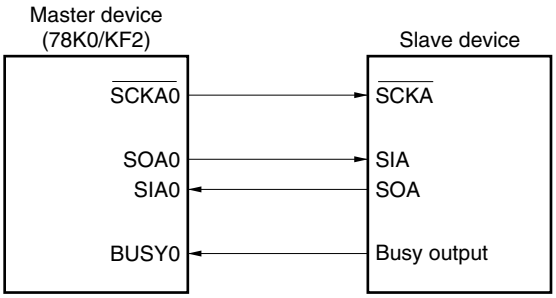
Busy control is a function to keep the serial transmission/reception by the master device waiting while the busy signal output by a slave device to the master is active.

When using this busy control option, the following conditions must be satisfied.

- Bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) is set to 1.
- Bit 4 (BUSYE0) of serial status register 0 (CSIS0) is set to 1.

Figure 17-23 shows the system configuration of the master device and slave device when the busy control option is used.

Figure 17-23. System Configuration When Busy Control Option Is Used



The master device inputs the busy signal output by the slave device to the BUSY0/BUZ/INTP7/P141 pin. The master device samples the input busy signal in synchronization with the falling of the serial clock. Even if the busy signal becomes active while 8-bit data is being transmitted or received, transmission/reception by the master is not kept waiting. If the busy signal is active at the rising edge of the serial clock one clock after completion of transmission/reception of the 8-bit data, the busy input becomes valid. After that, the master transmission/reception is kept waiting while the busy signal is active.

The active level of the busy signal is set by bit 3 (BUSYLV0) of CSIS0.

BUSYLV0 = 1: Active-high
BUSYLV0 = 0: Active-low

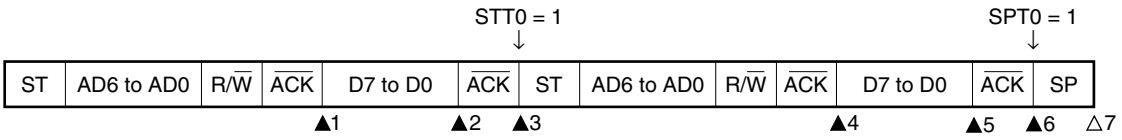
When using the busy control option, select the master mode. Control with the busy signal cannot be implemented in the slave mode.

Figure 17-24 shows the example of the operation timing when the busy control option is used.

Caution Busy control cannot be used simultaneously with the interval time control function of automatic data transfer interval specification register 0 (ADTI0).

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

(i) When WTIM0 = 0

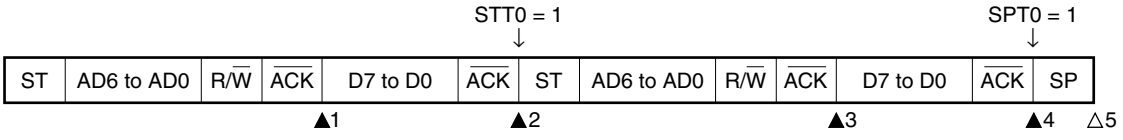


▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000×000B (Sets WTIM0 to 1[Note 1])
▲3: IICS0 = 1000××00B (Clears WTIM0 to 0[Note 2], sets STT0 to 1)
▲4: IICS0 = 1000×110B
▲5: IICS0 = 1000×000B (Sets WTIM0 to 1[Note 3])
▲6: IICS0 = 1000××00B (Sets SPT0 to 1)
△7: IICS0 = 00000001B

Notes 1. To generate a start condition, set WTIM0 to 1 and change the timing for generating the INTIIC0 interrupt request signal.
2. Clear WTIM0 to 0 to restore the original setting.
3. To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIIC0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000××00B (Sets STT0 to 1)
▲3: IICS0 = 1000×110B
▲4: IICS0 = 1000××00B (Sets SPT0 to 1)
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 20-4. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KD2)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	DUALIF0 CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	0	PIF6	WTIF	KRIF	TMIF51	WTIIF	SRIF0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
IF1H	0	0	0	0	0	0	0	IICIF0 DMUIF Note

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Note Products whose flash memory is at least 48 KB only.

Caution Be sure to clear bit 7 of 1F1L and bits 1 to 7 of IF1H to 0.

Figure 20-15. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KE2)

Address: FFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	DUALPR0 CSIPR10 STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR1L	PPR7	PPR6	WTPR	KRPR	TMPR51	WTIPR	SRPR0	ADPR

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR1H	1	1	1	1	TMPR011 Note	TMPR001 Note	CSIPR11 Note	IICPR0 DMUPR Note

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Note Products whose flash memory is at least 48 KB only.

Caution Be sure to set bits 1 to 7 of PR1H to 1 for the products whose flash memory is less than 32 KB. Be sure to set bits 4 to 7 of PR1H to 1 for the products whose flash memory is at least 48 KB.

CHAPTER 23 RESET FUNCTION

The reset function is mounted onto all 78K0/Kx2 microcontroller products.

The following four operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage and detection voltage of low-power-supply detector (LVI)

External and internal resets have no functional differences. In both cases, program execution starts at the address at 0000H and 0001H when the reset signal is generated.

A reset is applied when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Tables 23-1 and 23-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release, except for P130, which is low-level output.

When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (see **Figures 23-2** to **23-4**) after reset processing. Reset by POC and LVI circuit power supply detection is automatically released when $V_{DD} \geq V_{POC}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (see **CHAPTER 24 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 25 LOW-VOLTAGE DETECTOR**) after reset processing.

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.

2. During reset signal generation, the X1 clock, XT1 clock[Note 1], internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input and external subsystem clock[Note 1] input become invalid.

3. When the STOP mode is released by a reset, the STOP mode contents are held during reset input. However, the port pins become high-impedance, except for P130[Note 2], which is set to low-level output.

Notes 1. The 78K0/KB2 is not provided with XT1 clock and external subsystem clock.

2. P130 pin is not mounted onto 38-pin and 44-pin products of the 78K0/KC2 and 78K0/KB2.

CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD and 78F05xxDA ONLY)

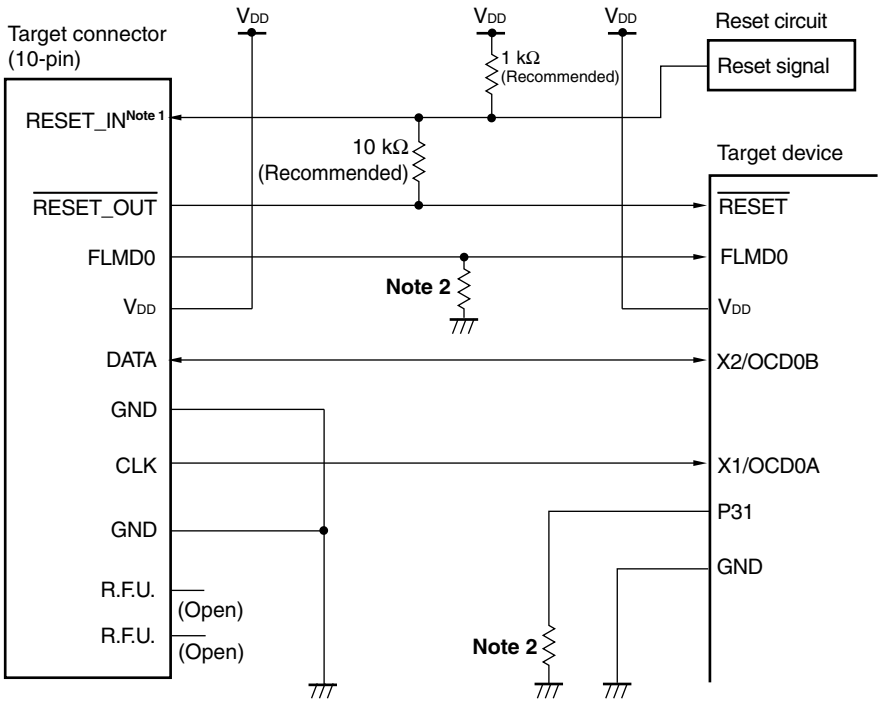
28.1 Connecting QB-MINI2 to μPD78F05xxD and 78F05xxDA

The μPD78F05xxD and 78F05xxDA use the V_{DD}, FLMD0, $\overline{\text{RESET}}$, OCD0A/X1 (or OCD1A/P31), OCD0B/X2 (or OCD1B/P32), and V_{SS} pins to communicate with the host machine via an on-chip debug emulator (QB-MINI2). Whether OCD0A/X1 and OCD1A/P31, or OCD0B/X2 and OCD1B/P32 are used can be selected.

Caution The μPD78F05xxD and 78F05xxDA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Remark μPD78F05xxD: μPD78F0503D, 78F0513D, 78F0515D, 78F0527D, 78F0537D, 78F0547D
μPD78F05xxDA: μPD78F0503DA, 78F0513DA, 78F0515DA, 78F0527DA, 78F0537DA, 78F0547DA

Figure 28-1. Connection Example of QB-MINI2 and μPD78F05xxD and 78F05xxDA (When OCD0A/X1 and OCD0B/X2 Are Used)



Notes 1. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **QB-MINI2 User's Manual (U18371E)**.

2. Make pull-down resistor 470 Ω or more (10 kΩ: recommended).

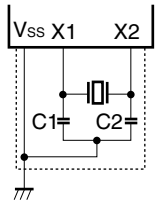
Cautions 1. Input the clock from the OCD0A/X1 pin during on-chip debugging.

2. Control the OCD0A/X1 and OCD0B/X2 pins by externally pulling down the OCD1A/P31 pin or by using an external circuit using the P130 pin (that outputs a low level when the device is reset).

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

X1 Oscillator Characteristics

(T_A = –40 to +110°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
Ceramic resonator, Crystal resonator		X1 clock oscillation frequency (f_X)Note 1	Conventional-specification Products (μPD78F05xx (A2))	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0Note 2		20.0	MHz
				2.7 V ≤ V_{DD} < 4.0 V	1.0Note 2		10.0	
			Expanded-specification Products (μPD78F05xxA(A2))		1.0Note 2		20.0	MHz

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

A/D Converter Characteristics

(T_A = –40 to +125°C, 2.7 V ≤ AV_{REF} ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}					10	bit
Overall error[Notes 1, 2]	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V				±0.6	%FSR
Conversion time	t_{CONV}	Conventional-specification Products (μPD78F05xx(A2))	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		36.7	μs
			2.7 V ≤ AV_{REF} < 4.0 V	12.2		36.7	μs
		Expanded-specification Products (μPD78F05xxA (A2))	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		66.6	μs
			2.7 V ≤ AV_{REF} < 4.0 V	12.2		66.6	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V				±0.6	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V				±0.6	%FSR
Integral non-linearity error[Note 1]	I_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V				±4.5	LSB
Differential non-linearity error[Note 1]	D_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V				±2.0	LSB
Analog input voltage	V_{AIN}			AV_{SS}		AV_{REF}	V

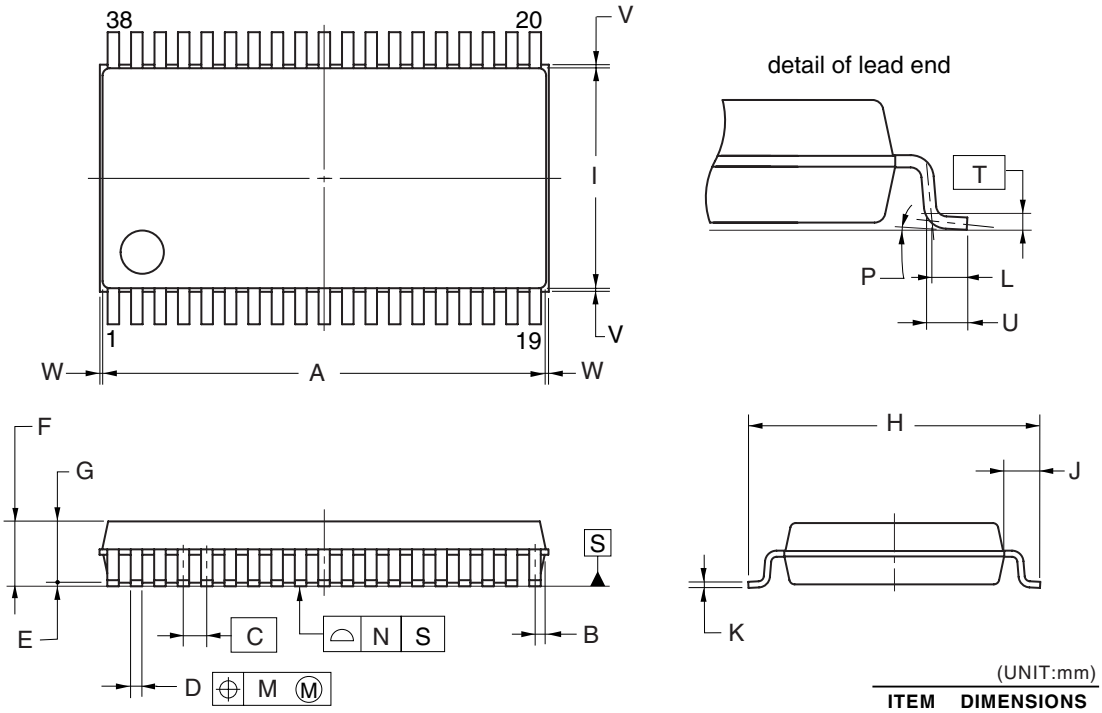
Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

34.2 78K0/KC2

- μPD78F0511AMC-GAA-AX, 78F0512AMC-GAA-AX, 78F0513AMC-GAA-AX, 78F0513DAMC-GAA-AX
- μPD78F0511AMCA-GAA-G, 78F0512AMCA-GAA-G, 78F0513AMCA-GAA-G
- μPD78F0511AMCA2-GAA-G, 78F0512AMCA2-GAA-G, 78F0513AMCA2-GAA-G

38-PIN PLASTIC SSOP (7.62mm (300))



(UNIT:mm)

ITEM	DIMENSIONS
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	$0.30^{+0.10}_{-0.05}$
E	0.125±0.075
F	2.00 MAX.
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.10}_{-0.05}$
L	0.50
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P38MC-65-GAA

NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

(15/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 14	Soft	Serial interface UART0	UART mode	If clock supply to serial interface UART0 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART0 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD0 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER0 = 0, RXE0 = 0, and TXE0 = 0.	p. 432 ☐
				Set POWER0 = 1 and then set TXE0 = 1 (transmission) or RXE0 = 1 (reception) to start communication.	p. 432 ☐
				TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.	p. 432 ☐
				Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.	pp. 432, 435 ☐
			TXS0: Transmit shift register 0	Do not write the next transmit data to TXS0 before the transmission completion interrupt signal (INTST0) is generated.	p. 435 ☐
			ASIM0: Asynchronous serial interface operation mode register 0	To start the transmission, set POWER0 to 1 and then set TXE0 to 1. To stop the transmission, clear TXE0 to 0, and then clear POWER0 to 0.	p. 437 ☐
				To start the reception, set POWER0 to 1 and then set RXE0 to 1. To stop the reception, clear RXE0 to 0, and then clear POWER0 to 0.	p. 437 ☐
				Set POWER0 to 1 and then set RXE0 to 1 while a high level is input to the RxD0 pin. If POWER0 is set to 1 and RXE0 is set to 1 while a low level is input, reception is started.	p. 437 ☐
				TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.	p. 437 ☐
				Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.	p. 437 ☐
				Clear the TXE0 and RXE0 bits to 0 before rewriting the PS01, PS00, and CL0 bits.	p. 437 ☐
				Make sure that TXE0 = 0 when rewriting the SL0 bit. Reception is always performed with “number of stop bits = 1”, and therefore, is not affected by the set value of the SL0 bit.	p. 437 ☐
				Be sure to set bit 0 to 1.	p. 437 ☐
			ASIS0: Asynchronous serial interface reception error status register 0	The operation of the PE0 bit differs depending on the set values of the PS01 and PS00 bits of asynchronous serial interface operation mode register 0 (ASIM0)	p. 438 ☐
				Only the first bit of the receive data is checked as the stop bit, regardless of the number of stop bits.	p. 438 ☐
				If an overrun error occurs, the next receive data is not written to receive buffer register 0 (RXB0) but discarded.	p. 438 ☐
				If data is read from ASIS0, a wait cycle is generated. Do not read data from ASIS0 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.	p. 438 ☐
			BRGC0: Baud rate generator control register 0	Make sure that bit 6 (TXE0) and bit 5 (RXE0) of the ASIM0 register = 0 when rewriting the MDL04 to MDL00 bits.	p. 440 ☐
				Make sure that bit 7 (POWER0) of the ASIM0 register = 0 when rewriting the TPS01 and TPS00 bits.	p. 440 ☐
	Hard			The baud rate value is the output clock of the 5-bit counter divided by 2.	p. 440 ☐