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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Last Time Buy |
| Core Processor | 78K/0 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | 3-Wire SIO, I²C, LINbus, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 30-LSSOP (0.240", 6.10mm Width) |
| Supplier Device Package | 30-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0500mc-5a4-a |

**(1) Conventional-specification products (μPD78F05xx and 78F05xxD) (2/3)**

**<3> When high-speed system clock (X1 oscillation or external clock input) is used and entry RAM is located outside short direct addressing range**

| Library Name | | Processing Time (μs) | | | |
|---|---|---|---|---|---|
| | | Normal Model of C Compiler | | Static Model of C Compiler/Assembler | |
| | | Min. | Max. | Min. | Max. |
| Self programming start library | | 34/$f_{CPU}$ | | | |
| Initialize library | | 49/$f_{CPU}$ + 485.8125 | | | |
| Mode check library | | 35/$f_{CPU}$ + 374.75 | | 29/$f_{CPU}$ + 374.75 | |
| Block blank check library | | 174/$f_{CPU}$ + 6382.0625 | | 134/$f_{CPU}$ + 6382.0625 | |
| Block erase library | | 174/$f_{CPU}$ + 31093.875 | 174/$f_{CPU}$ + 298948.125 | 134/$f_{CPU}$ + 31093.875 | 134/$f_{CPU}$ + 298948.125 |
| Word write library | | 318 (321)/$f_{CPU}$ + 644.125 | 318 (321)/$f_{CPU}$ + 1491.625 | 262 (265)/$f_{CPU}$ + 644.125 | 262 (265)/$f_{CPU}$ + 1491.625 |
| Block verify library | | 174/$f_{CPU}$ + 13448.5625 | | 134/$f_{CPU}$ + 13448.5625 | |
| Self programming end library | | 34/$f_{CPU}$ | | | |
| Get information library | Option value: 03H | 171 (172 )/$f_{CPU}$ + 432.4375 | | 129 (130)/$f_{CPU}$ + 432.4375 | |
| | Option value: 04H | 181 (182)/$f_{CPU}$ + 427.875 | | 139 (140)/$f_{CPU}$ + 427.875 | |
| | Option value: 05H | 404 (411)/$f_{CPU}$ + 496.125 | | 362 (369)/$f_{CPU}$ + 496.125 | |
| Set information library | | 75/$f_{CPU}$ + 79157.6875 | 75/$f_{CPU}$ + 652400 | 67$f_{CPU}$ + 79157.6875 | 67$f_{CPU}$ + 652400 |
| EEPROM write library | | 318 (321)/$f_{CPU}$ + 799.875 | 318 (321)/$f_{CPU}$ + 1647.375 | 262 (265)/$f_{CPU}$ + 799.875 | 262 (265)/$f_{CPU}$ + 1647.375 |

**Remarks 1.** Values in parentheses indicate values when a write start address structure is located other than in the internal high-speed RAM.

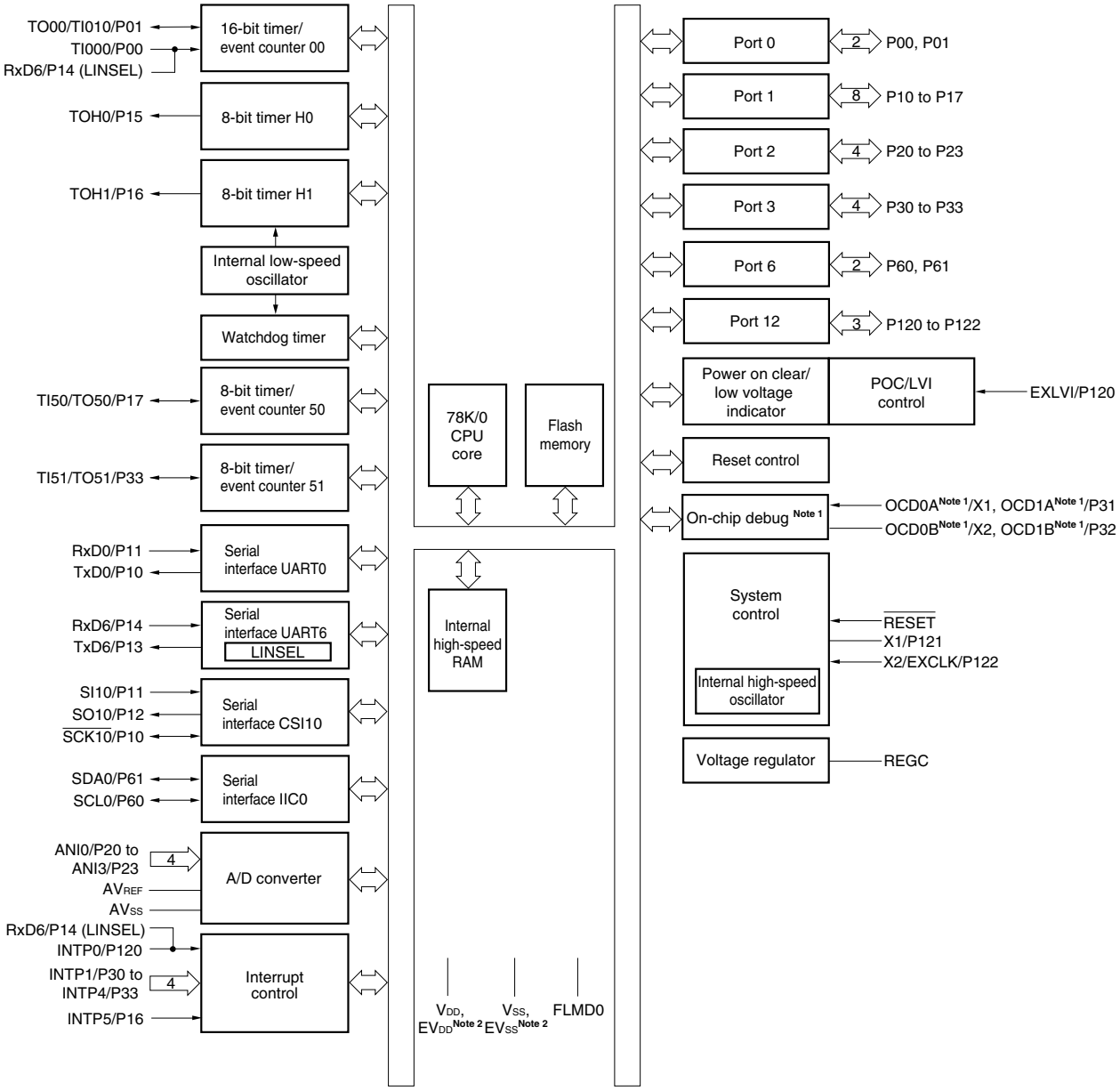
**2.** The above processing times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

**3.** $f_{CPU}$: CPU operation clock frequency

**4.** RSTS: Bit 7 of the internal oscillation mode register (RCM)

## 1.7 Block Diagram

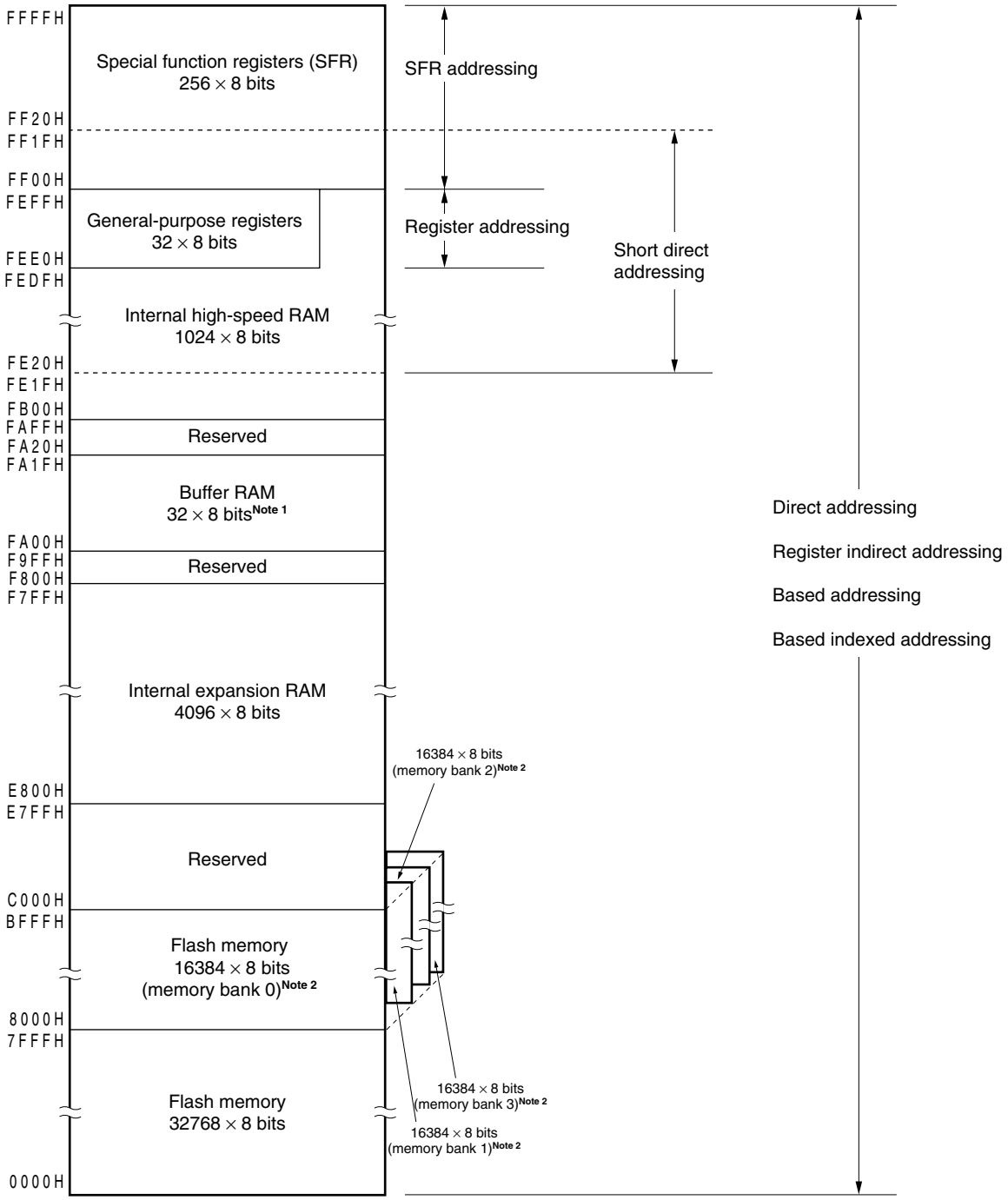
### 1.7.1 78K0/KB2




**Notes 1.** Available only in the products with on-chip debug function.

**2.** Available only in the 36-pin products.

**Figure 3-18. Correspondence Between Data Memory and Addressing (μPD78F0526, 78F0526A, 78F0536, 78F0536A, 78F0546, and 78F0546A)**

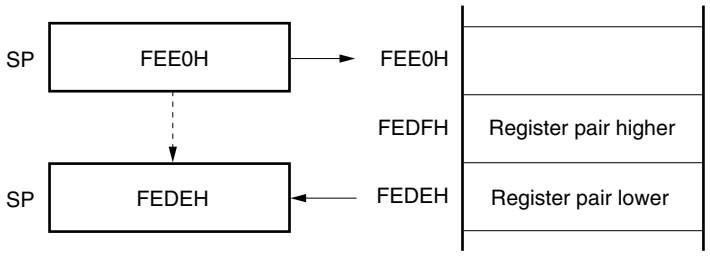



**Notes 1.** The buffer RAM is incorporated only in the μPD78F0546 and 78F0546A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0526, 78F0526A, 78F0536 and 78F0536A.

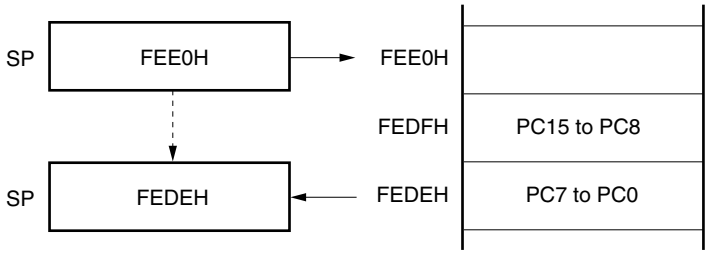
**2.** To branch to or address a memory bank that is not set by the memory bank select register (BANK), change the setting of the memory bank by using BANK.

**Figure 3-23. Data to Be Saved to Stack Memory**

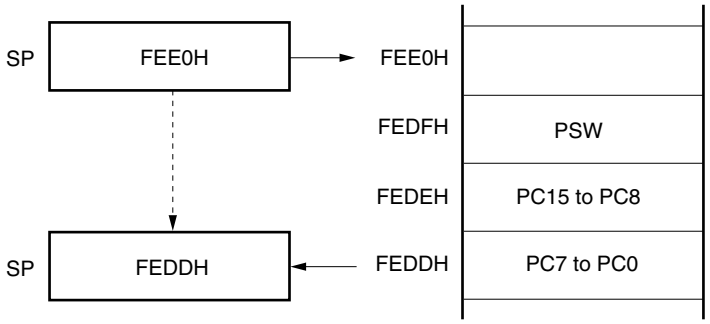
**(a) PUSH rp instruction (when SP = FEE0H)**




**(b) CALL, CALLF, CALLT instructions (when SP = FEE0H)**




**(c) Interrupt, BRK instructions (when SP = FEE0H)**



### 3.4.2 Register addressing

**[Function]**

The general-purpose register to be specified is accessed as an operand with the register bank select flags (RBS0 to RBS1) and the register specify codes of an operation code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the operation code.

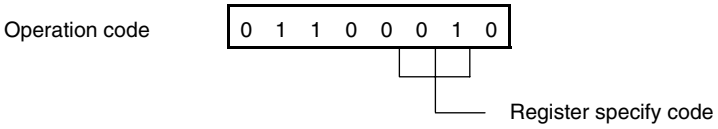
**[Operand format]**

| Identifier | Description |
|---|---|
| r | X, A, C, B, E, D, L, H |
| rp | AX, BC, DE, HL |

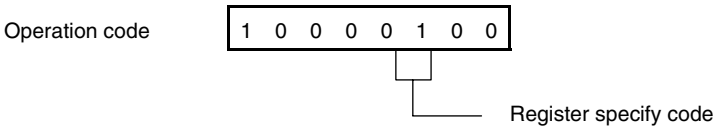
'r' and 'rp' can be described by absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

**[Description example]**

MOV A, C; when selecting C register as r




INCW DE; when selecting DE register pair as rp



**(b) To stop X1 oscillation (disabling external clock input) by setting MSTOP to 1**

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the high-speed system clock. When CLS = 0 and MCS = 1, the high-speed system clock is supplied to the CPU, so change the CPU clock to a clock other than the high-speed system clock.

- 78K0/KB2

| MCS | CPU Clock Status |
|---|---|
| 0 | Internal high-speed oscillation clock |
| 1 | High-speed system clock |

- 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2

| CLS | MCS | CPU Clock Status |
|---|---|---|
| 0 | 0 | Internal high-speed oscillation clock |
| 0 | 1 | High-speed system clock |
| 1 | × | Subsystem clock |

<2> Stopping the high-speed system clock (MOC register)

When MSTOP is set to 1, X1 oscillation is stopped (the input of the external clock is disabled).

**Caution Be sure to confirm that MCS = 0 or CLS = 1 when setting MSTOP to 1. In addition, stop peripheral hardware that is operating on the high-speed system clock.**

### 6.6.2 Example of controlling internal high-speed oscillation clock

The following describes examples of clock setting procedures for the following cases.

(1) When restarting oscillation of the internal high-speed oscillation clock
(2) When using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock
(3) When stopping the internal high-speed oscillation clock

**(3) Port mode registers 1 and 3 (PM1, PM3)**

These registers set port 1 and 3 input/output in 1-bit units.

When using the P17/TO50/TI50 and P33/TO51/TI51/INTP4 pins for timer output, clear PM17 and PM33 and the output latches of P17 and P33 to 0.

When using the P17/TO50/TI50 and P33/TO51/TI51/INTP4 pins for timer input, set PM17 and PM33 to 1. The output latches of P17 and P33 at this time may be 0 or 1.

PM1 and PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Figure 8-9. Format of Port Mode Register 1 (PM1)**

Address: FF21H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM1 | PM17 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 |

| PM1n | P1n pin I/O mode selection (n = 0 to 7) |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

**Figure 8-10. Format of Port Mode Register 3 (PM3)**

Address: FF23H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM3 | 1 | 1 | 1 | 1 | PM33 | PM32 | PM31 | PM30 |

| PM3n | P3n pin I/O mode selection (n = 0 to 3) |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

## 12.4 Operations of Clock Output/Buzzer Output Controller

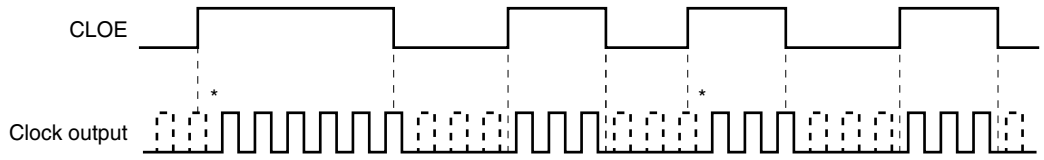
### 12.4.1 Operation as clock output

The clock pulse is output as the following procedure.

<1> Select the clock pulse output frequency with bits 0 to 3 (CCS0 to CCS3) of the clock output selection register (CKS) (clock pulse output in disabled status).
<2> Set bit 4 (CLOE) of CKS to 1 to enable clock output.

**Remark** The clock output controller is designed not to output pulses with a small width during output enable/disable switching of the clock output. As shown in Figure 12-6, be sure to start output from the low period of the clock (marked with * in the figure). When stopping output, do so after the high-level period of the clock.

**Figure 12-6. Remote Control Output Application Example**

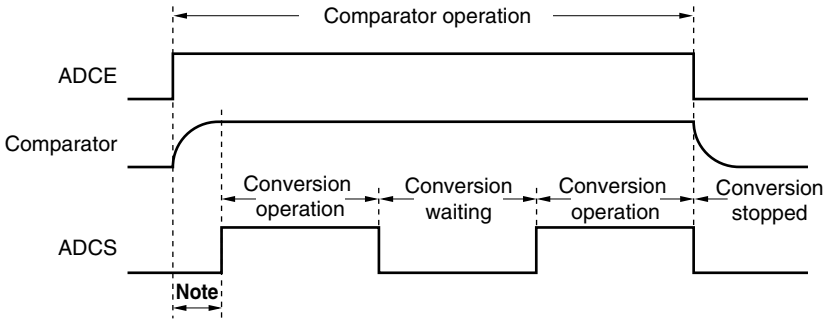



### 12.4.2 Operation as buzzer output

The buzzer frequency is output as the following procedure.

<1> Select the buzzer output frequency with bits 5 and 6 (BCS0, BCS1) of the clock output selection register (CKS) (buzzer output in disabled status).
<2> Set bit 7 (BZOE) of CKS to 1 to enable buzzer output.

**Figure 13-4. Timing Chart When Comparator Is Used**




**Note** To stabilize the internal circuit, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 $\mu$s or longer.

**Cautions 1. A/D conversion must be stopped before rewriting bits FR0 to FR2, LV1, and LV0 to values other than the identical data.**

**2. If data is written to ADM, a wait cycle is generated. Do not write data to ADM when the peripheral hardware clock ($f_{PRS}$) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.**

The setting methods are described below.

<1> Set bit 0 (ADCE) of the A/D converter mode register (ADM) to 1.
<2> Set the channel to be used in the analog input mode by using bits 3 to 0 (ADPC3 to ADPC0) of the A/D port configuration register (ADPC) and bits 7 to 0 (PM27 to PM20) of port mode register 2 (PM2).
<3> Select conversion time by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of ADM.
<4> Select a channel to be used by using bits 2 to 0 (ADS2 to ADS0) of the analog input channel specification register (ADS).
<5> Set bit 7 (ADCS) of ADM to 1 to start A/D conversion.
<6> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<7> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Change the channel>

<8> Change the channel using bits 2 to 0 (ADS2 to ADS0) of ADS to start A/D conversion.
<9> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<10> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Complete A/D conversion>

<11> Clear ADCS to 0.
<12> Clear ADCE to 0.

**Cautions 1. Make sure the period of <1> to <5> is 1 μs or more.**
**2. <1> may be done between <2> and <4>.**
**3. <1> can be omitted. However, ignore data of the first conversion after <5> in this case.**
**4. The period from <6> to <9> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM. The period from <8> to <9> is the conversion time set using FR2 to FR0, LV1, and LV0.**

**(7) Automatic data transfer address count register 0 (ADTC0)**

This is a register used to indicate buffer RAM addresses during automatic transfer. When automatic transfer is stopped, the data position when transfer stopped can be ascertained by reading ADTC0 register value.

This register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H. However, reading from ADTC0 is prohibited when bit 0 (TSF0) of serial status register 0 (CSIS0) = 1.

**Figure 17-8. Format of Automatic Data Transfer Address Count Register 0 (ADTC0)**

Address: FF97H After reset: 00H R

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADTC0 | 0 | 0 | 0 | ADTC04 | ADTC03 | ADTC02 | ADTC01 | ADTP00 |

**(8) Port mode register 14 (PM14)**

This register sets port 14 input/output in 1-bit units.

When using P142/$\overline{\text{SCKA0}}$ pin as the clock output of the serial interface, clear PM142 to 0 and set the output latch of P142 to 1.

When using P144/SOA0 and P145/STB0 pins as the data output or strobe output of the serial interface, clear PM144, PM145, and the output latches of P144 and P145 to 0.

When using P141/BUSY0, P142/$\overline{\text{SCKA0}}$, and P143/SIA0 pins as the busy input, clock input, or data input of the serial interface, set PM141, PM142, and PM143 to 1. At this time, the output latches of P141, P142, and P143 may be 0 or 1.

PM14 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

**Figure 17-9. Format of Port Mode Register 14 (PM14)**

Address: FF2EH After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM14 | 1 | 1 | PM145 | PM144 | PM143 | PM142 | PM141 | PM140 |

| PM14n | P14n pin I/O mode selection (n = 0 to 5) |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

**(2) Automatic transmit/receive data setting**

Here is an example of the procedure for successively transmitting/receiving data as the master.

<1> Enable CSIA0 to operate by setting bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) to 1 (the buffer RAM can now be accessed).
<2> Select a serial clock by using serial status register 0 (CSIS0).
<3> Set the division ratio of the serial clock by using division value selection register 0 (BRGCA0), and specify a communication rate.
<4> Sequentially write data to be transmitted to the buffer RAM, starting from the least significant address FA00H, up to FA1FH. Data is transmitted from the lowest address, continuing on to higher addresses.
<5> Set "number of data items to be transmitted − 1" to automatic data transfer address point specification register 0 (ADTP0).
<6> Set bits 6 (ATE0) and 4 (MASTER0) of CSIMA0 to select a master operation in the automatic communication mode.
<7> Set bits 3 (TXEA0) and 2 (RXEA0) of CSIMA0 to 1 to enable transmission/reception.
<8> Set the transmission interval of data to the automatic data transfer interval specification register (ADTI0).
<9> Automatic transmit/receive processing is started when bit 0 (ATSTA0) of serial trigger register 0 (CSIT0) is set to 1.

**Caution Take the relationship with the other communicating party into consideration when setting the port mode register and port register.**

Operations <1> to <9> execute the following operation.

- After the buffer RAM data indicated by automatic data transfer address count register 0 (ADTC0) is transferred to SIOA0, transmission is carried out (start of automatic transmission/reception).
- The received data is written to the buffer RAM address indicated by ADTC0.
- ADTC0 is incremented and the next data transmission/reception is carried out. Data transmission/reception continues until the ADTC0 incremental output matches the set value of automatic data transfer address point specification register 0 (ADTP0) (end of automatic transmission/reception). However, if bit 5 (ATM0) of CSIMA0 is set to 1 (repeat mode), ADTC0 is cleared after a match between ADTP0 and ADTC0, and then repeated transmission/reception is started.
- When automatic transmission/reception is terminated, an interrupt request (INTACSI) is generated and bit 0 (TSF0) of CSIS0 is cleared.
- To continue transmitting the next data, set the new data to the buffer RAM, and set "number of data to be transmitted − 1" to ADTP0. After setting the number of data, set ATSTA0 to 1.

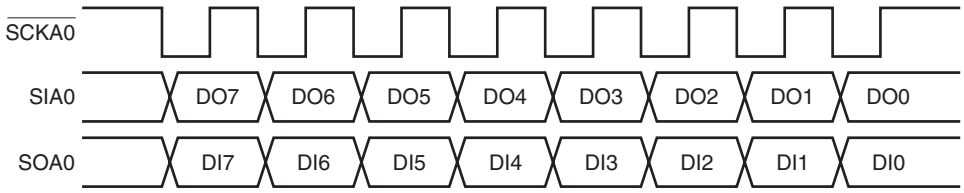
**(d) Data format**

Data is changed in synchronization with the $\overline{\text{SCKA0}}$ falling edge as shown below.

The data length is fixed to 8 bits and the data transfer direction can be switched by the specification of bit 1 (DIR0) of serial operation mode specification register 0 (CSIMA0).

**Figure 17-21. Format of CSIA0 Transmit/Receive Data**

**(a) MSB-first (DIR0 bit = 0)**




**(b) LSB-first (DIR0 bit = 1)**

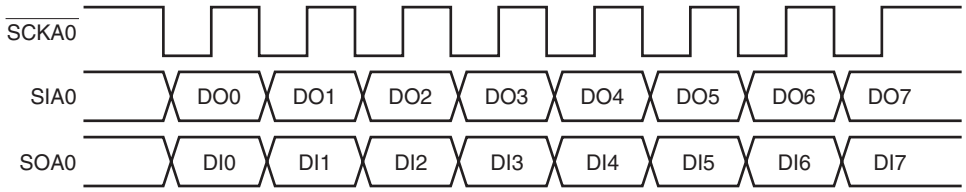


**Figure 18-6. Format of IIC Status Register 0 (IICS0) (2/3)**

| COI0 | Detection of matching addresses |
|---|---|
| 0 | Addresses do not match. |
| 1 | Addresses match. |

| Condition for clearing (COI0 = 0) | Condition for setting (COI0 = 1) |
|---|---|
| • When a start condition is detected<br>• When a stop condition is detected<br>• Cleared by LREL0 = 1 (exit from communications)<br>• When IICE0 changes from 1 to 0 (operation stop)<br>• Reset | • When the received address matches the local address (slave address register 0 (SVA0))<br>(set at the rising edge of the eighth clock). |

| TRC0 | Detection of transmit/receive status |
|---|---|
| 0 | Receive status (other than transmit status). The SDA0 line is set for high impedance. |
| 1 | Transmit status. The value in the SO0 latch is enabled for output to the SDA0 line (valid starting at the falling edge of the first byte's ninth clock). |

| Condition for clearing (TRC0 = 0) | Condition for setting (TRC0 = 1) |
|---|---|
| <Both master and slave><br>• When a stop condition is detected<br>• Cleared by LREL0 = 1 (exit from communications)<br>• When the IICE0 bit changes from 1 to 0 (operation stop)<br>• Cleared by WREL0 = 1[Note] (wait cancel)<br>• When the ALD0 bit changes from 0 to 1 (arbitration loss)<br>• Reset<br>• When not used for communication (MSTS0, EXC0, COI0 = 0)<br><Master><br>• When "1" is output to the first byte's LSB (transfer direction specification bit)<br><Slave><br>• When a start condition is detected<br>• When "0" is input to the first byte's LSB (transfer direction specification bit) | <Master><br>• When a start condition is generated<br>• When 0 (master transmission) is output to the LSB (transfer direction specification bit) of the first byte (during address transfer)<br><Slave><br>• When 1 (slave transmission) is input to the LSB (transfer direction specification bit) of the first byte from the master (during address transfer) |

<R>

**Note** When bit 3 (TRC0) of the IIC status register 0 (IICS0) is set to 1 (transmission status), bit 5 (WREL0) of the IIC control register 0 (IICC0) is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while TRC0 bit is 1 (transmission status) by writing to the IIC shift register.

**Remark** LREL0: Bit 6 of IIC control register 0 (IICC0)
IICE0: Bit 7 of IIC control register 0 (IICC0)

**Figure 20-13. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KC2)**

Address: FFE8H After reset: FFH R/W

| Symbol | <7> | <6> | <5> | <4> | <3> | <2> | <1> | <0> |
|---|---|---|---|---|---|---|---|---|
| PR0L | SREPR6 | PPR5 | PPR4 | PPR3 | PPR2 | PPR1 | PPR0 | LVIPR |

Address: FFE9H After reset: FFH R/W

| Symbol | <7> | <6> | <5> | <4> | <3> | <2> | <1> | <0> |
|---|---|---|---|---|---|---|---|---|
| PR0H | TMPR010 | TMPR000 | TMPR50 | TMPRH0 | TMPRH1 | DUALPR0<br>CSIPR10<br>STPR0 | STPR6 | SRPR6 |

Address: FFEAH After reset: FFH R/W

| Symbol | 7 | <6> | <5> | <4> | <3> | <2> | <1> | <0> |
|---|---|---|---|---|---|---|---|---|
| PR1L | 1 | PPR6Note 1 | WTPR | KRPR | TMPR51 | WTIPR | SRPR0 | ADPR |

Address: FFEBH After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | <0> |
|---|---|---|---|---|---|---|---|---|
| PR1H | 1 | 1 | 1 | 1 | 1 | 1 | 1 | IICPR0<br>DMUPRNote 2 |

| XXPRX | Priority level selection |
|---|---|
| 0 | High priority level |
| 1 | Low priority level |

**Notes 1.** 48-pin products only.

**2.** Products whose flash memory is at least 48 KB only.

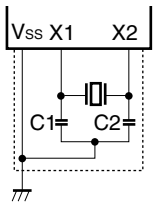
**Cautions 1. Be sure to set bits 6 and 7 of PR1L to 1 in the 38-pin and 44-pin products.**
**Be sure to set bit 7 of PR1L to 1 in the 48-pin products.**

**2. Be sure to set bits 1 to 7 of PR1H to 1.**

**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

**X1 Oscillator Characteristics**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $EV_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = $AV_{SS}$ = 0 V)**

| Resonator | Recommended Circuit | Parameter | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Ceramic resonator, Crystal resonator |  | X1 clock oscillation frequency ($f_X$)Note 1 | Conventional-specification Products ($\mu$PD78F05xx, 78F05xxD) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0Note 2 | | 20.0 | MHz |
| | | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | 1.0Note 2 | | 10.0 | |
| | | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 5.0 | |
| | | | Expanded-specification Products ($\mu$PD78F05xxA, 78F05xxDA) | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0Note 2 | | 20.0 | |
| | | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 5.0 | |

**Notes 1.** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

**2.** It is 2.0 MHz (MIN.) when programming on the board via UART6.

**Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.**

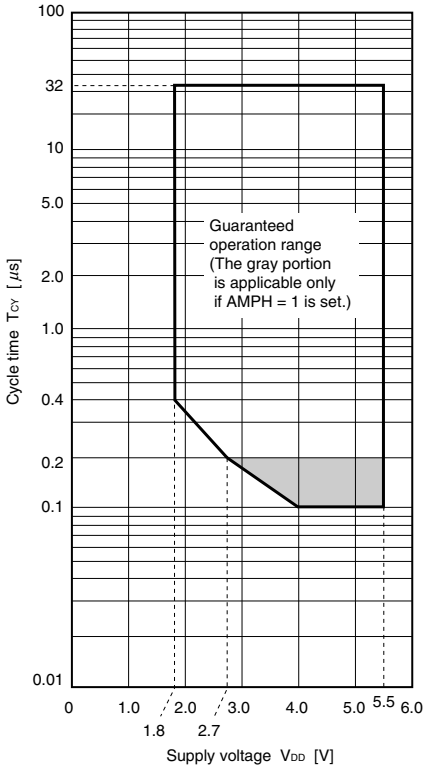
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as $V_{SS}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

**2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

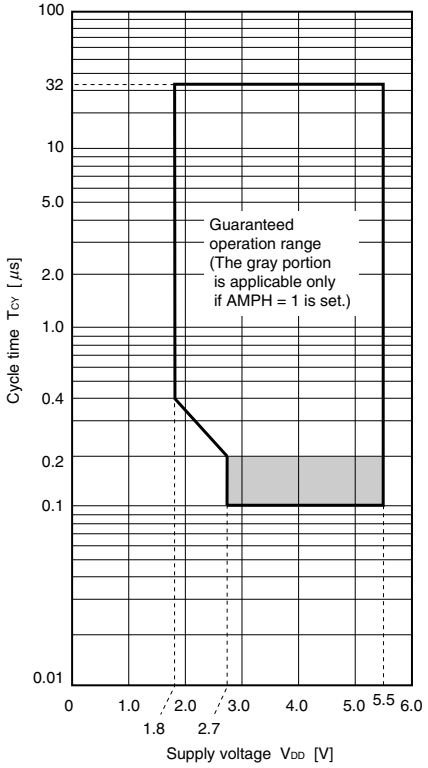
**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

**$T_{CY}$ vs. $V_{DD}$ (Main System Clock Operation)**

**<1> Conventional-specification Products (μPD78F05xx, 78F05xxD)**




**<2> Expanded-specification Products (μPD78F05xxA, 78F05xxDA)**



### (2) Non-port functions

| Port | | 78K0/KB2 | 78K0/KC2 | | | 78K0/KD2 | 78K0/KE2 | 78K0/KF2 |
|---|---|---|---|---|---|---|---|---|
| | | 30/36 Pins | 38 Pins | 44 Pins | 48 Pins | 52 Pins | 64 Pins | 80 Pins |
| Power supply, ground | | $V_{DD}$, $EV_{DD}$[Note 1], $V_{SS}$, $EV_{SS}$[Note 1], $AV_{REF}$, $AV_{SS}$ | $V_{DD}$, $AV_{REF}$, $V_{SS}$, $AV_{SS}$ | | | | $V_{DD}$, $EV_{DD}$, $V_{SS}$, $EV_{SS}$, $AV_{REF}$, $AV_{SS}$ | |
| Regulator | | REGC | | | | | | |
| Reset | | $\overline{\text{RESET}}$ | | | | | | |
| Clock oscillation | | X1, X2, EXCLK | X1, X2, XT1, XT2, EXCLK, EXCLKS | | | | | |
| Writing to flash memory | | FLMD0 | | | | | | |
| Interrupt | | INTP0 to INTP5 | | | INTP0 to INTP6 | | INTP0 to INTP7 | |
| Key interrupt | | – | KR0, KR1 | KR0 to KR3 | | KR0 to KR7 | | |
| Timer | TM00 | TI000, TI010, TO00 | | | | | | |
| | TM01 | – | | | | | TI001[Note 2], TI011[Note 2], TO01[Note 2] | |
| | TM50 | TI50, TO50 | | | | | | |
| | TM51 | TI51, TO51 | | | | | | |
| | TMH0 | TOH0 | | | | | | |
| | TMH1 | TOH1 | | | | | | |
| Serial interface | UART0 | RxD0, TxD0 | | | | | | |
| | UART6 | RxD6, TxD6 | | | | | | |
| | IIC0 | SCL0, SDA0 | SCL0, SDA0, EXSCL0 | | | | | |
| | CSI10 | $\overline{\text{SCK10}}$, SI10, SO10 | | | | | | |
| | CSI11 | – | | | | | $\overline{\text{SCK11}}$[Note 2], SI11[Note 2], SO11[Note 2], $\overline{\text{SSI11}}$[Note 2] | |
| | CSIA0 | – | | | | | | $\overline{\text{SCKA0}}$, SIA0, SOA0, BUSY0, STB0 |
| A/D converter | | ANI0 to ANI3 | ANI0 to ANI5 | ANI0 to ANI7 | | | | |
| Clock output | | – | | | PCL | | | |
| Buzzer output | | – | | | | | BUZ | |
| Low-voltage detector (LVI) | | EXLVI | | | | | | |

**Notes 1.** This is not mounted onto 30-pin products.

**2.** This is not mounted onto the 78K0/KE2 products whose flash memory is less than 32 KB.

**Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.**

**LVI Circuit Characteristics ($T_A$ = –40 to +110°C, $V_{POC} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $AV_{REF} \leq V_{DD}$, $V_{SS} = EV_{SS}$ = 0 V)**

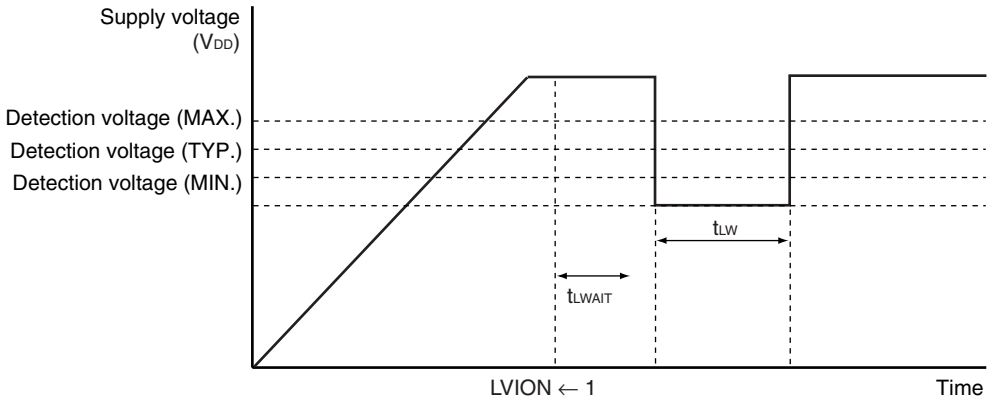
| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVI0}$ | | 4.14 | 4.24 | 4.34 | V |
| | | $V_{LVI1}$ | | 3.99 | 4.09 | 4.19 | V |
| | | $V_{LVI2}$ | | 3.83 | 3.93 | 4.03 | V |
| | | $V_{LVI3}$ | | 3.68 | 3.78 | 3.88 | V |
| | | $V_{LVI4}$ | | 3.52 | 3.62 | 3.72 | V |
| | | $V_{LVI5}$ | | 3.37 | 3.47 | 3.57 | V |
| | | $V_{LVI6}$ | | 3.22 | 3.32 | 3.42 | V |
| | | $V_{LVI7}$ | | 3.06 | 3.16 | 3.26 | V |
| | | $V_{LVI8}$ | | 2.91 | 3.01 | 3.11 | V |
| | | $V_{LVI9}$ | | 2.75 | 2.85 | 2.95 | V |
| | External input pin[Note 1] | EXLVI | EXLVI < $V_{DD}$, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.11 | 1.21 | 1.31 | V |
| Minimum pulse width | | $t_{LW}$ | | 200 | | | μs |
| Operation stabilization wait time[Note 2] | | $t_{LWAIT}$ | | 10 | | | μs |

**Notes 1.** The EXLVI/P120/INTP0 pin is used.

**2.** Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

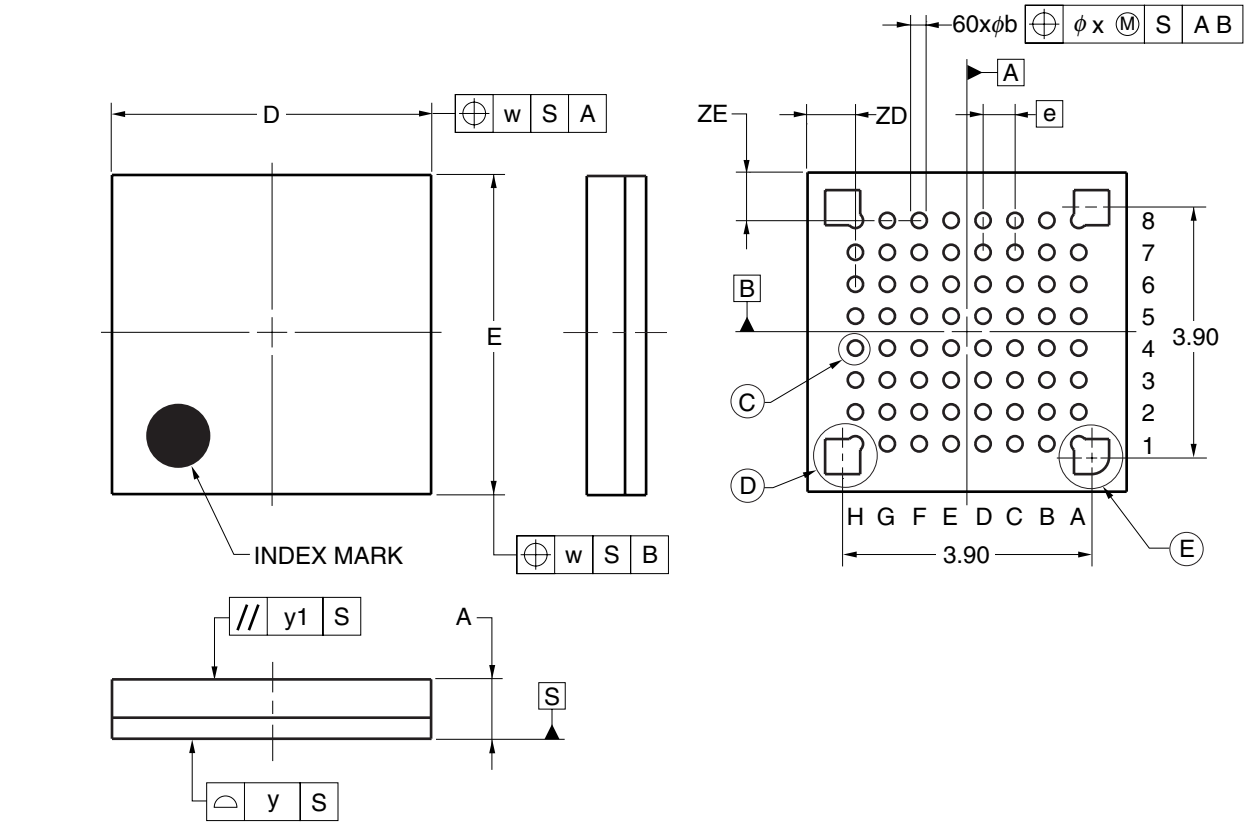
**Remark** $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 9

**LVI Circuit Timing**

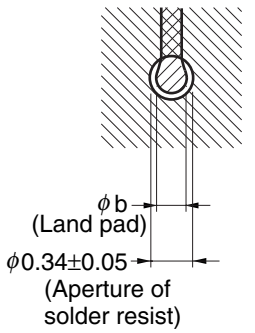


- μPD78F0531FC-AA1-A, 78F0532FC-AA1-A, 78F0533FC-AA1-A, 78F0534FC-AA1-A, 78F0535FC-AA1-A, 78F0536FC-AA1-A, 78F0537FC-AA1-A, 78F0537DFC-AA1-A
- μPD78F0531AFC-AA1-A, 78F0532AFC-AA1-A, 78F0533AFC-AA1-A, 78F0534AFC-AA1-A, 78F0535AFC-AA1-A, 78F0536AFC-AA1-A, 78F0537AFC-AA1-A, 78F0537DAFC-AA1-A

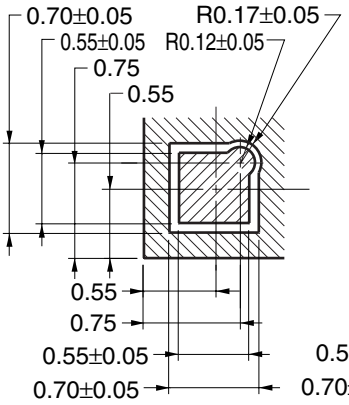
64-PIN PLASTIC FLGA(5x5)



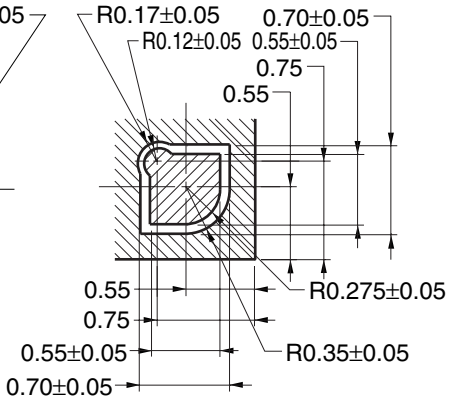

DETAIL OF Ⓒ PART




DETAIL OF Ⓓ PART




DETAIL OF Ⓔ PART




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 5.00±0.10 |
| E | 5.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.91±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

P64FC-50-AA1-1