Renesas Electronics America Inc - UPD78F0501AMC-CAB-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0501amc-cab-ax

1.1.4 Number of flash memory rewrites and retention time

Item	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)	
Number of rewrites per chip (retention time)	100 times (Retention: 10 years)	• When a flash memory programmer is used, and the libraries[Note 1] provided by Renesas Electronics are used • For program update	1,000 times (Retention: 15 years)
		• When the EEPROM emulation libraries[Note 2] provided by Renesas Electronics are used • The rewritable ROM size: 4 KB • For data update	10,000 times (Retention: 5 years)
		Conditions other than the above[Note 3]	100 times (Retention: 10 years)

Notes 1. The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual** (Document No.: **U17516E**) is excluded.

2. The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) is excluded.

3. These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual** (Document No.: **U17516E**) and the sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) are used.

(1) Conventional-specification products (μPD78F05xx and 78F05xxD) (2/3)

<3> When high-speed system clock (X1 oscillation or external clock input) is used and entry RAM is located outside short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		34/f_{CPU}			
Initialize library		49/f_{CPU} + 485.8125			
Mode check library		35/f_{CPU} + 374.75		29/f_{CPU} + 374.75	
Block blank check library		174/f_{CPU} + 6382.0625		134/f_{CPU} + 6382.0625	
Block erase library		174/f_{CPU} + 31093.875	174/f_{CPU} + 298948.125	134/f_{CPU} + 31093.875	134/f_{CPU} + 298948.125
Word write library		318 (321)/f_{CPU} + 644.125	318 (321)/f_{CPU} + 1491.625	262 (265)/f_{CPU} + 644.125	262 (265)/f_{CPU} + 1491.625
Block verify library		174/f_{CPU} + 13448.5625		134/f_{CPU} + 13448.5625	
Self programming end library		34/f_{CPU}			
Get information library	Option value: 03H	171 (172)/f_{CPU} + 432.4375		129 (130)/f_{CPU} + 432.4375	
	Option value: 04H	181 (182)/f_{CPU} + 427.875		139 (140)/f_{CPU} + 427.875	
	Option value: 05H	404 (411)/f_{CPU} + 496.125		362 (369)/f_{CPU} + 496.125	
Set information library		75/f_{CPU} + 79157.6875	75/f_{CPU} + 652400	67f_{CPU} + 79157.6875	67f_{CPU} + 652400
EEPROM write library		318 (321)/f_{CPU} + 799.875	318 (321)/f_{CPU} + 1647.375	262 (265)/f_{CPU} + 799.875	262 (265)/f_{CPU} + 1647.375

Remarks 1. Values in parentheses indicate values when a write start address structure is located other than in the internal high-speed RAM.

2. The above processing times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

3. f_{CPU}: CPU operation clock frequency

4. RSTS: Bit 7 of the internal oscillation mode register (RCM)

1.1.6 Interrupt response time for self programming library

(1) Conventional-specification products (μPD78F05xx and 78F05xxD) (1/2)

<1> When internal high-speed oscillation clock is used

Library Name	Interrupt Response Time (μs (Max.))			
	Normal Model of C Compiler		Static Model of C Compiler/Assembler	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	933.6	668.6	927.9	662.9
Block erase library	1026.6	763.6	1020.9	757.9
Word write library	2505.8	1942.8	2497.8	1934.8
Block verify library	958.6	693.6	952.9	687.9
Set information library	476.5	211.5	475.5	210.5
EEPROM write library	2760.8	2168.8	2759.5	2167.5

Remarks 1. The above interrupt response times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

<2> When high-speed system clock is used (normal model of C compiler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	179/f_{CPU} + 507	179/f_{CPU} + 407	179/f_{CPU} + 1650	179/f_{CPU} + 714
Block erase library	179/f_{CPU} + 559	179/f_{CPU} + 460	179/f_{CPU} + 1702	179/f_{CPU} + 767
Word write library	333/f_{CPU} + 1589	333/f_{CPU} + 1298	333/f_{CPU} + 2732	333/f_{CPU} + 1605
Block verify library	179/f_{CPU} + 518	179/f_{CPU} + 418	179/f_{CPU} + 1661	179/f_{CPU} + 725
Set information library	80/f_{CPU} + 370	80/f_{CPU} + 165	80/f_{CPU} + 1513	80/f_{CPU} + 472
EEPROM write library[Note]	29/f_{CPU} + 1759 333/f_{CPU} + 834	29/f_{CPU} + 1468 333/f_{CPU} + 512	29/f_{CPU} + 1759 333/f_{CPU} + 2061	29/f_{CPU} + 1468 333/f_{CPU} + 873

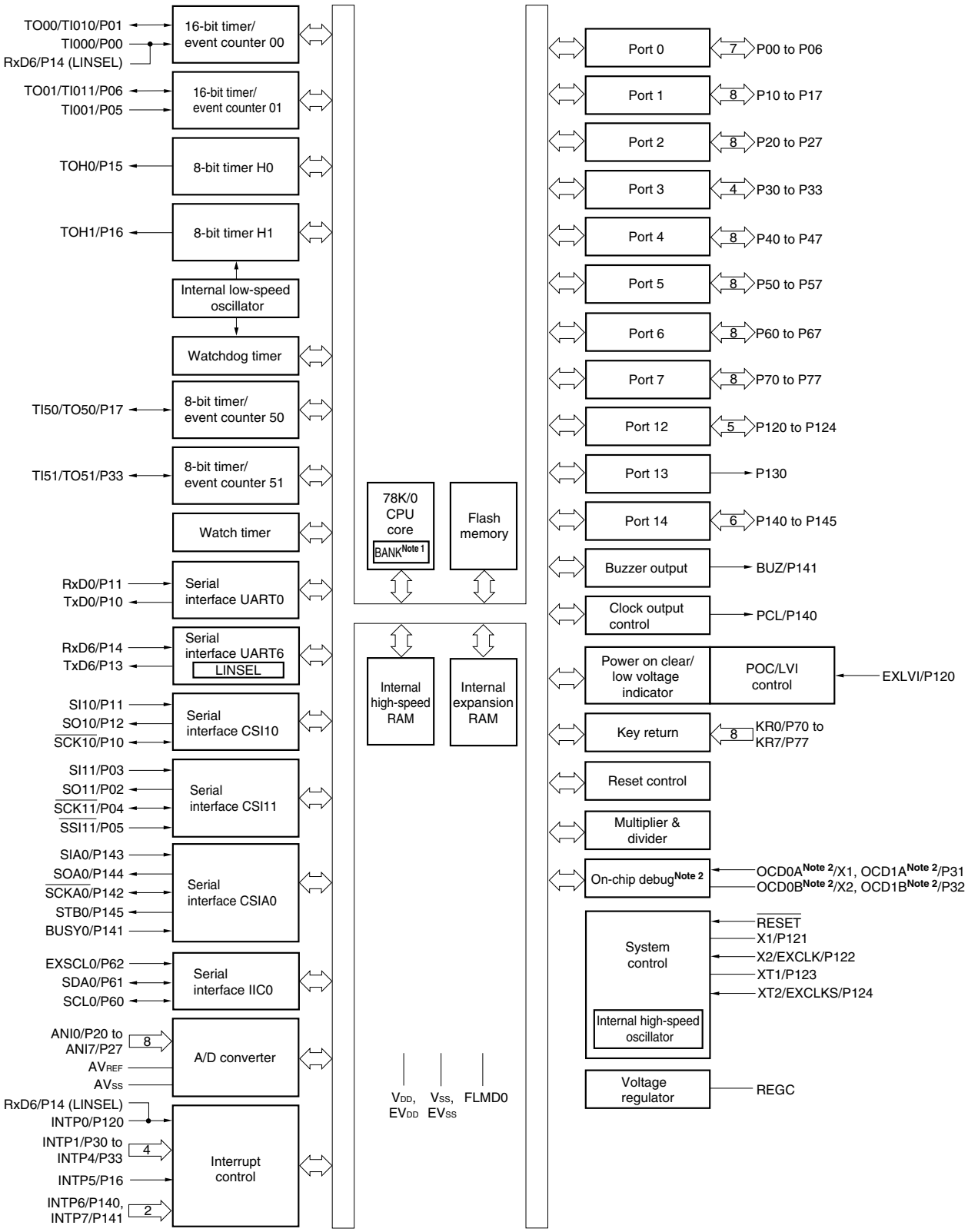
Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

1.7.5 78K0/KF2



Notes 1. Available only in the products whose flash memory is at least 96 KB.

2. Available only in the products with on-chip debug function.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

(e) XT1, XT2

These are the pins for connecting a resonator for subsystem clock.

(f) EXCLKS

This is an external clock input pin for subsystem clock.

Caution Process the P121/X1/OCD0A pin of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P121/X1/OCD0A
Flash memory programmer connection		Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset	
	During reset released	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

Remark X1 and X2 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A and OCD0B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD and 78F05xxDA ONLY).**

2.2.10 P130 (port 13)

P130 functions as an output-only port.

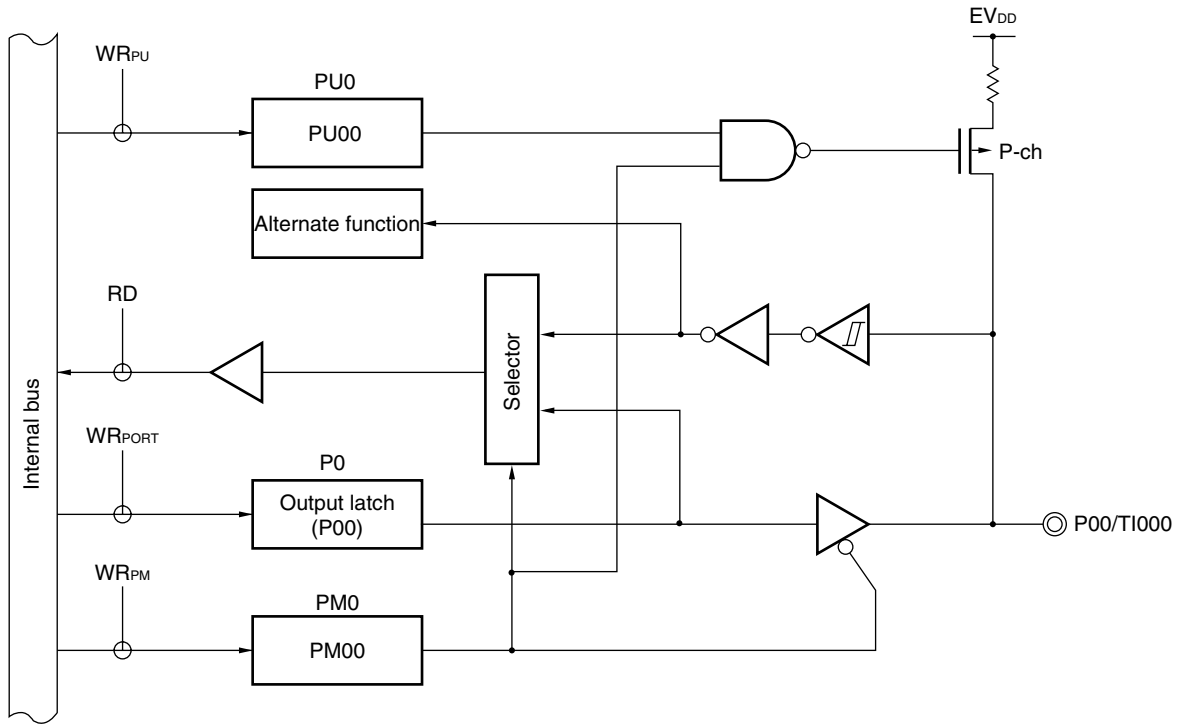
	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P130	–	√Note	√			

Note This is not mounted onto 38-pin and 44-pin products of the 78K0/KC2.

Remarks 1. When the device is reset, P130 outputs a low level. Therefore, to output a high level from P130 before the device is reset, the output signal of P130 can be used as a pseudo reset signal of the CPU (see the figure for **Remark** in **5.2.10 Port 13**).

2. √: Mounted, –: Not mounted

Figure 5-1. Block Diagram of P00

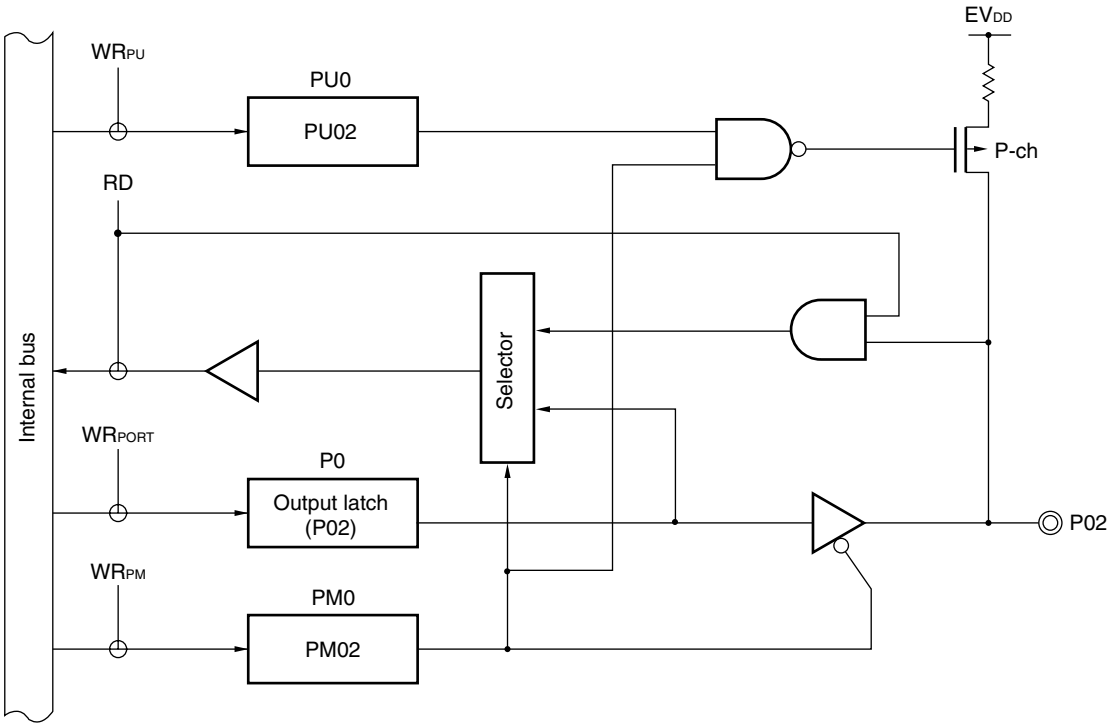


P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-3. Block Diagram of P02 (1/2)

(1) 78K0/KE2 products whose flash memory is less than 32 KB and 78K0/KD2



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-41. Format of Pull-up Resistor Option Register (78K0/KD2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	PU03	PU02	PU01	PU00	FF30H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU4	0	0	0	0	0	0	PU41	PU40	FF34H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	FF37H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W
PU14	0	0	0	0	0	0	0	PU140	FF3EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3, 4, 7, 12, 14; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Table 5-6. Settings of Port Mode Register and Output Latch When Using Alternate Function (2/2)

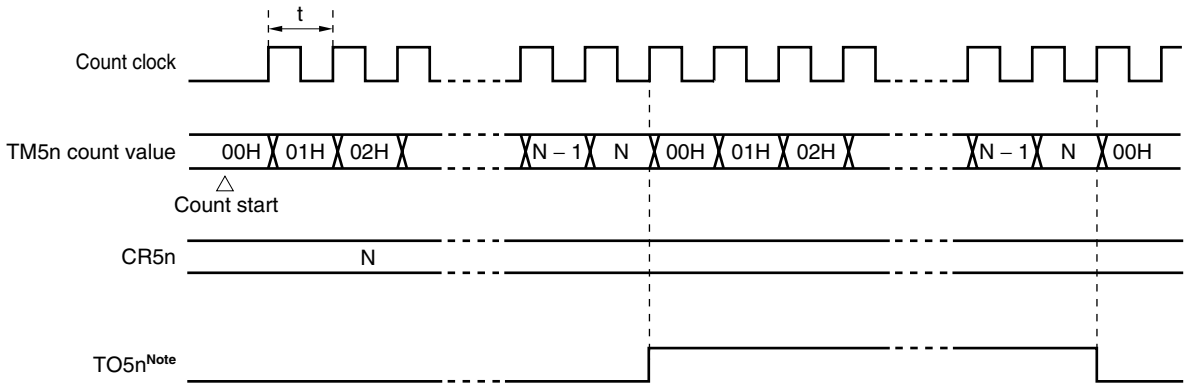
Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P30 to P32	INTP1 to INTP3	Input	1	×
P33	INTP4	Input	1	×
	TI51	Input	1	×
	TO51	Output	0	0
P60	SCL0	I/O	0	0
P61	SDA0	I/O	0	0
P62	EXSCL0	Input	1	×
P70 to P77	KR0 to KR7	Input	1	×
P120	INTP0	Input	1	×
	EXLVI	Input	1	×
P121	X1[Note]	–	×	×
P122	X2[Note]	–	×	×
	EXCLK[Note]	Input	×	×
P123	XT1[Note]	–	×	×
P124	XT2[Note]	–	×	×
	EXCLKS[Note]	Input	×	×
P140	PCL	Output	0	0
	INTP6	Input	1	×
P141	BUZ	Output	0	0
	INTP7	Input	1	×
	BUSY0	Input	1	×
P142	$\overline{\text{SCKA0}}$	Input	1	×
		Output	0	1
P143	SIA0	Input	1	×
P144	SOA0	Output	0	0
P145	STB0	Output	0	0

Note When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK) or subsystem clock (EXCLKS), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **6.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are I/O port pins). At this time, setting of PM121 to PM124 and P121 to P124 is not necessary.

Remarks 1. ×: Don't care
PM××: Port mode register
P××: Port output latch

2. X1, X2, P31, and P32 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A, OCD0B, OCD1A, and OCD1B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD AND 78F05xxDA ONLY).**

Figure 8-13. Square-Wave Output Operation Timing



Note The initial value of TO5n output can be set by bits 2 and 3 (LVR5n, LVS5n) of 8-bit timer mode control register 5n (TMC5n).

8.4.4 PWM output operation

8-bit timer/event counter 5n operates as a PWM output when bit 6 (TMC5n6) of 8-bit timer mode control register 5n (TMC5n) is set to 1.

The duty pulse determined by the value set to 8-bit timer compare register 5n (CR5n) is output from TO5n.

Set the active level width of the PWM pulse to CR5n; the active level can be selected with bit 1 (TMC5n1) of TMC5n.

The count clock can be selected with bits 0 to 2 (TCL5n0 to TCL5n2) of timer clock selection register 5n (TCL5n).

PWM output can be enabled/disabled with bit 0 (TOE5n) of TMC5n.

Caution In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.

Remark n = 0, 1

13.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$1LSB = 1/2^{10} = 1/1024$
$= 0.098\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 13-14. Overall Error

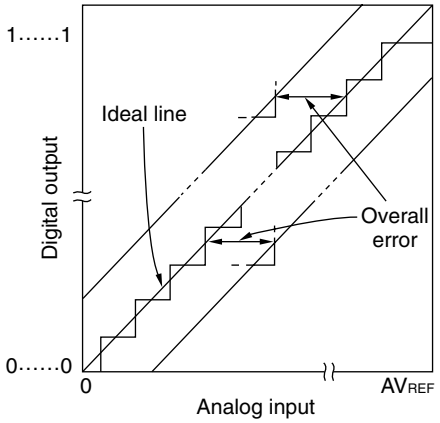
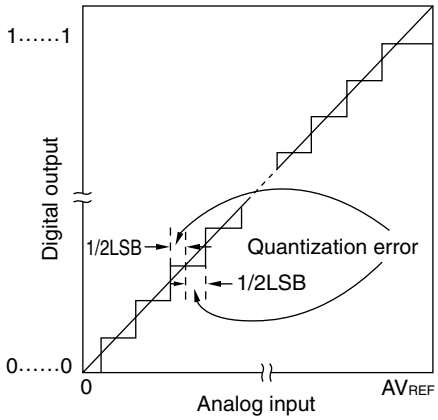


Figure 13-15. Quantization Error



(4) Zero-scale error

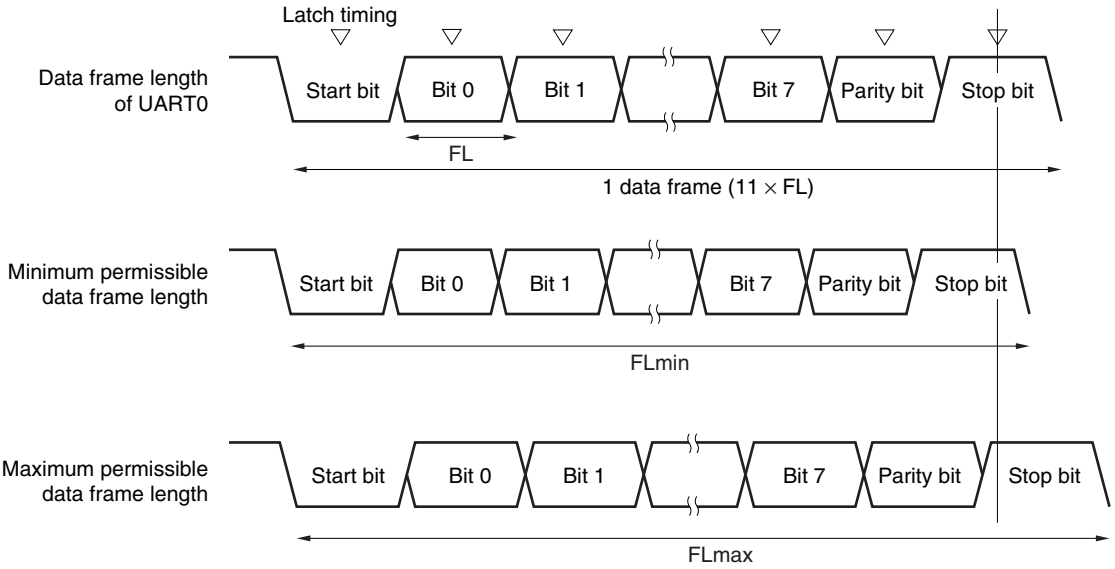
This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.
If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 14-12. Permissible Baud Rate Range During Reception



As shown in Figure 14-12, the latch timing of the receive data is determined by the counter set by baud rate generator control register 0 (BRGC0) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.

Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART0
k: Set value of BRGC0
FL: 1-bit data length
Margin of latch timing: 2 clocks

Figure 15-5. Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (2/2)

PS61	PS60	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL6	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL6	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

ISRM6	Enables/disables occurrence of reception completion interrupt in case of error
0	“INTSRE6” occurs in case of error (at this time, INTSR6 does not occur).
1	“INTSR6” occurs in case of error (at this time, INTSRE6 does not occur).

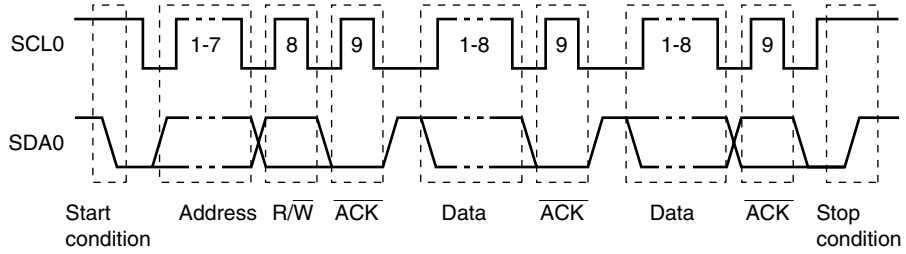
Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE6) of asynchronous serial interface reception error status register 6 (ASIS6) is not set and the error interrupt does not occur.

Cautions
1. **To start the transmission, set POWER6 to 1 and then set TXE6 to 1. To stop the transmission, clear TXE6 to 0, and then clear POWER6 to 0.**
2. **To start the reception, set POWER6 to 1 and then set RXE6 to 1. To stop the reception, clear RXE6 to 0, and then clear POWER6 to 0.**
3. **Set POWER6 to 1 and then set RXE6 to 1 while a high level is input to the RxD6 pin. If POWER6 is set to 1 and RXE6 is set to 1 while a low level is input, reception is started.**
4. **TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.**
5. **Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.**
6. **Clear the TXE6 and RXE6 bits to 0 before rewriting the PS61, PS60, and CL6 bits.**
7. **Fix the PS61 and PS60 bits to 0 when used in LIN communication operation.**
8. **Clear TXE6 to 0 before rewriting the SL6 bit. Reception is always performed with “the number of stop bits = 1”, and therefore, is not affected by the set value of the SL6 bit.**
9. **Make sure that RXE6 = 0 when rewriting the ISRM6 bit.**

18.5 I^2C Bus Definitions and Control Methods

The following section describes the I^2C bus's serial data communication format and the signals used by the I^2C bus. Figure 18-12 shows the transfer timing for the "start condition", "address", "data", and "stop condition" output via the I^2C bus's serial data bus.

Figure 18-12. I^2C Bus Serial Data Transfer Timing



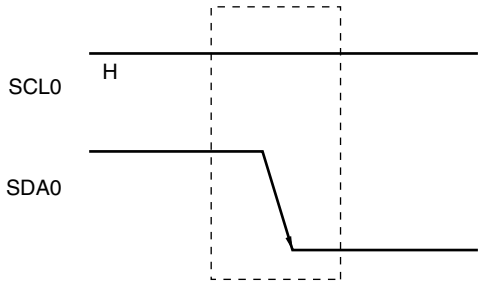
The master device generates the start condition, slave address, and stop condition.
The acknowledge ($\overline{ACK}$) can be generated by either the master or slave device (normally, it is output by the device that receives 8-bit data).

The serial clock (SCL0) is continuously output by the master device. However, in the slave device, the SCL0's low level period can be extended and a wait can be inserted.

18.5.1 Start conditions

A start condition is met when the SCL0 pin is at high level and the SDA0 pin changes from high level to low level. The start conditions for the SCL0 pin and SDA0 pin are signals that the master device generates to the slave device when starting a serial transfer. When the device is used as a slave, start conditions can be detected.

Figure 18-13. Start Conditions



A start condition is output when bit 1 (STT0) of IIC control register 0 (IICC0) is set (to 1) after a stop condition has been detected (SPD0: Bit 0 = 1 in IIC status register 0 (IICS0)). When a start condition is detected, bit 1 (STD0) of IICS0 is set (to 1).

Figure 20-17. Format of External Interrupt Rising Edge Enable Register (EGP) and External Interrupt Falling Edge Enable Register (EGN) (1/2)

(1) 78K0/KB2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

(2) 38-pin and 44-pin products of 78K0/KC2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

(3) 48-pin products of 78K0/KC2, 78K0/KD2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Caution Be sure to clear bits 6 and 7 of EGP and EGN to 0 in 78K0/KB2, and 38-pin and 44-pin products of 78K0/KC2.
Be sure to clear bit 7 of EGP and EGN to 0 in 78K0/KD2, and 48-pin products of 78K0/KC2.

Remark n = 0 to 5: 78K0/KB2, 38-pin and 44-pin products of 78K0/KC2
n = 0 to 6: 78K0/KD2, 48-pin products of 78K0/KC2

21.3 Register Controlling Key Interrupt

(1) Key return mode register (KRM)

This register controls the KRMn bit using the KRn signal.

KRM is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears KRM to 00H.

Figure 21-2. Format of Key Return Mode Register (KRM)

(1) 38-pin products of 78K0/KC2

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	0	0	KRM1	KRM0

(2) 44-pin and 48-pin products of 78K0/KC2

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	KRM3	KRM2	KRM1	KRM0

(3) 78K0/KD2, 78K0/KE2, 78K0/KF2

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

Cautions 1. If any of the KRMn bits used is set to 1, set bit n (PU7n) of the corresponding pull-up resistor register 7 (PU7) to 1.

2. If KRM is changed, the interrupt request flag may be set. Therefore, disable interrupts and then change the KRM register. Clear the interrupt request flag and enable interrupts.

3. The bits not used in the key interrupt mode can be used as normal ports.

4. For the 38-pin products of 78K0/KC2, be sure to set bits 2 to 7 of KRM to "0". For the 44-pin and 48-pin products of 78K0/KC2, be sure to set bits 4 to 7 of KRM to "0".

Remark n = 0, 1: 38-pin products of 78K0/KC2

n = 0 to 3: 44-pin and 48-pin products of 78K0/KC2

n = 0 to 7: 78K0/KD2, 78K0/KE2, 78K0/KF2

CHAPTER 22 STANDBY FUNCTION

22.1 Standby Function and Configuration

22.1.1 Standby function

The standby function is mounted onto all 78K0/Kx2 microcontroller products.

The standby function is designed to reduce the operating current of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, internal low-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

Note The 78K0/KB2 is not provided with a subsystem clock oscillator.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The subsystem clock oscillation cannot be stopped. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

<R> 27.11 Creating ROM Code to Place Order for Previously Written Product

Before placing an order with Renesas Electronics for a previously written product, the ROM code for the order must be created.

To create the ROM code, use the Hex Consolidation Utility (hereafter abbreviated to HCU) on the finished programs (hex files) and optional data (such as security settings for flash memory programs).

The HCU is a software tool that includes functions required for creating ROM code.

The HCU can be downloaded at the Renesas Electronics website.

(1) Website

http:www2.renesas.com/micro/en/ods → Click Version-up Service.

(2) Downloading the HCU

To download the HCU, click Software for previously written flash products and then HCU_GUI.

Remark For details about how to install and use the HCU, see the materials (the user's manual) that comes with the HCU at the above website.

27.11.1 Procedure for using ROM code to place an order

Use the HCU to create the ROM code by following the procedure below, and then place your order with Renesas Electronics. For details, see the ROM Code Ordering Method Information (C10302J).

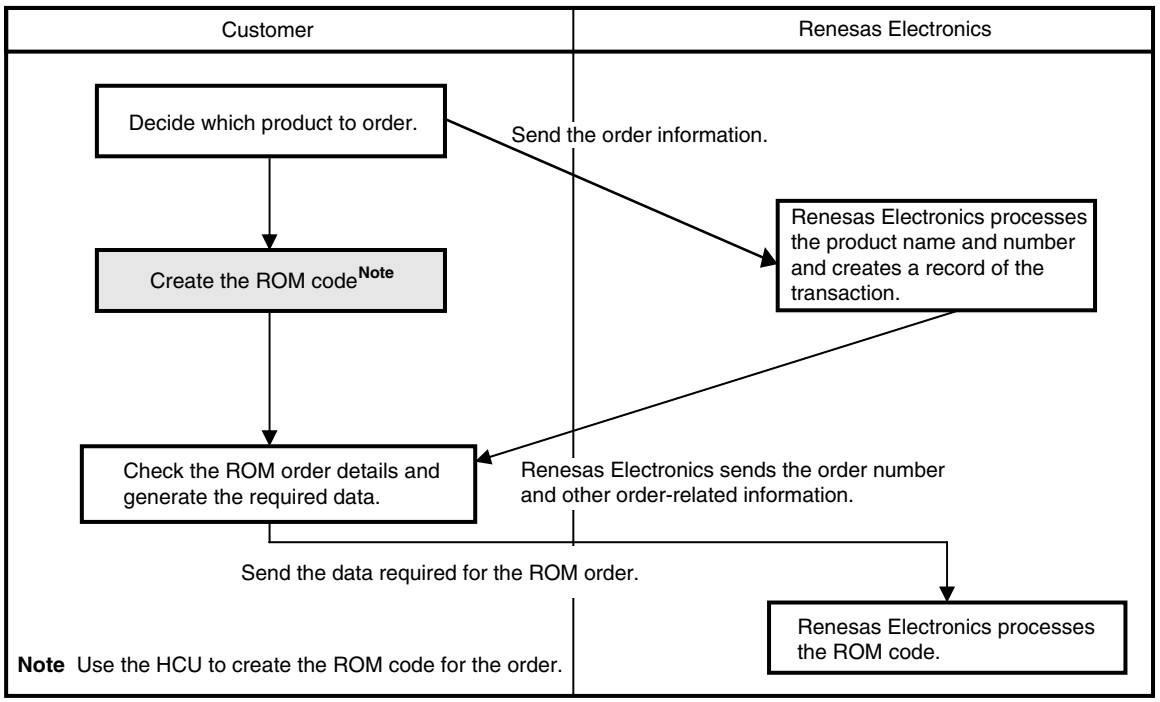
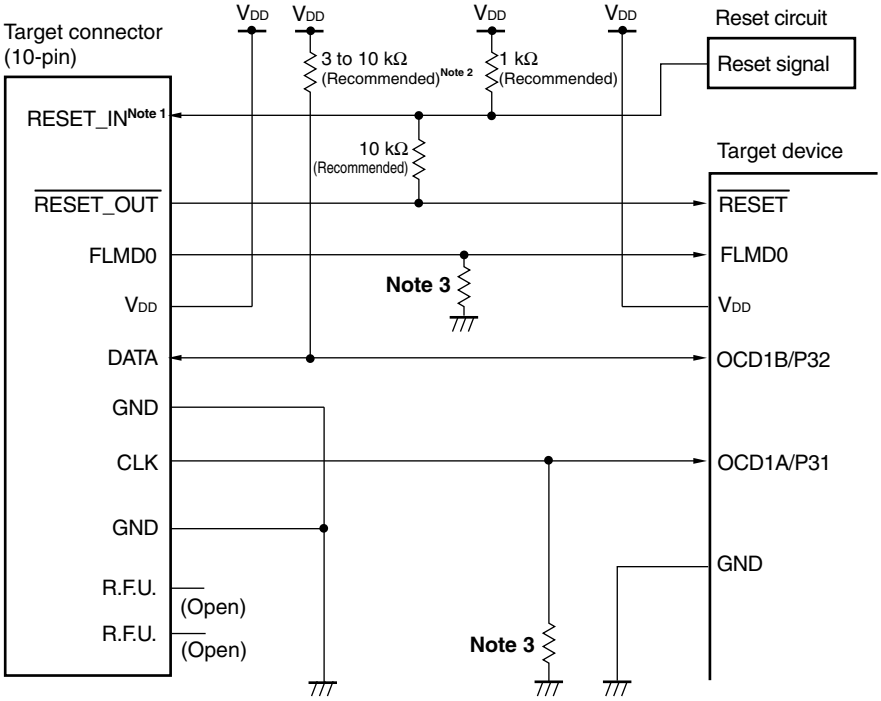


Figure 28-2. Connection Example of QB-MINI2 and μPD78F05xxD and 78F05xxDA (When OCD1A/P31 and OCD1B/P32 Are Used)



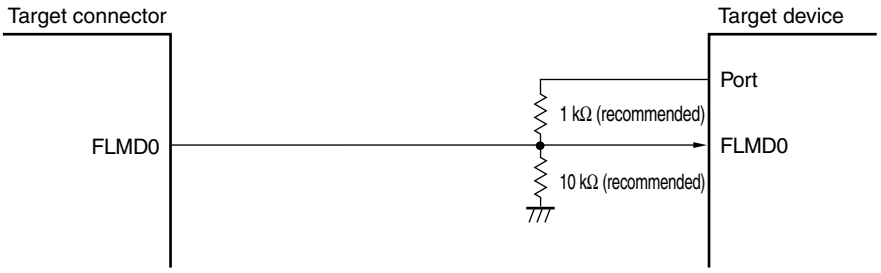
Notes 1. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **QB-MINI2 User's Manual (U18371E)**.

2. This is the processing of the pin when OCD1B/P32 is set as the input port (to prevent the pin from being left opened when not connected to QB-MINI2).

3. Make pull-down resistor 470 Ω or more (10 kΩ: recommended).

Connect the FLMD0 pin as follows when performing self programming by means of on-chip debugging.

Figure 28-3. Connection of FLMD0 Pin for Self Programming by Means of On-Chip Debugging



Caution When using the port that controls the FLMD0 pin, make sure that it satisfies the values of the high-level output current and FLMD0 supply voltage (minimum value: 0.8VDD) stated in CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: TA = –40 to +125°C).

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second Operand / First Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second Operand / First Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1