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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFLGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0502afc-aa3-a

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flag (ISP)

This flag manages the priority of acknowledgeable maskable vectored interrupts. When this flag is 0, low-level vectored interrupt requests specified by a priority specification flag register (PR0L, PR0H, PR1L, PR1H) (see **20.3 (3) Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

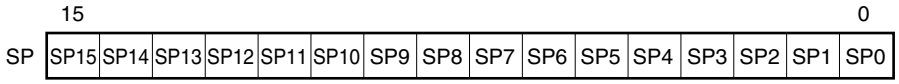
(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area.

Figure 3-22. Format of Stack Pointer



The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves/restores data as shown in Figures 3-23 and 3-24.

Caution Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

Figure 5-43. Format of Pull-up Resistor Option Register (78K0/KF2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00	FF30H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40	FF34H	00H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	FF35H	00H	R/W
PU6	PU67	PU66	PU65	PU64	0	0	0	0	FF36H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	FF37H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W
PU14	0	0	PU145	PU144	PU143	PU142	PU141	PU140	FF3EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 7, 12, 14; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

(4) A/D port configuration register (ADPC)

This register switches the P20/ANI0 to P27/ANI7 pins to digital I/O of port or analog input of A/D converter.

ADPC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark P20/ANI0 to P23/ANI3 pins: 78K0/KB2
P20/ANI0 to P25/ANI5 pins: 38-pin products of 78K0/KC2
P20/ANI0 to P27/ANI7 pins: Products other than above

Table 5-6. Settings of Port Mode Register and Output Latch When Using Alternate Function (1/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P00	TI000	Input	1	×
P01	TI010	Input	1	×
	TO00	Output	0	0
P02	SO11	Output	0	0
P03	SI11	Input	1	×
P04	$\overline{SCK11}$	Input	1	×
		Output	0	1
P05	$\overline{SSI11}$	Input	1	×
	TI001	Input	1	×
P06	TI011	Input	1	×
	TO01	Output	0	0
P10	$\overline{SCK10}$	Input	1	×
		Output	0	1
	TxD0	Output	0	1
P11	SI10	Input	1	×
	RxD0	Input	1	×
P12	SO10	Output	0	0
P13	TxD6	Output	0	1
P14	RxD6	Input	1	×
P15	TOH0	Output	0	0
P16	TOH1	Output	0	0
	INTP5	Input	1	×
P17	TI50	Input	1	×
	TO50	Output	0	0
P20 to P27[Note]	ANI0 to ANI7[Note]	Input	1	×

Note The function of the ANI0/P20 to ANI7/P27 pins can be selected by using the A/D port configuration register (ADPC), the analog input channel specification register (ADS), and PM2.

ADPC	PM2	ADS	ANI0/P20 to ANI7/P27 Pins
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output

Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

Table 5-6. Settings of Port Mode Register and Output Latch When Using Alternate Function (2/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P30 to P32	INTP1 to INTP3	Input	1	×
P33	INTP4	Input	1	×
	TI51	Input	1	×
	TO51	Output	0	0
P60	SCL0	I/O	0	0
P61	SDA0	I/O	0	0
P62	EXSCL0	Input	1	×
P70 to P77	KR0 to KR7	Input	1	×
P120	INTP0	Input	1	×
	EXLVI	Input	1	×
P121	X1[Note]	–	×	×
P122	X2[Note]	–	×	×
	EXCLK[Note]	Input	×	×
P123	XT1[Note]	–	×	×
P124	XT2[Note]	–	×	×
	EXCLKS[Note]	Input	×	×
P140	PCL	Output	0	0
	INTP6	Input	1	×
P141	BUZ	Output	0	0
	INTP7	Input	1	×
	BUSY0	Input	1	×
P142	$\overline{\text{SCKA0}}$	Input	1	×
		Output	0	1
P143	SIA0	Input	1	×
P144	SOA0	Output	0	0
P145	STB0	Output	0	0

Note When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK) or subsystem clock (EXCLKS), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **6.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are I/O port pins). At this time, setting of PM121 to PM124 and P121 to P124 is not necessary.

Remarks 1. ×: Don't care
PM××: Port mode register
P××: Port output latch

2. X1, X2, P31, and P32 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A, OCD0B, OCD1A, and OCD1B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD AND 78F05xxDA ONLY).**

Figure 6-3. Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KB2)

Address: FF9FH After reset: 00H R/W

Symbol	<7>	<6>	5	4	3	2	1	<0>
OSCCTL	EXCLK	OSCSEL	0	0	0	0	0	AMPH

EXCLK	OSCSEL	High-speed system clock pin operation mode	P121/X1 pin	P122/X2/EXCLK pin
0	0	I/O port mode	I/O port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	I/O port mode	I/O port	
1	1	External clock input mode	I/O port	External clock input

AMPH	Operating frequency control
0	1 MHz ≤ f_{XH} ≤ 10 MHz
1	10 MHz < f_{XH} ≤ 20 MHz

Cautions 1. Be sure to set AMPH to 1 if the high-speed system clock oscillation frequency exceeds 10 MHz.

<R> **2. Set AMPH before setting the main clock mode register (MCM).**

3. Set AMPH before setting the peripheral functions after a reset release. The value of AMPH can be changed only once after a reset release. When the high-speed system clock (X1 oscillation) is selected as the CPU clock, supply of the CPU clock is stopped for 4.06 to 16.12 μs after AMPH is set to 1. When the high-speed system clock (external clock input) is selected as the CPU clock, supply of the CPU clock is stopped for the duration of 160 external clocks after AMPH is set to 1.

4. If the STOP instruction is executed when AMPH = 1, supply of the CPU clock is stopped for 4.06 to 16.12 μs after the STOP mode is released when the internal high-speed oscillation clock is selected as the CPU clock, or for the duration of 160 external clocks when the high-speed system clock (external clock input) is selected as the CPU clock. When the high-speed system clock (X1 oscillation) is selected as the CPU clock, the oscillation stabilization time is counted after the STOP mode is released.

5. To change the value of EXCLK and OSCSEL, be sure to confirm that bit 7 (MSTOP) of the main OSC control register (MOC) is 1 (the X1 oscillator stops or the external clock from the EXCLK pin is disabled).

6. Be sure to clear bits 1 to 5 to 0.

Remark f_{XH}: High-speed system clock oscillation frequency

6.6.5 Clocks supplied to CPU and peripheral hardware

The following table shows the relation among the clocks supplied to the CPU and peripheral hardware, and setting of registers.

Table 6-4. Clocks Supplied to CPU and Peripheral Hardware, and Register Setting (78K0/KB2)

Supplied Clock		XSEL	MCM0	EXCLK
Clock Supplied to CPU	Clock Supplied to Peripheral Hardware			
Internal high-speed oscillation clock		0	×	×
Internal high-speed oscillation clock	X1 clock	1	0	0
	External main system clock	1	0	1
X1 clock		1	1	0
External main system clock		1	1	1

Remarks 1. The 78K0/KB2 is not provided with a subsystem clock.

2. XSEL: Bit 2 of the main clock mode register (MCM)
MCM0: Bit 0 of MCM
EXCLK: Bit 7 of the clock operation mode select register (OSCCTL)
×: don't care

Table 6-5. Clocks Supplied to CPU and Peripheral Hardware, and Register Setting (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)

Supplied Clock		XSEL	CSS	MCM0	EXCLK
Clock Supplied to CPU	Clock Supplied to Peripheral Hardware				
Internal high-speed oscillation clock		0	0	×	×
Internal high-speed oscillation clock	X1 clock	1	0	0	0
	External main system clock	1	0	0	1
X1 clock		1	0	1	0
External main system clock		1	0	1	1
Subsystem clock	Internal high-speed oscillation clock	0	1	×	×
	X1 clock	1	1	0	0
		1	1	1	0
	External main system clock	1	1	0	1
		1	1	1	1

Remark XSEL: Bit 2 of the main clock mode register (MCM)
CSS: Bit 4 of the processor clock control register (PCC)
MCM0: Bit 0 of MCM
EXCLK: Bit 7 of the clock operation mode select register (OSCCTL)
×: don't care

6.6.8 Time required for switchover of CPU clock and main system clock

By setting bits 0 to 2 (PCC0 to PCC2) and bit 4 (CSS) of the processor clock control register (PCC), the CPU clock can be switched (between the main system clock and the subsystem clock) and the division ratio of the main system clock can be changed.

The actual switchover operation is not performed immediately after rewriting to PCC; operation continues on the pre-switchover clock for several clocks (see **Table 6-8** and **6-9**).

Whether the CPU is operating on the main system clock or the subsystem clock[Note] can be ascertained using bit 5 (CLS) of the PCC register.

Note The 78K0/KB2 is not provided with a subsystem clock.

Table 6-8. Time Required for Switchover of CPU Clock and Main System Clock Cycle Division Factor (78K0/KB2)

Set Value Before Switchover			Set Value After Switchover														
PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0
			0	0	0	0	0	1	0	1	0	0	1	1	1	0	0
0	0	0				16 clocks			16 clocks			16 clocks			16 clocks		
0	0	1	8 clocks						8 clocks			8 clocks			8 clocks		
0	1	0	4 clocks			4 clocks						4 clocks			4 clocks		
0	1	1	2 clocks			2 clocks			2 clocks						2 clocks		
1	0	0	1 clock			1 clock			1 clock			1 clock					

Remark The number of clocks listed in Table 6-8 is the number of CPU clocks before switchover.

Table 6-9. Time Required for Switchover of CPU Clock and Main System Clock Cycle Division Factor (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)

Set Value Before Switchover				Set Value After Switchover																							
CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0
				0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	×	×	×
0	0	0	0					16 clocks				16 clocks				16 clocks				16 clocks				$2f_{XP}/f_{SUB}$ clocks			
	0	0	1	8 clocks								8 clocks				8 clocks				8 clocks				f_{XP}/f_{SUB} clocks			
	0	1	0	4 clocks				4 clocks								4 clocks				4 clocks				$f_{XP}/2f_{SUB}$ clocks			
	0	1	1	2 clocks				2 clocks				2 clocks								2 clocks				$f_{XP}/4f_{SUB}$ clocks			
	1	0	0	1 clock				1 clock				1 clock				1 clock								$f_{XP}/8f_{SUB}$ clocks			
1	×	×	×	2 clocks				2 clocks				2 clocks				2 clocks				2 clocks							

Caution Selection of the main system clock cycle division factor (PCC0 to PCC2) and switchover from the main system clock to the subsystem clock (changing CSS from 0 to 1) should not be set simultaneously.

Simultaneous setting is possible, however, for selection of the main system clock cycle division factor (PCC0 to PCC2) and switchover from the subsystem clock to the main system clock (changing CSS from 1 to 0).

Remark 1. The number of clocks listed in Table 6-9 is the number of CPU clocks before switchover.

7.4 Operation of 16-Bit Timer/Event Counters 00 and 01

7.4.1 Interval timer operation

If bits 3 and 2 (TMC0n3 and TMC0n2) of the 16-bit timer mode control register (TMC0n) are set to 11 (clear & start mode entered upon a match between TM0n and CR00n), the count operation is started in synchronization with the count clock.

When the value of TM0n later matches the value of CR00n, TM0n is cleared to 0000H and a match interrupt signal (INTTM00n) is generated. This INTTM00n signal enables TM0n to operate as an interval timer.

Remarks 1. For the setting of I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 7-16. Block Diagram of Interval Timer Operation

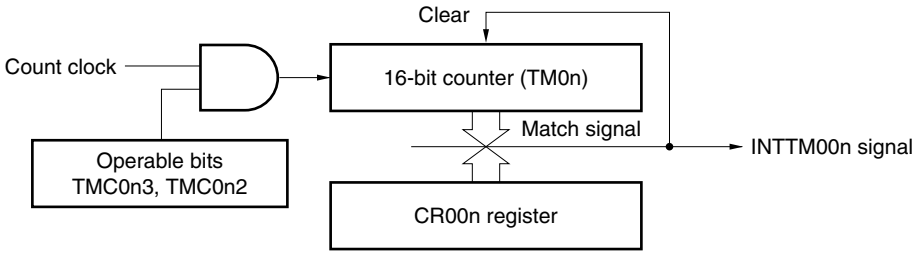
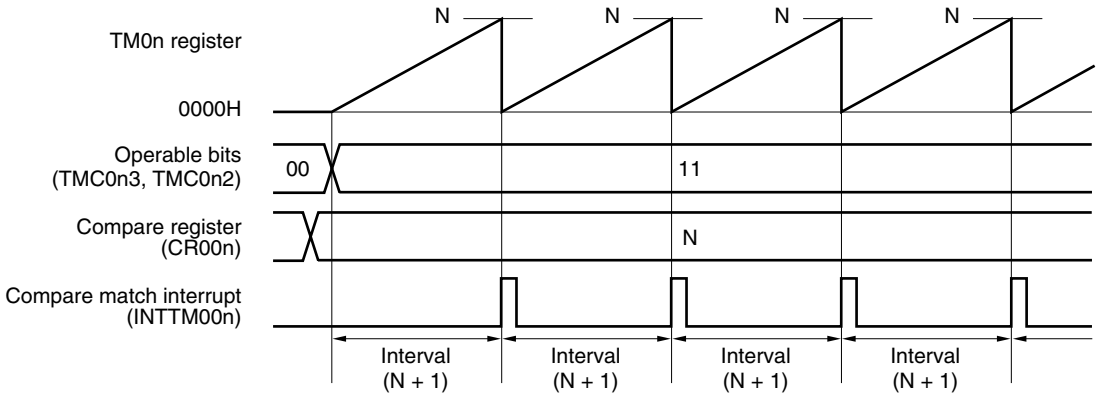


Figure 7-17. Basic Timing Example of Interval Timer Operation



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

Caution When data is read from ADCR and ADCRH, a wait cycle is generated. Do not read data from ADCR and ADCRH when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. Make this pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

The signal input to ANI0 to ANI7 is converted into a digital signal, based on the voltage applied across AV_{REF} and AV_{SS}.

(10) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always use this pin at the same potential as that of the V_{SS} pin even when the A/D converter is not used.

(11) A/D converter mode register (ADM)

This register is used to set the conversion time of the analog input signal to be converted, and to start or stop the conversion operation.

(12) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 pins to analog input of A/D converter or digital I/O of port.

(13) Analog input channel specification register (ADS)

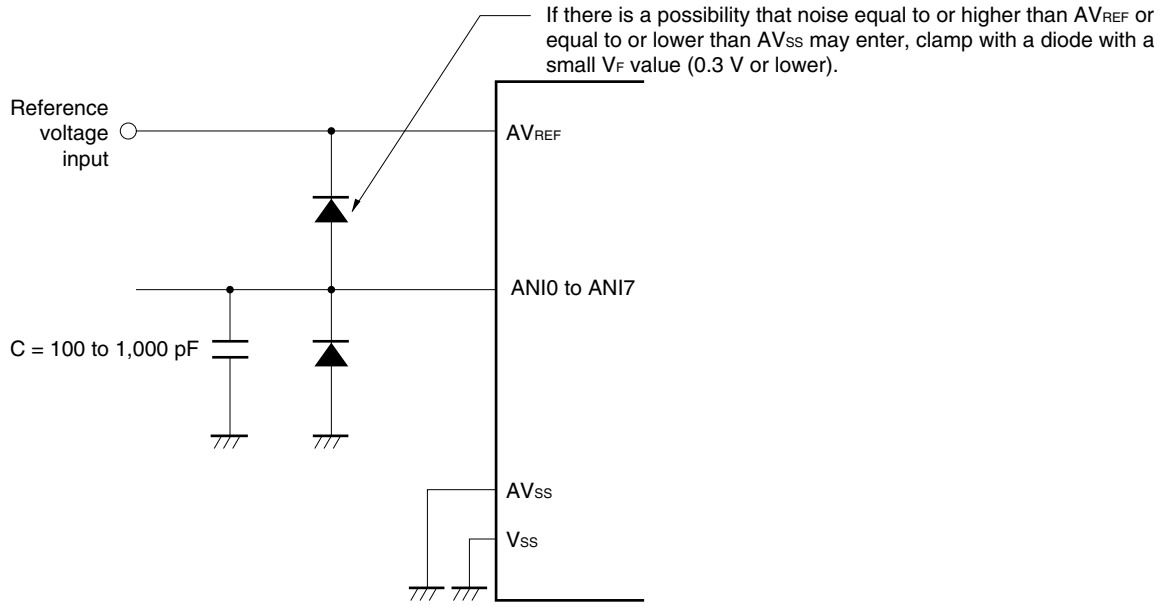
This register is used to specify the port that inputs the analog voltage to be converted into a digital signal.

(14) Port mode register 2 (PM2)

This register switches the ANI0/P20 to ANI7/P27 pins to input or output.

Remark ANI0 to ANI3: 78K0/KB2
ANI0 to ANI5: 38-pin products of the 78K0/KC2
ANI0 to ANI7: Products other than above

Figure 13-20. Analog Input Pin Connection



(5) ANI0/P20 to ANI7/P27

<1> The analog input pins (ANI0 to ANI7) are also used as I/O port pins (P20 to P27).
When A/D conversion is performed with any of ANI0 to ANI7 selected, do not access P20 to P27 while conversion is in progress; otherwise the conversion resolution may be degraded. It is recommended to select pins used as P20 to P27 starting with the ANI0/P20 that is the furthest from AV_{REF}.

<2> If a digital pulse is applied to the pins adjacent to the pins currently used for A/D conversion, the expected value of the A/D conversion may not be obtained due to coupling noise. Therefore, do not apply a pulse to the pins adjacent to the pin undergoing A/D conversion.

(6) Input impedance of ANI0 to ANI7 pins

This A/D converter charges a sampling capacitor for sampling during sampling time.
Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.
To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 10 kΩ, and to connect a capacitor of about 100 pF to the ANI0 to ANI7 pins (see **Figure 13-20**).

(7) AV_{REF} pin input impedance

A series resistor string of several tens of kΩ is connected between the AV_{REF} and AV_{SS} pins.
Therefore, if the output impedance of the reference voltage source is high, this will result in a series connection to the series resistor string between the AV_{REF} and AV_{SS} pins, resulting in a large reference voltage error.

Remark ANI0 to ANI3: 78K0/KB2
ANI0 to ANI5: 38-pin products of the 78K0/KC2
ANI0 to ANI7: Products other than above

(b) Parity types and operation

The parity bit is used to detect a bit error in communication data. Usually, the same type of parity bit is used on both the transmission and reception sides. With even parity and odd parity, a 1-bit (odd number) error can be detected. With zero parity and no parity, an error cannot be detected.

(i) Even parity

- Transmission

  Transmit data, including the parity bit, is controlled so that the number of bits that are "1" is even.
  The value of the parity bit is as follows.

  If transmit data has an odd number of bits that are "1": 1
  If transmit data has an even number of bits that are "1": 0

- Reception

  The number of bits that are "1" in the receive data, including the parity bit, is counted. If it is odd, a parity error occurs.

(ii) Odd parity

- Transmission

  Unlike even parity, transmit data, including the parity bit, is controlled so that the number of bits that are "1" is odd.

  If transmit data has an odd number of bits that are "1": 0
  If transmit data has an even number of bits that are "1": 1

- Reception

  The number of bits that are "1" in the receive data, including the parity bit, is counted. If it is even, a parity error occurs.

(iii) 0 parity

The parity bit is cleared to 0 when data is transmitted, regardless of the transmit data.
The parity bit is not detected when the data is received. Therefore, a parity error does not occur regardless of whether the parity bit is "0" or "1".

(iv) No parity

No parity bit is appended to the transmit data.
Reception is performed assuming that there is no parity bit when data is received. Because there is no parity bit, a parity error does not occur.

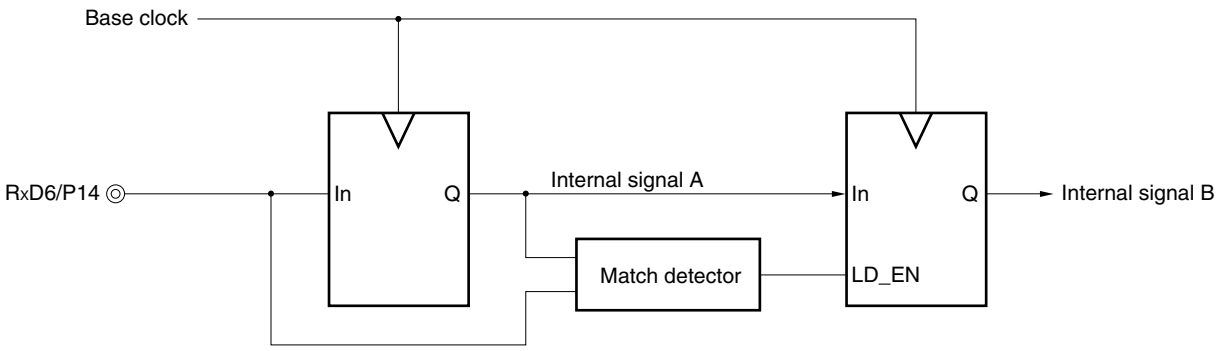
(g) Noise filter of receive data

The RxD6 signal is sampled with the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 15-21, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 15-21. Noise Filter Circuit



(h) SBF transmission

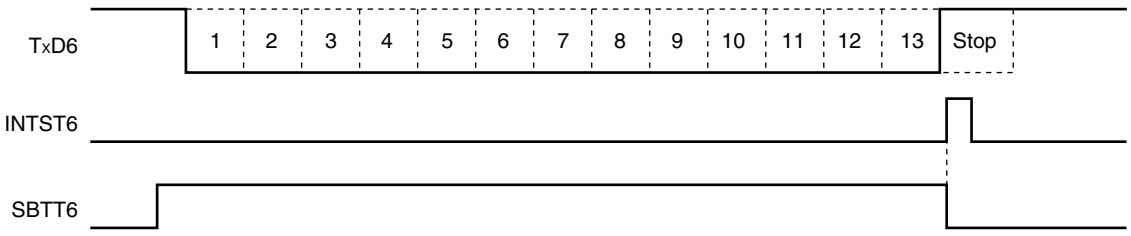
When the device is use in LIN communication operation, the SBF (Synchronous Break Field) transmission control function is used for transmission. For the transmission operation of LIN, see **Figure 15-1 LIN Transmission Operation**.

When bit 7 (POWER6) of asynchronous serial interface mode register 6 (ASIM6) is set to 1, the TxD6 pin outputs high level. Next, when bit 6 (TXE6) of ASIM6 is set to 1, the transmission enabled status is entered, and SBF transmission is started by setting bit 5 (SBTT6) of asynchronous serial interface control register 6 (ASICL6) to 1.

Thereafter, a low level of bits 13 to 20 (set by bits 4 to 2 (SBL62 to SBL60) of ASICL6) is output. Following the end of SBF transmission, the transmission completion interrupt request (INTST6) is generated and SBTT6 is automatically cleared. Thereafter, the normal transmission mode is restored.

Transmission is suspended until the data to be transmitted next is written to transmit buffer register 6 (TXB6), or until SBTT6 is set to 1.

Figure 15-22. SBF Transmission



Remark TxD6: TxD6 pin (output)
INTST6: Transmission completion interrupt request
SBTT6: Bit 5 of asynchronous serial interface control register 6 (ASICL6)

(e) Automatic transmission/reception suspension and restart

Automatic transmission/reception can be temporarily suspended by setting bit 1 (ATSTP0) of serial trigger register 0 (CSIT0) to 1.

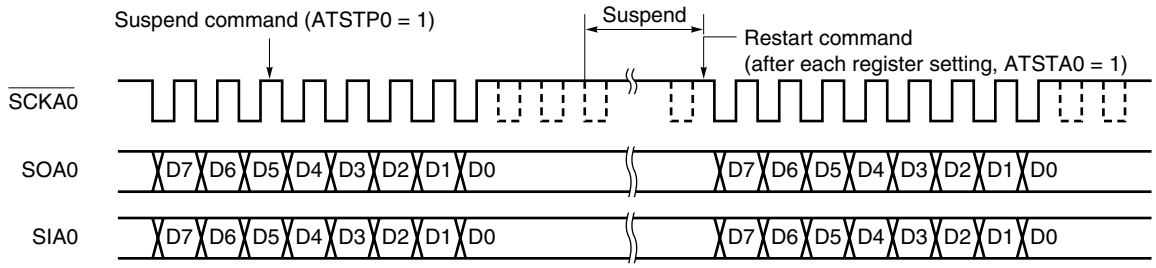
During 8-bit data communication, the transmission/reception is not suspended. It is suspended upon completion of 8-bit data communication.

When suspended, bit 0 (TSF0) of serial status register 0 (CSIS0) is cleared to 0 after transfer of the 8th bit.

Cautions 1. If the HALT instruction is executed during automatic transmission/reception, communication is suspended and the HALT mode is set if during 8-bit data communication. When the HALT mode is cleared, automatic transmission/reception is restarted from the suspended point.

2. When suspending automatic transmission/reception, do not change the operating mode to 3-wire serial I/O mode while TSF0 = 1.

Figure 17-22. Automatic Transmission/Reception Suspension and Restart



ATSTP0: Bit 1 of serial trigger register 0 (CSIT0)

ATSTA0: Bit 0 of CSIT0

18.5.6 Wait

The wait is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCL0 pin to low level notifies the communication partner of the wait state. When wait state has been canceled for both the master and slave devices, the next data transfer can begin.

Figure 18-18. Wait (1/2)

(1) When master device has a nine-clock wait and slave device has an eight-clock wait (master transmits, slave receives, and ACKE0 = 1)

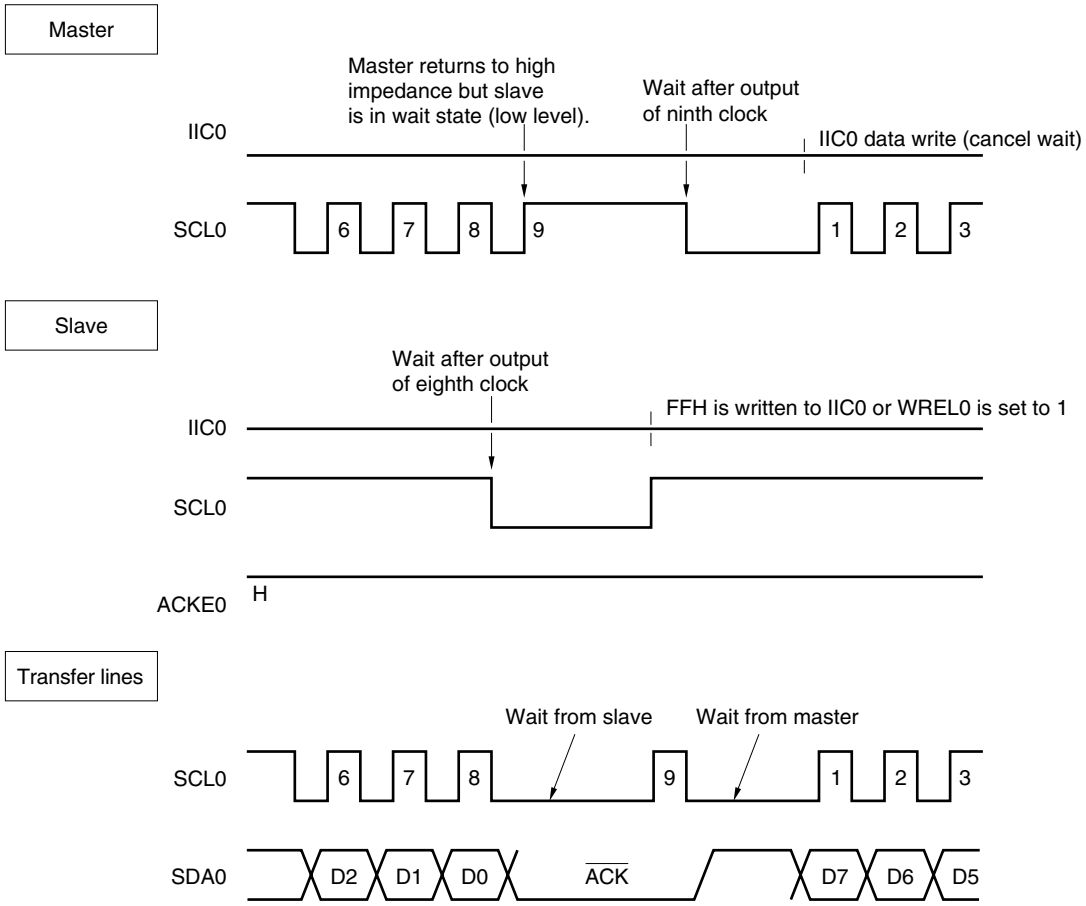


Figure 27-2. Format of Internal Expansion RAM Size Switching Register (IXS)

Address: FFF4H After reset: 0CH R/W

Symbol	7	6	5	4	3	2	1	0
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expansion RAM capacity selection
1	1	0	0	0 bytes
1	0	1	0	1024 bytes
1	0	0	0	2048 bytes
0	1	0	0	4096 bytes
0	0	0	0	6144 bytes
Other than above				Setting prohibited

Caution To set memory size, set IMS and then IXS. Set memory size so that the internal ROM area and internal expansion RAM area do not overlap.

Table 27-2. Internal Expansion RAM Size Switching Register Settings

48-pin products of 78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2	IXS Setting
μPD78F0511, 78F0511A	μPD78F0521, 78F0521A	μPD78F0531, 78F0531A	–	0CH
μPD78F0512, 78F0512A	μPD78F0522, 78F0522A	μPD78F0532, 78F0532A	–	0CH
μPD78F0513, 78F0513A	μPD78F0523, 78F0523A	μPD78F0533, 78F0533A	–	0CH
μPD78F0514, 78F0514A	μPD78F0524, 78F0524A	μPD78F0534, 78F0534A	μPD78F0544, 78F0544A	0AH
μPD78F0515, 78F0515A, 78F0515D[Note], 78F0515DA[Note]	μPD78F0525, 78F0525A	μPD78F0535, 78F0535A	μPD78F0545, 78F0545A	08H
–	μPD78F0526, 78F0526A	μPD78F0536, 78F0536A	μPD78F0546, 78F0546A	04H
–	μPD78F0527, 78F0527A, 78F0527D[Note], 78F0527DA[Note]	μPD78F0537, 78F0537A, 78F0537D[Note], 78F0537DA[Note]	μPD78F0547, 78F0547A, 78F0547D[Note], 78F0547DA[Note]	00H

Note The internal expansion RAM capacity of the products with the on-chip debug function can be debugged according to the debug target products. Set IXS according to the debug target products.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

(2) Serial interface

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

(a) UART6 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(c) IIC0

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{SCL}		0	100	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7	–	0.6	–	μs
Hold time[Note 1]	$t_{HD:STA}$		4.0	–	0.6	–	μs
Hold time when SCL0 = "L"	t_{LOW}	Internal clock operation	4.7	–	1.3	–	μs
		EXSCL0 clock (6.4 MHz) operation	4.7	–	1.25	–	μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0	–	0.6	–	μs
Data setup time (reception)	$t_{SU:DAT}$		250	–	100	–	ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	$f_W = f_{XH}/2^N$ or $f_W = f_{EXSCL0}$ selected[Note 3]	0	3.45	0	0.9[Note 4]	μs
						1.00[Note 5]	
		$f_W = f_{RH}/2^N$ selected[Note 3]	0	3.45	0	1.05	μs
Setup time of stop condition	$t_{SU:STO}$		4.0	–	0.6	–	μs
Bus free time	t_{BUF}		4.7	–	1.3	–	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. f_W indicates the IIC0 transfer clock selected by the IICCL and IICX0 registers.

4. When $f_W \geq 4.4$ MHz is selected

5. When $f_W < 4.4$ MHz is selected

(2) Non-port functions

Port		78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
		30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Power supply, ground		V_{DD}, EV_{DD}[Note 1], V_{SS}, EV_{SS}[Note 1], AV_{REF}, AV_{SS}	V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, V_{SS}, EV_{SS}, AV_{REF}, AV_{SS}	
Regulator		REGC						
Reset		$\overline{\text{RESET}}$						
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK, EXCLKS					
Writing to flash memory		FLMD0						
Interrupt		INTP0 to INTP5			INTP0 to INTP6		INTP0 to INTP7	
Key interrupt		–	KR0, KR1	KR0 to KR3		KR0 to KR7		
Timer	TM00	TI000, TI010, TO00						
	TM01	–					TI001[Note 2], TI011[Note 2], TO01[Note 2]	
	TM50	TI50, TO50						
	TM51	TI51, TO51						
	TMH0	TOH0						
	TMH1	TOH1						
Serial interface	UART0	RxD0, TxD0						
	UART6	RxD6, TxD6						
	IIC0	SCL0, SDA0	SCL0, SDA0, EXSCL0					
	CSI10	$\overline{\text{SCK10}}$, SI10, SO10						
	CSI11	–					$\overline{\text{SCK11}}$[Note 2], SI11[Note 2], SO11[Note 2], $\overline{\text{SSI11}}$[Note 2]	
	CSIA0	–						$\overline{\text{SCKA0}}$, SIA0, SOA0, BUSY0, STB0
A/D converter		ANI0 to ANI3	ANI0 to ANI5	ANI0 to ANI7				
Clock output		–			PCL			
Buzzer output		–					BUZ	
Low-voltage detector (LVI)		EXLVI						

Notes 1. This is not mounted onto 30-pin products.

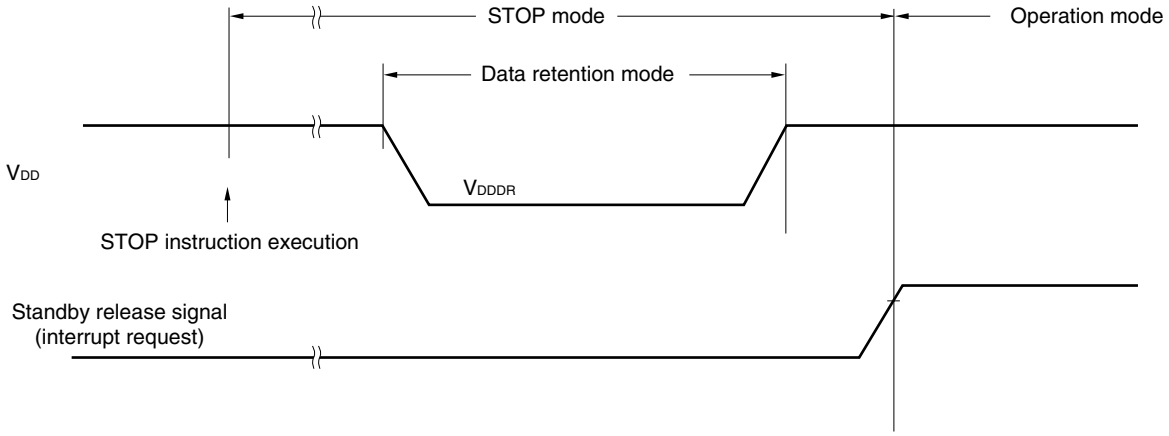
2. This is not mounted onto the 78K0/KE2 products whose flash memory is less than 32 KB.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +125°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



(2/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 4	Soft	Memory bank switching function (products whose flash memory is at least 96 KB only)	BANK: Memory bank select register	Be sure to change the value of the BANK register in the common area (0000H to 7FFFH). If the value of the BANK register is changed in the bank area (8000H to BFFFH), an inadvertent program loop occurs in the CPU. Therefore, never change the value of the BANK register in the bank area.	p. 150 ☐
			Memory bank	Instructions cannot be fetched between different memory banks.	p. 151 ☐
				Branching and accessing cannot be directly executed between different memory banks. Execute branching or accessing between different memory banks via the common area.	p. 151 ☐
				Allocate interrupt servicing in the common area.	p. 151 ☐
				An instruction that extends from 7FFFH to 8000H can only be executed in memory bank 0.	p. 151 ☐
Chapter 5	Soft	Port function	P02/SO11, P04/$\overline{\text{SCK11}}$	To use P02/SO11 and P04/$\overline{\text{SCK11}}$ as general-purpose ports, set serial operation mode register 11 (CSIM11) and serial clock selection register 11 (CSIC11) to the default status (00H).	p. 164 ☐
			P10/$\overline{\text{SCK10}}$/TxD0, P12/SO10	To use P10/$\overline{\text{SCK10}}$/TxD0 and P12/SO10 as general-purpose ports, set serial operation mode register 10 (CSIM10) and serial clock selection register 10 (CSIC10) to the default status (00H)	p. 175 ☐
			P13/TxD6	To use P13/TxD6 as general-purpose port, clear bit 0 (TXDLV6) of synchronous serial interface control register 6 (ASICL6) to 0 (normal output of TxD6).	p. 175 ☐
	Hard		Port 2	Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.	p. 181 ☐
	Soft			For the 38-pin products of 78K0/KC2, be sure to set bits 6 and 7 of PM2 to “1”, and bits 6 and 7 of P2 to “0”.	p. 182 ☐
	Hard		P31/INTP2/ OCD1A	In the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA), be sure to pull the P31/INTP2/OCD1A pin down before a reset release, to prevent malfunction.	p. 183 ☐
				Process the P31/INTP2/OCD1A pin of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator (see the table on p.183).	p. 183 ☐
	Soft		Port 4	For the 38-pin products of 78K0/KC2, be sure to set bits 0 and 1 of PM4 and P4 to “0”.	p. 187 ☐
	Hard		P60, P61	A through current flows through P60 and P61 if an intermediate potential is input to these pins, because the input buffer is also turned on when P60 and P61 are in output mode. Consequently, do not input an intermediate potential when P60 and P61 are in output mode.	p. 190 ☐
			P62	A through current flows through P62 if an intermediate potential is input to this pin, because the input buffer is also turned on when P62 is in output mode. Consequently, do not input an intermediate potential when P62 is in output mode.	p. 191 ☐
	Soft		Port 7	For the 38-pin products of 78K0/KC2, be sure to set bits 2 and 3 of PM7 and P7 to “0”.	p. 195 ☐