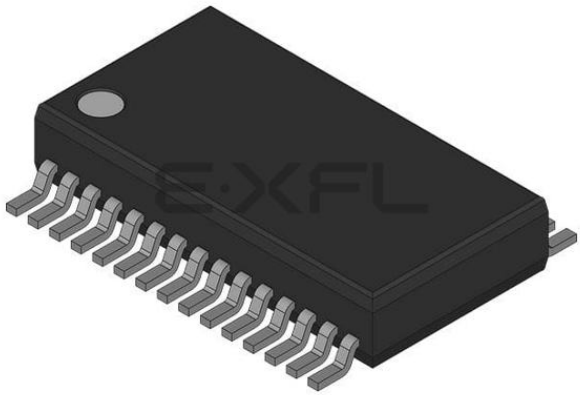
Renesas Electronics America Inc - UPD78F0503AMC-CAB-AX Datasheet



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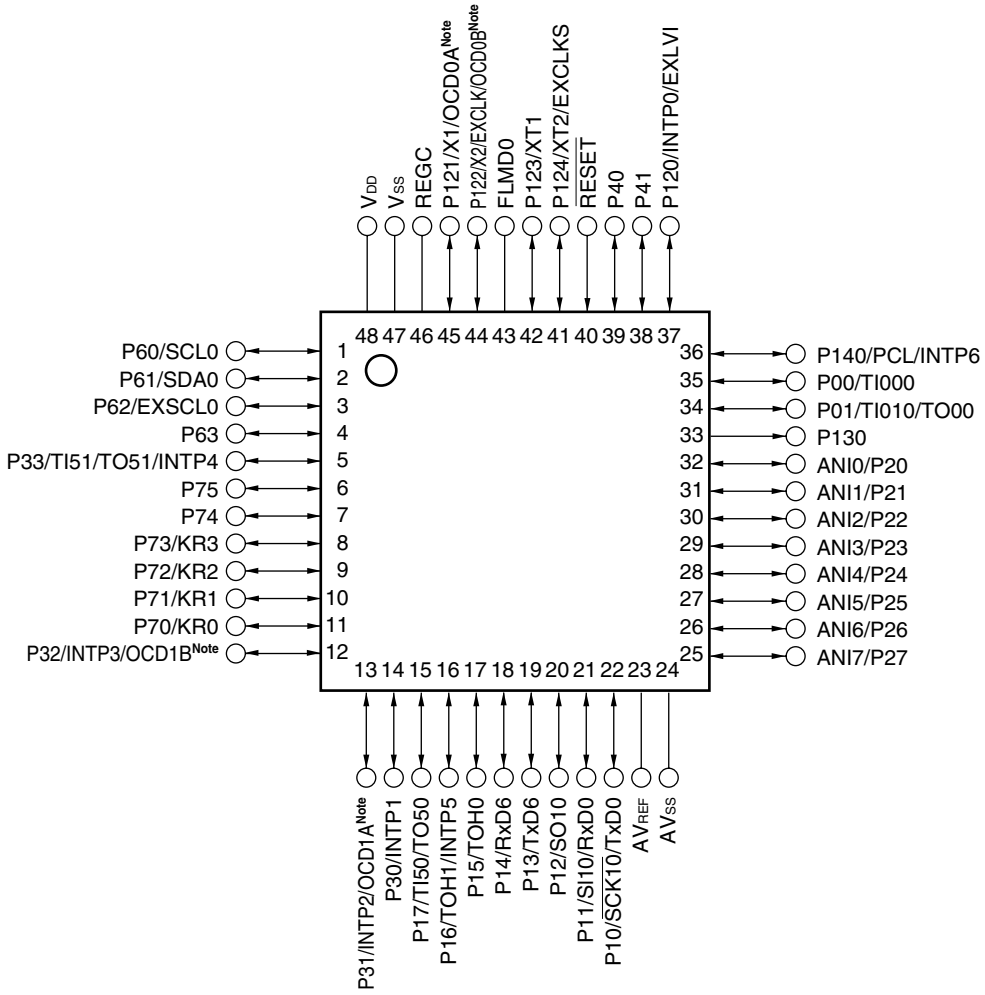
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0503amc-cab-ax

- 48-pin plastic LQFP (fine pitch) (7 × 7)



Note Products with on-chip debug function only

Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

3. ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

Remark For pin identification, see **1.6 Pin Identification**.

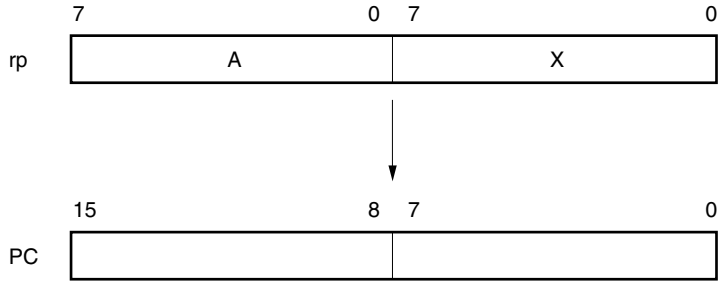
3.3.4 Register addressing

[Function]

Register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

This function is carried out when the BR AX instruction is executed.

[Illustration]



3.4 Operand Address Addressing

The following methods are available to specify the register and memory (addressing) to undergo manipulation during instruction execution.

3.4.1 Implied addressing

[Function]

The register that functions as an accumulator (A and AX) among the general-purpose registers is automatically (implicitly) addressed.

Of the 78K0/Kx2 microcontroller instruction words, the following instructions employ implied addressing.

Instruction	Register to Be Specified by Implied Addressing
MULU	A register for multiplicand and AX register for product storage
DIVUW	AX register for dividend and quotient storage
ADJBA/ADJBS	A register for storage of numeric values that become decimal correction targets
ROR4/ROL4	A register for storage of digit data that undergoes digit rotation

[Operand format]

Because implied addressing can be automatically determined with an instruction, no particular operand format is necessary.

[Description example]

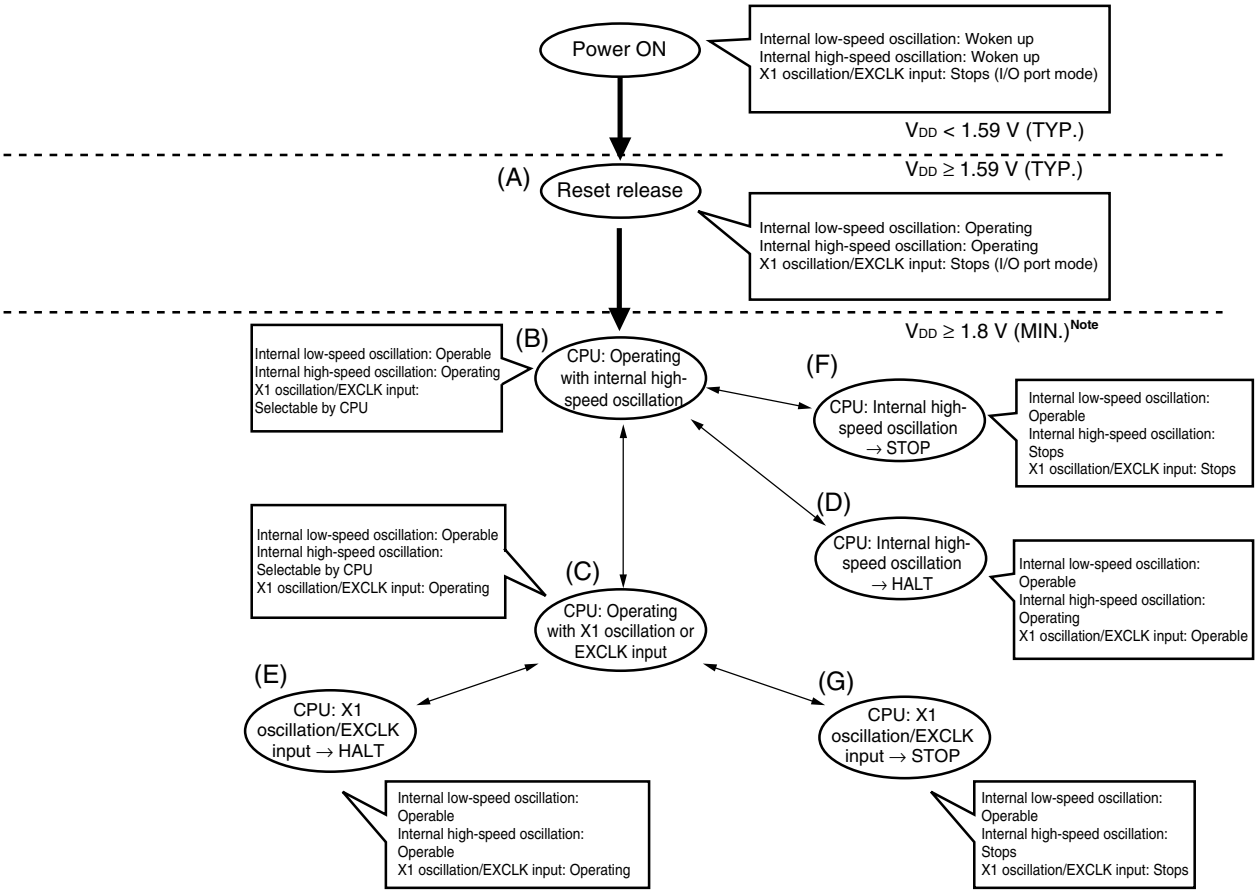
In the case of MULU X

With an 8-bit × 8-bit multiply instruction, the product of the A register and X register is stored in AX. In this example, the A and AX registers are specified by implied addressing.

6.6.6 CPU clock status transition diagram

Figure 6-17 and 6-18 shows the CPU clock status transition diagram of this product.

Figure 6-17. CPU Clock Status Transition Diagram
(When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0), 78K0/KB2)



Note Standard and (A) grade products: 1.8 V,
(A2) grade products: 2.7 V

Remark In the 2.7 V/1.59 V POC mode (option byte: POCMODE = 1), the CPU clock status changes to (A) in the above figure when the supply voltage exceeds 2.7 V (TYP.), and to (B) after reset processing (11 to 45 μs).

7.4.6 PPG output operation

A square wave having a pulse width set in advance by CR01n is output from the TO0n pin as a PPG (Programmable Pulse Generator) signal during a cycle set by CR00n when bits 3 and 2 (TMC0n3 and TMC0n2) of 16-bit timer mode control register 0n (TMC0n) are set to 11 (clear & start upon a match between TM0n and CR00n).

The pulse cycle and duty factor of the pulse generated as the PPG output are as follows.

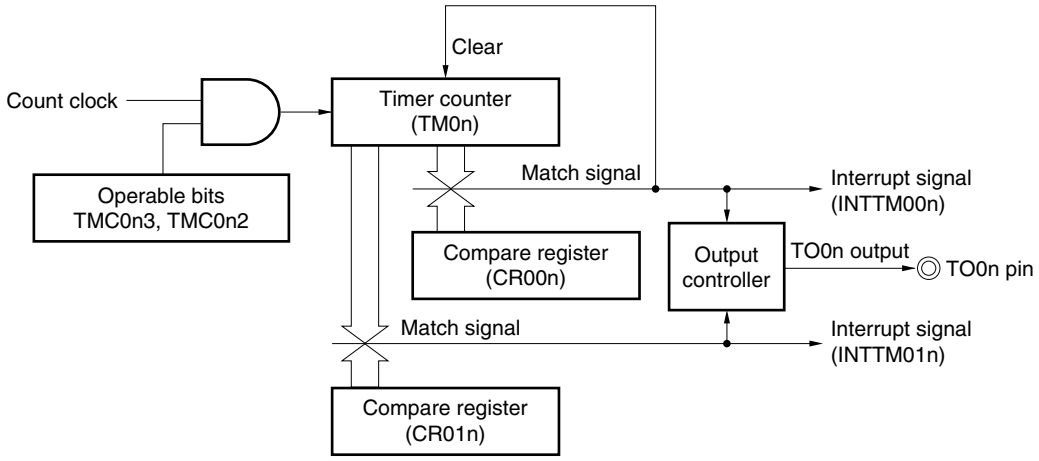
- Pulse cycle = (Set value of CR00n + 1) × Count clock cycle
- Duty = (Set value of CR01n + 1) / (Set value of CR00n + 1)

Caution To change the duty factor (value of CR01n) during operation, see 7.5.1 Rewriting CR01n during TM0n operation.

Remarks 1. For the setting of I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 7-45. Block Diagram of PPG Output Operation



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

8.4.2 Operation as external event counter

The external event counter counts the number of external clock pulses to be input to the TI5n pin by 8-bit timer counter 5n (TM5n).

TM5n is incremented each time the valid edge specified by timer clock selection register 5n (TCL5n) is input. Either the rising or falling edge can be selected.

When the TM5n count value matches the value of 8-bit timer compare register 5n (CR5n), TM5n is cleared to 0 and an interrupt request signal (INTTM5n) is generated.

Whenever the TM5n value matches the value of CR5n, INTTM5n is generated.

Setting

<1> Set each register.

- Set the port mode register (PM17 or PM33)[Note] to 1.
- TCL5n: Select TI5n pin input edge.
  TI5n pin falling edge → TCL5n = 00H
  TI5n pin rising edge → TCL5n = 01H
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on match of TM5n and CR5n, disable the timer F/F inversion operation, disable timer output.
  (TMC5n = 00000000B)

<2> When TCE5n = 1 is set, the number of pulses input from the TI5n pin is counted.

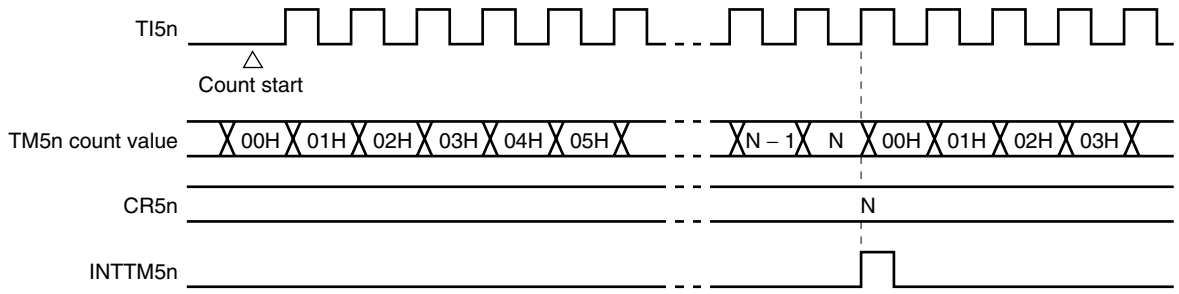
<3> When the values of TM5n and CR5n match, INTTM5n is generated (TM5n is cleared to 00H).

<4> After these settings, INTTM5n is generated each time the values of TM5n and CR5n match.

Note 8-bit timer/event counter 50: PM17
8-bit timer/event counter 51: PM33

Remark For how to enable the INTTM5n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

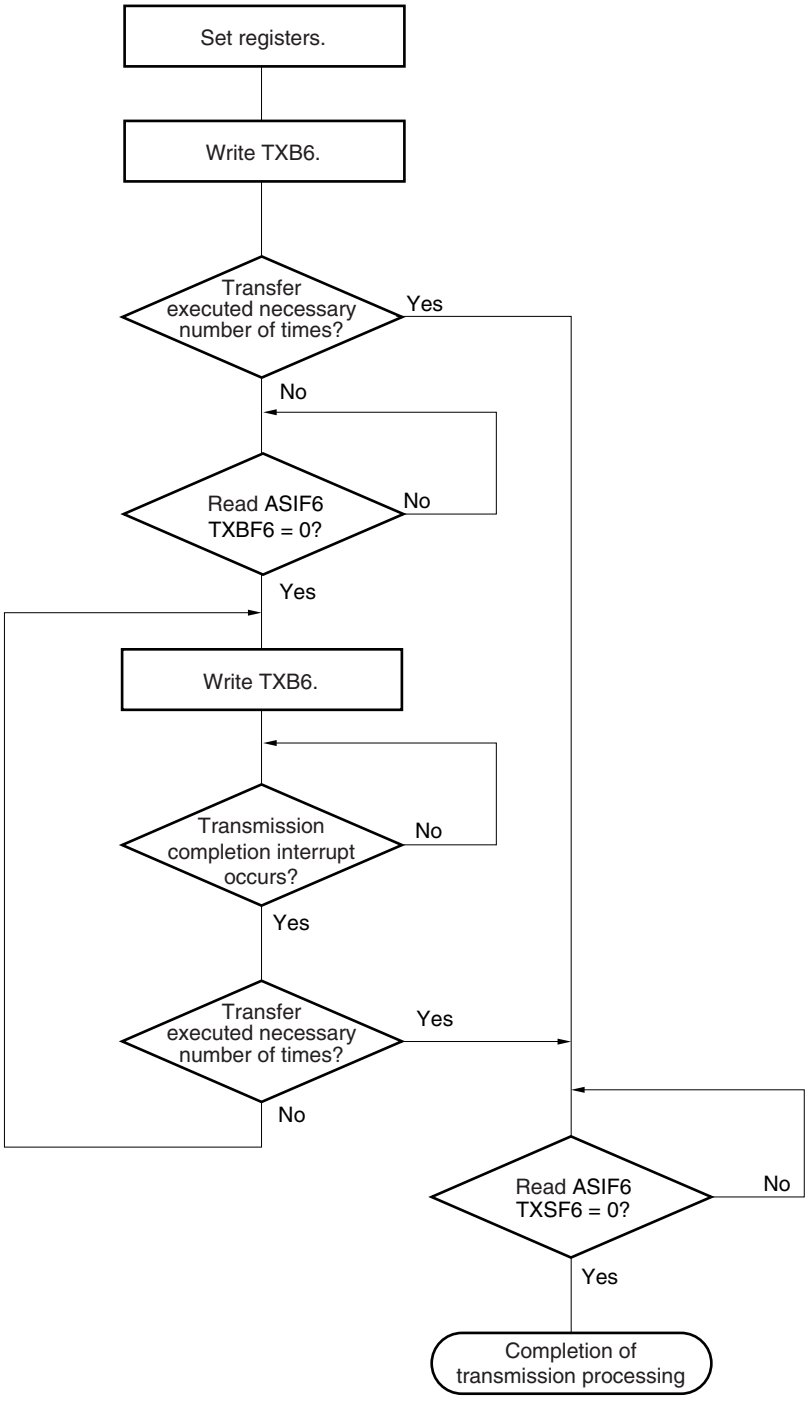
Figure 8-12. External Event Counter Operation Timing (with Rising Edge Specified)



Remark N = 00H to FFH
n = 0, 1

Figure 15-16 shows an example of the continuous transmission processing flow.

Figure 15-16. Example of Continuous Transmission Processing Flow



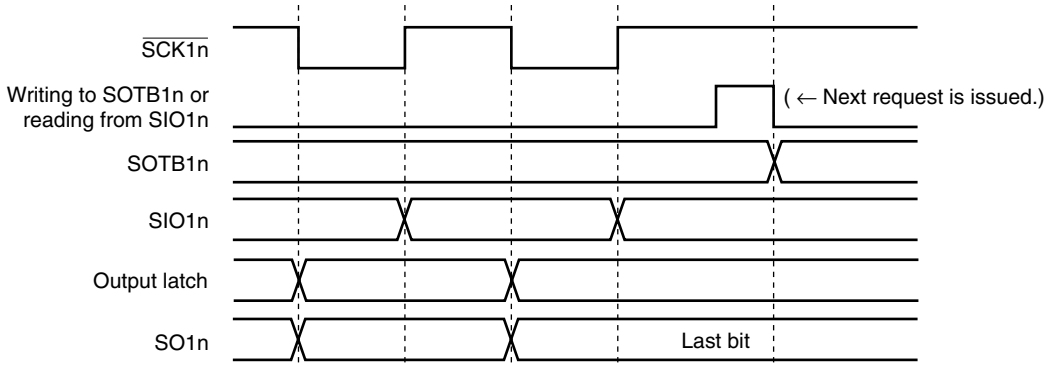
Remark TXB6: Transmit buffer register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6 (transmit buffer data flag)
TXSF6: Bit 0 of ASIF6 (transmit shift register data flag)

(4) Output value of SO1n pin (last bit)

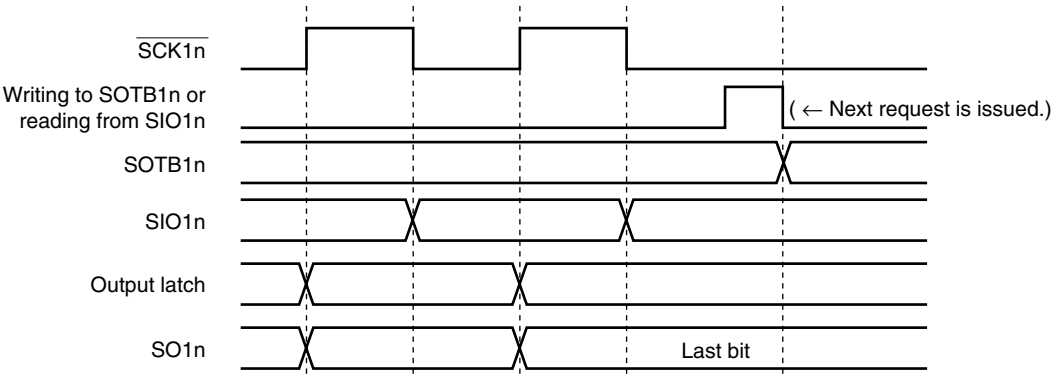
After communication has been completed, the SO1n pin holds the output value of the last bit.

Figure 16-12. Output Value of SO1n Pin (Last Bit) (1/2)

(a) Type 1: CKP1n = 0, DAP1n = 0



(b) Type 3: CKP1n = 1, DAP1n = 0



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

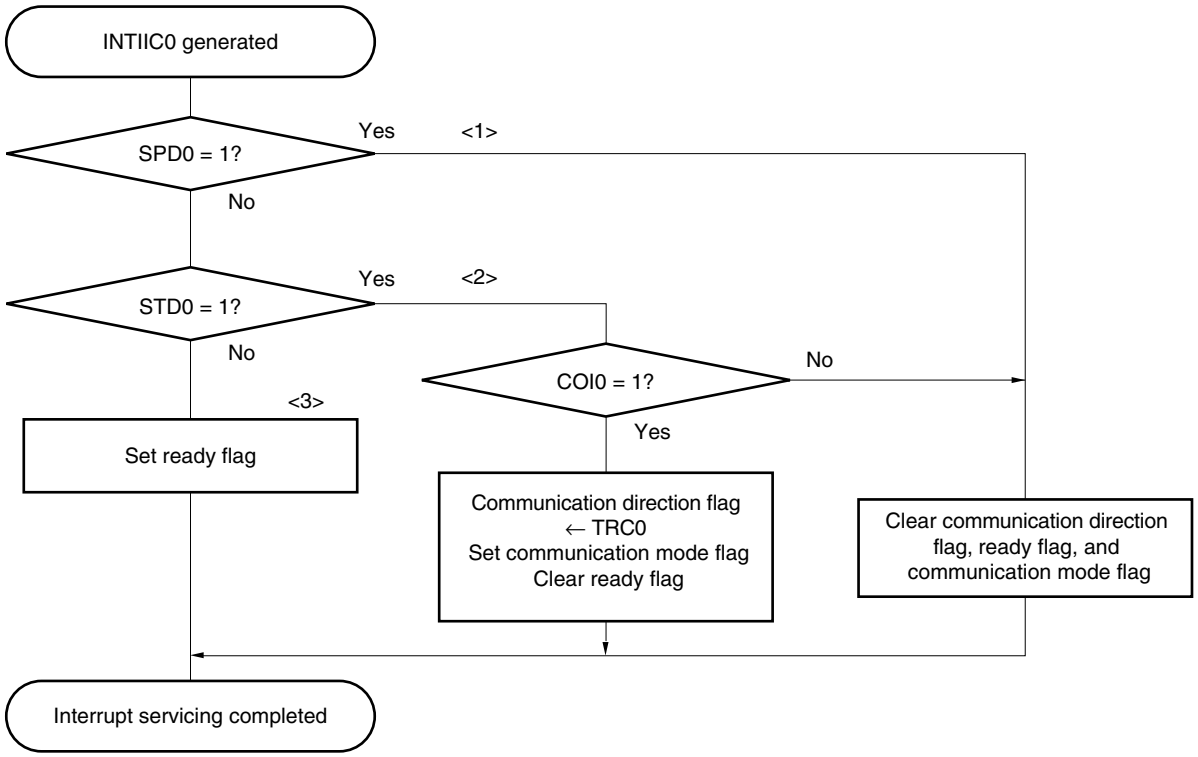
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

An example of the processing procedure of the slave with the INTIIC0 interrupt is explained below (processing is performed assuming that no extension code is used). The INTIIC0 interrupt checks the status, and the following operations are performed.

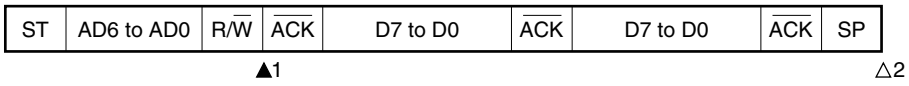
<1> Communication is stopped if the stop condition is issued.
<2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
<3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I^2C bus remaining in the wait state.

Remark <1> to <3> above correspond to <1> to <3> in **Figure 18-26 Slave Operation Flowchart (2)**.

Figure 18-26. Slave Operation Flowchart (2)



(b) When arbitration loss occurs during transmission of extension code



▲1: IICS0 = 0110×010B

Sets LREL0 = 1 by software

△2: IICS0 = 00000001B

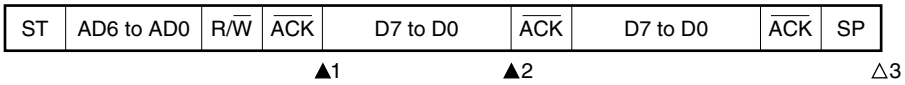
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(c) When arbitration loss occurs during transmission of data

(i) When WTIM0 = 0



▲1: IICS0 = 10001110B

▲2: IICS0 = 01000000B

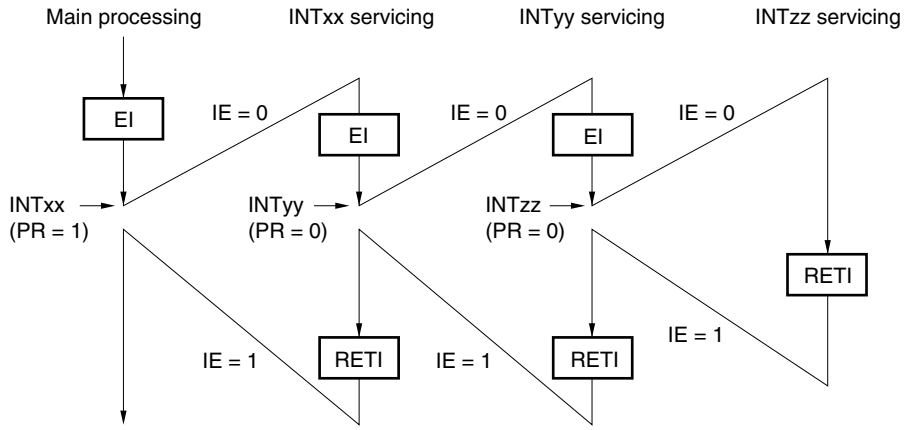
△3: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

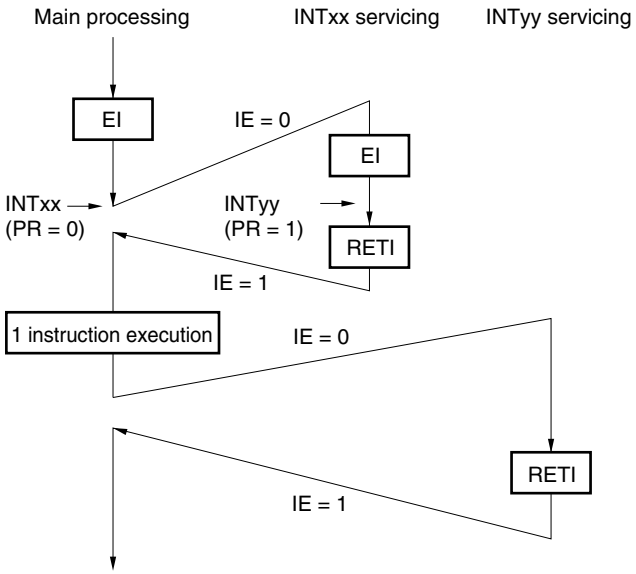
Figure 20-22. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control



Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
PR = 1: Lower priority level
IE = 0: Interrupt request acknowledgment disabled

Table 22-2. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	HALT mode held
Reset	–	–	×	×	Reset processing

×: don't care

22.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

Caution Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

The operating statuses in the STOP mode are shown below.

Figure 24-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source

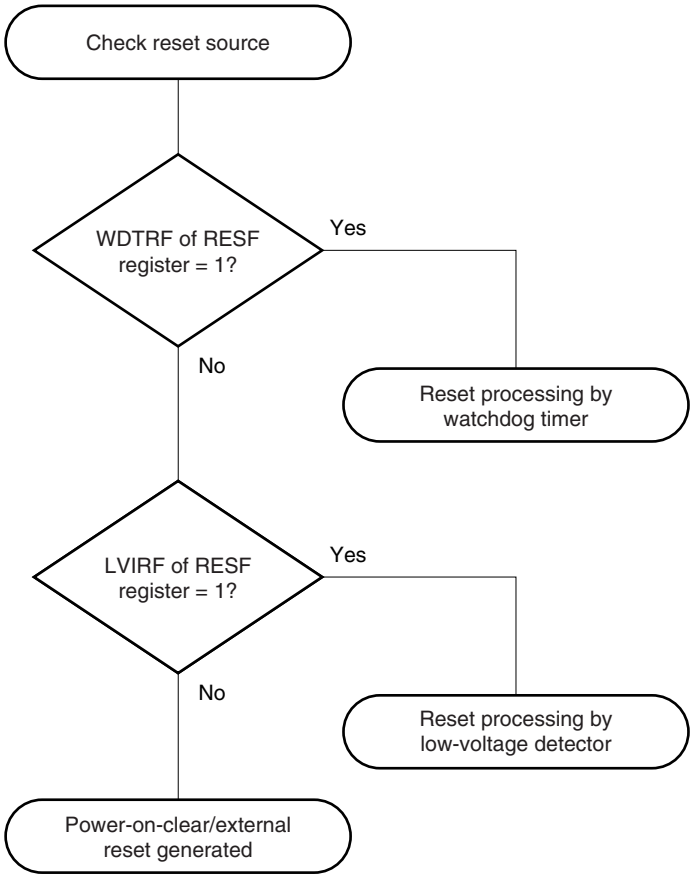
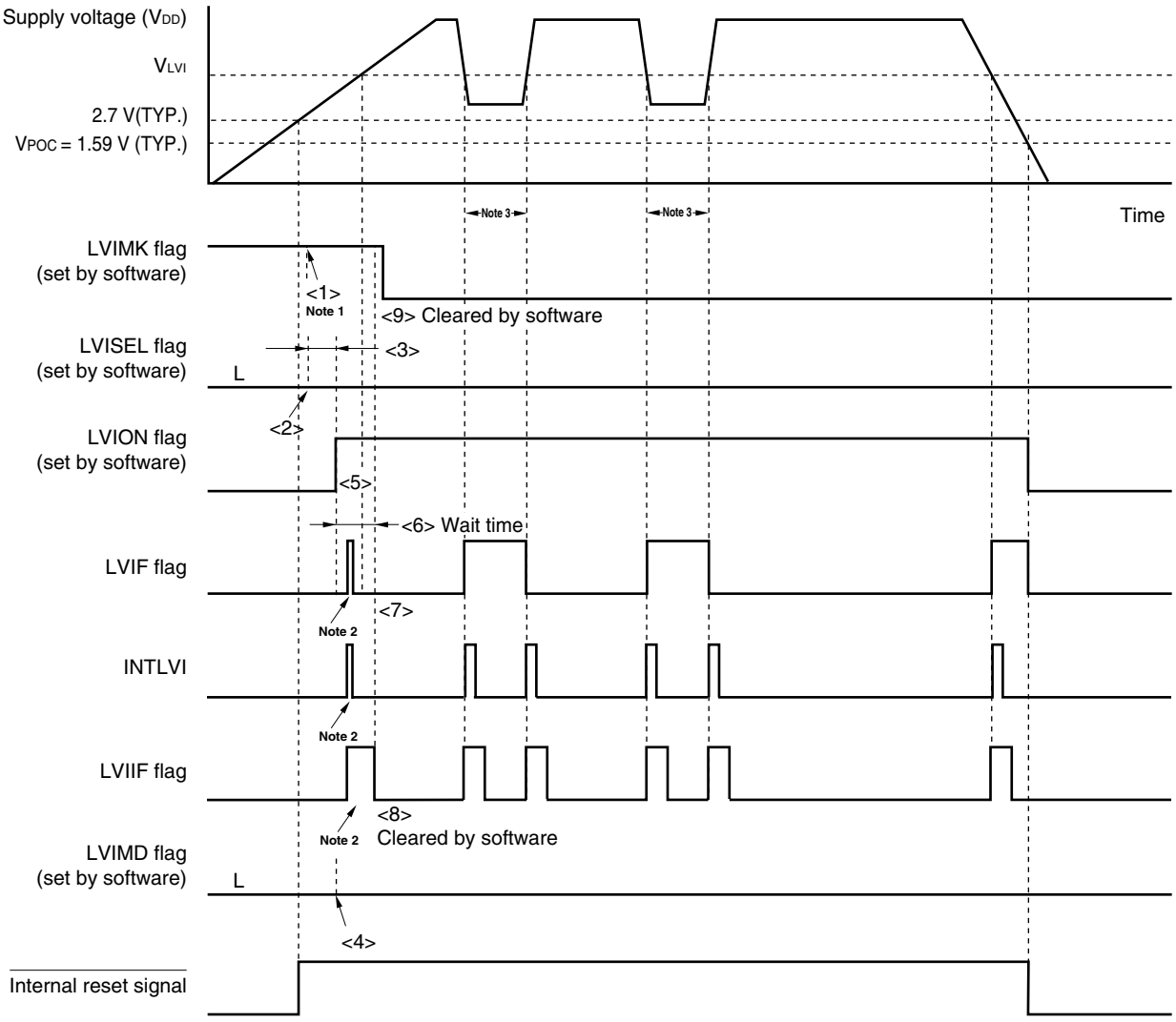


Figure 25-7. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage (V_{DD})) (2/2)

(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

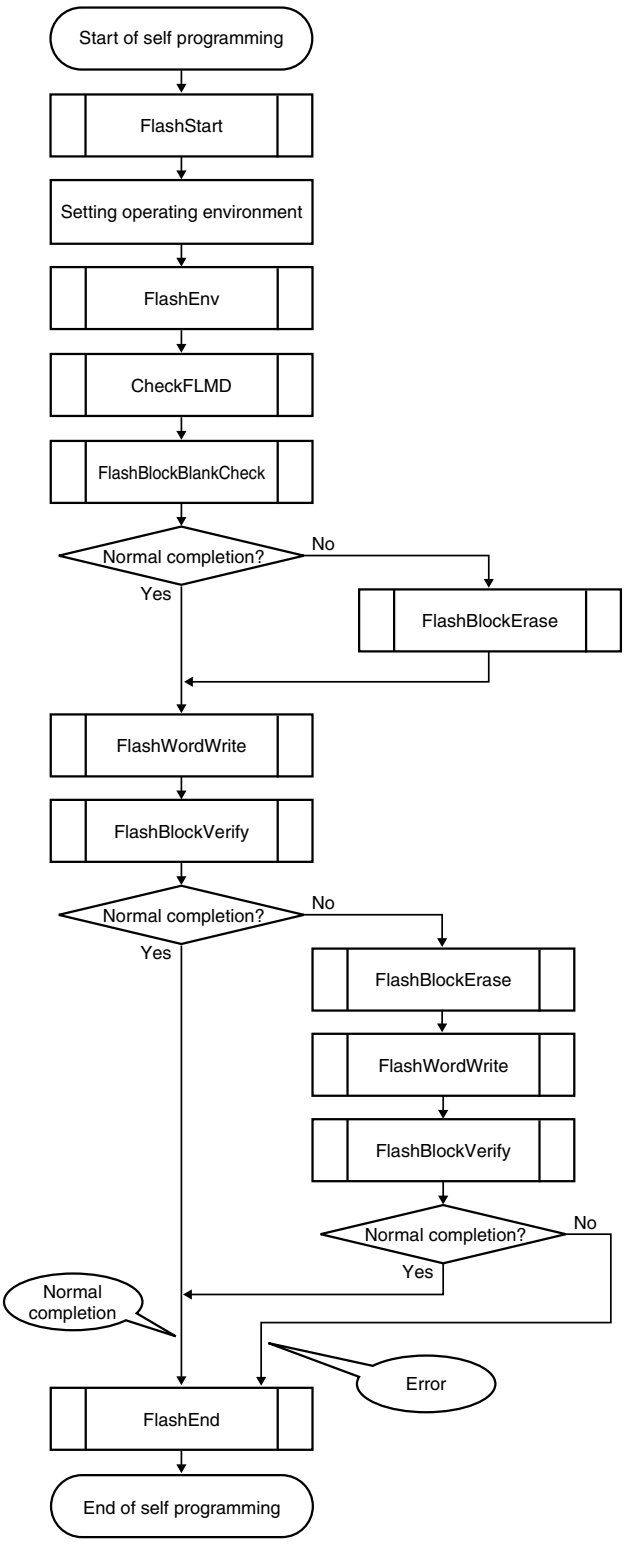
2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

Remark <1> to <9> in Figure 25-7 above correspond to <1> to <9> in the description of "When starting operation" in **25.4.2 (1) When detecting level of supply voltage (V_{DD})**.

The following figure illustrates a flow of rewriting the flash memory by using a self-programming library.

Figure 27-14. Flow of Self Programming (Rewriting Flash Memory)



Remark For details of the self-programming library, refer to **78K0 Microcontrollers Self Programming Library Type01 User's Manual (U18274E)**.

Table 27-13. Processing Time for Self Programming Library
(Conventional-specification Products (μPD78F05xx and 78F05xxD)) (2/4)

(2) When internal high-speed oscillation clock is used and entry RAM is located in short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		4.25			
Initialize library		443.5			
Mode check library		219.625		218.875	
Block blank check library		12236.625		12231.625	
Block erase library		36363.25	355771.75	36358.25	355750
Word write library		679.75 (680.125)	1874.75 (1875.125)	672.75 (673.125)	1867.75 (1868.125)
Block verify library		25072.625		25067.625	
Self programming end library		4.25			
Get information library	Option value: 03H	337 (337.125)		331.75 (331.875)	
	Option value: 04H	329.125 (239.25)		323.875 (324)	
	Option value: 05H	502.25 (503.125)		497 (497.875)	
Set information library		104978.5	541143.125	104977.5	541142.125
EEPROM write library		962.25 (962.625)	2157.25 (2157.625)	955.25 (955.625)	2150.25 (2150.625)

Remarks 1. Values in parentheses indicate values when a write start address structure is located other than in the internal high-speed RAM.

2. The above processing times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit data transfer	**MOVW**	rp, #word	3	6	–	rp ← word	
		saddrp, #word	4	8	10	(saddrp) ← word	
		sfrp, #word	4	–	10	sfrp ← word	
		AX, saddrp	2	6	8	AX ← (saddrp)	
		saddrp, AX	2	6	8	(saddrp) ← AX	
		AX, sfrp	2	–	8	AX ← sfrp	
		sfrp, AX	2	–	8	sfrp ← AX	
		AX, rp Note 3	1	4	–	AX ← rp	
		rp, AX Note 3	1	4	–	rp ← AX	
		AX, !addr16	3	10	12	AX ← (addr16)	
		!addr16, AX	3	10	12	(addr16) ← AX	
	XCHW	AX, rp Note 3	1	4	–	AX ↔ rp	
8-bit operation	**ADD**	A, #byte	2	4	–	A, CY ← A + byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r	× × ×
		r, A	2	4	–	r, CY ← r + A	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL)	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B)	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C)	× × ×
	ADDC	A, #byte	2	4	–	A, CY ← A + byte + CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte + CY	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r + CY	× × ×
		r, A	2	4	–	r, CY ← r + A + CY	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr) + CY	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16) + C	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL) + CY	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte) + CY	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B) + CY	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C) + CY	× × ×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Only when rp = BC, DE or HL

4. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

DC Characteristics (4/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		3.2	5.5	mA
				Resonator connection		4.5	6.9	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		1.6	2.8	mA
				Resonator connection		2.3	3.9	mA
			f_{XH} = 10 MHz V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		1.5	2.7	mA
				Resonator connection		2.2	3.2	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.9	1.6	mA
				Resonator connection		1.3	2.0	mA
			f_{XH} = 5 MHz, V_{DD} = 2.0 V [Notes 2, 3]	Square wave input		0.7	1.4	mA
				Resonator connection		1.0	1.6	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			1.4	2.5	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		6	30	μA
				Resonator connection		15	35	μA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		0.8	2.6	mA
				Resonator connection		2.0	4.4	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		0.4	1.3	mA
				Resonator connection		1.0	2.4	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.2	0.65	mA
				Resonator connection		0.5	1.1	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			0.4	1.2	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		3.0	27	μA
				Resonator connection		12	32	μA
	I_{DD3}[Note 6]	STOP mode				1	20	μA
			T_A = −40 to +70 °C			1	10	μA
A/D converter operating current	I_{ADC}[Note 7]	2.3 V ≤ AV_{REF} ≤ V_{DD}, ADCS = 1				0.86	1.9	mA
Watchdog timer operating current	I_{WDT}[Note 8]	During 240 kHz internal low-speed oscillation clock operation				5	10	μA
LVI operating current	I_{LVI}[Note 9]					9	18	μA

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or external subsystem clock frequency)

(Notes on next page)

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

- **Basic characteristics**

Parameter		Symbol	Conditions				MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}	f_{XP} = 10 MHz (TYP.), 20 MHz (MAX.)					4.5	11.0	mA
Erase time Notes 1, 2	All block	T_{eraca}						20	200	ms
	Block unit	T_{erasa}						20	200	ms
Write time (in 8-bit units) Note 1		T_{wrwa}						10	100	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite Note 3	Expanded-specification Products (μPD78F05xxA (A))	• When a flash memory programmer is used, and the libraries Note 4 provided by Renesas Electronics are used • For program update	Retention: 15 years	1000			Times
					• When the EEPROM emulation libraries Note 5 provided by Renesas Electronics are used • The rewritable ROM size: 4 KB • For data update	Retention: 5 years	10000			Times
				Expanded-specification Products (μPD78F05xxA (A))	Conditions other than the above Note 6	Retention: 10 years	100			Times
				Conventional-specification Products (μPD78F05xx (A))						

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP4 or PG-FP5, is used and the rewrite time during self programming, see **Tables 27-12** to **27-14**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

4. The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) is excluded.

5. The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) is excluded.

6. These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) and the sample program specified by **the 78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) are used.

Remarks 1. f_{XP}: Main system clock oscillation frequency

2. For serial write operation characteristics, refer to **78K0/Kx2 Flash Memory Programming (Programmer) Application Note (**Document No.: **U17739E)**.

Table 35-2. Soldering Conditions of Expanded-specification products (μPD78F05xxA and 78F05xxDA) (2/2)

(3) 30-pin plastic SSOP (7.62 mm (300))
μPD78F050xAMC-CAB-AX (x = 0 to 3), 78F0503DAMC-CAB-AX
μPD78F050xAMCA-CAB-G (x = 0 to 3), 78F050xAMCA2-CAB-G (x = 0 to 3)
38-pin plastic SSOP (7.62 mm (300))
μPD78F051xAMC-GAA-AX (x = 1 to 3), 78F0513DAMC-GAA-AX
μPD78F051xAMCA-GAA-G (x = 1 to 3), 78F051xAMCA2-GAA-G (x = 1 to 3)
44-pin plastic LQFP (10x10)
μPD78F051xAGB-GAF-AX (x = 1 to 3), 78F0513DAGB-GAF-AX
μPD78F05x1AGBA-GAF-G (x = 1 to 3), 78F051xAGBA2-GAF-G (x = 1 to 3)
52-pin plastic LQFP (10x10)
μPD78F052xAGB-GAG-AX (x = 1 to 7), 78F0527DAGB-GAG-AX
μPD78F052xAGBA-GAG-G (x = 1 to 7), 78F052xAGBA2-GAG-G (x = 1 to 7)
64-pin plastic LQFP (14x14)
μPD78F053xAGC-GAL-AX (x = 1 to 7), 78F0537DAGC-GAL-AX
μPD78F053xAGCA-GAL-G (x = 1 to 7), 78F053xAGCA2-GAL-G (x = 1 to 7)
64-pin plastic LQFP (12x12)
μPD78F053xAGK-GAJ-AX (x = 1 to 7), 78F0537DAGK-GAJ-AX
μPD78F053xAGKA-GAJ-G (x = 1 to 7), 78F053xAGKA2-GAJ-G (x = 1 to 7)
80-pin plastic LQFP (14x14)
μPD78F054xAGC-GAD-G (x = 4 to 7), 78F0547DAGC-GAD-AX
μPD78F054xAGCA-GAD-G (x = 4 to 7), 78F054xAGCA2-GAD-G (x = 4 to 7)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR60-107-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	WS60-107-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Cautions 1. Do not use different soldering methods together (except for partial heating).
2. The μPD78F05xxDA has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Remarks 1. The QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Download the software for operating the QB-MINI2 from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html) when using the QB-MINI2.

2. The packed contents of QB-78K0KX2 differ depending on the part number, as follows.

Packed Contents / Part Number	In-Circuit Emulator	Emulation Probe	Exchange Adapter	YQ Connector	Target Connector
QB-78K0KX2-ZZZ	QB-78K0KX2	None			
QB-78K0KX2-T30MC		QB-80-EP-01T	QB-30MC-EA-02T	QB-30MC-YQ-01T	QB-30MC-NQ-01T
QB-78K0KX2-T36FC			QB-36FC-EA-01T	None	QB-36FC-NQ-01T
QB-78K0KX2-T38MC			QB-38MC-EA-01T	QB-38MC-YQ-01T	QB-38MC-NQ-01T
QB-78K0KX2-T44GB			QB-44GB-EA-03T	QB-44GB-YQ-01T	QB-44GB-NQ-01T
QB-78K0KX2-T48GA			QB-48GA-EA-02T	QB-48GA-YQ-01T	QB-48GA-NQ-01T
QB-78K0KX2-T52GB			QB-52GB-EA-02T	QB-52GB-YQ-01T	QB-52GB-NQ-01T
QB-78K0KX2-T64GB			QB-64GB-EA-04T	QB-64GB-YQ-01T	QB-64GB-NQ-01T
QB-78K0KX2-T64GC			QB-64GC-EA-03T	QB-64GC-YQ-01T	QB-64GC-NQ-01T
QB-78K0KX2-T64GK			QB-64GK-EA-04T	QB-64GK-YQ-01T	QB-64GK-NQ-01T
QB-78K0KX2-T64GA			QB-64GA-EA-01T	QB-64GA-YQ-01T	QB-64GA-NQ-01T
QB-78K0KX2-T64FC			QB-64FC-EA-01T	None	QB-64FC-NQ-01T
QB-78K0KX2-T80GC			QB-80GC-EA-01T	QB-80GC-YQ-01T	QB-80GC-NQ-01T
QB-78K0KX2-T80GK			QB-80GK-EA-01T	QB-80GK-YQ-01T	QB-80GK-NQ-01T

Note Under development

A.4.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This on-chip debug emulator serves to debug hardware and software when developing application systems using the 78K0/Kx2. It is available also as flash memory programmer dedicated to microcontrollers with on-chip flash memory. When using this as on-chip debug emulator, it should be used in combination with a connection cable (10-pin cable or 16-pin cable), a USB interface cable that is used to connect the host machine, and the 78K0-OCD board.
Target connector specifications	10-pin general-purpose connector (2.54 mm pitch) or 16-pin general-purpose connector (2.54 mm pitch)

Remarks 1. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. A connection cable (10-pin cable) and the 78K0-OCD board are used only when using the on-chip debug function.

2. Download the software for operating the QB-MINI2 from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).