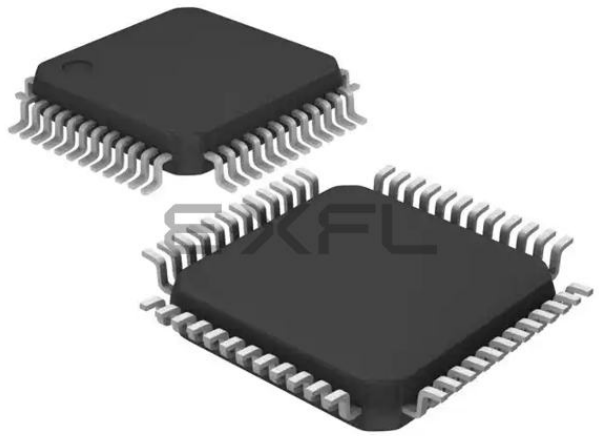
Renesas Electronics America Inc - UPD78F0511AGA-GAM-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0511aga-gam-ax

1.1.3 Time Instruction cycle, peripheral hardware clock frequency, external main system clock frequency, external main system clock input high-level width, and external main system clock input low-level width (AC characteristics)

(1) Conventional-specification products (μPD78F05xx and 78F05xxD)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	4.0 V ≤ V_{DD} ≤ 5.5 V	0.1		32	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.2		32	μs
			1.8 V ≤ V_{DD} < 2.7 V Note 1	0.4 Note 3		32	μs
		Subsystem clock (f_{SUB}) operation Note 2		114	122	125	μs
Peripheral hardware clock frequency	f_{PRS}	f_{PRS} = f_{XH} (XSEL = 1)	4.0 V ≤ V_{DD} ≤ 5.5 V			20	MHz
			2.7 V ≤ V_{DD} < 4.0 V			10	MHz
			1.8 V ≤ V_{DD} < 2.7 V Note 1			5	MHz
		f_{PRS} = f_{RH} (XSEL = 0)	2.7 V ≤ V_{DD} ≤ 5.5 V	7.6		8.4	MHz
			1.8 V ≤ V_{DD} < 2.7 V Notes 1, 5	7.6		10.4	MHz
External main system clock frequency	f_{EXCLK}	4.0 V ≤ V_{DD} ≤ 5.5 V		1.0 Note 6		20.0	MHz
		2.7 V ≤ V_{DD} < 4.0 V		1.0 Note 6		10.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V Note 1		1.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXCLKH}, t_{EXCLKL}	4.0 V ≤ V_{DD} ≤ 5.5 V		24			ns
		2.7 V ≤ V_{DD} < 4.0 V		48			ns
		1.8 V ≤ V_{DD} < 2.7 V Note 1		96			ns

(2) Expanded-specification products (μPD78F05xxA and 78F05xxDA)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.1		32	μs
			1.8 V ≤ V_{DD} < 2.7 V Note 1	0.4 Note 3		32	μs
		Subsystem clock (f_{SUB}) operation Note 2		114	122	125	μs
Peripheral hardware clock frequency	f_{PRS}	f_{PRS} = f_{XH} (XSEL = 1)	4.0 V ≤ V_{DD} ≤ 5.5 V			20	MHz
			2.7 V ≤ V_{DD} < 4.0 V Note 4			20	MHz
			1.8 V ≤ V_{DD} < 2.7 V Note 1			5	MHz
		f_{PRS} = f_{RH} (XSEL = 0)	2.7 V ≤ V_{DD} ≤ 5.5 V	7.6		8.4	MHz
			1.8 V ≤ V_{DD} < 2.7 V Notes 1, 5	7.6		10.4	MHz
External main system clock frequency	f_{EXCLK}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.0 Note 6		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V Note 1		1.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXCLKH}, t_{EXCLKL}	2.7 V ≤ V_{DD} ≤ 5.5 V		24			ns
		1.8 V ≤ V_{DD} < 2.7 V Note 1		96			ns

Notes 1. Standard and (A) grade products only

2. The 78K0/KB2 is not provided with a subsystem clock.

3. 0.38 μs when operating with the 8 MHz internal oscillator.

4. Characteristics of the main system clock frequency. Set the division clock to be set by a peripheral function to f_{XH}/2 (10 MHz) or less. The multiplier/divider, however, can operate on f_{XH} (20 MHz).

5. Characteristics of the main system clock frequency. Set the division clock to be set by a peripheral function to f_{RH}/2 or less.

6. 2.0 MHz (MIN.) when using UART6 during on-board programming.

(3/6)

78K0/Kx2 Microcontrollers	Package	Product type	Quality grace	Part Number
78K0/KE2	64-pin plastic LQFP (fine pitch) (10x10)	Conventional-specification products	Standard products	μPD78F0531GB-UEU-A, 78F0532GB-UEU-A, 78F0533GB-UEU-A, 78F0534GB-UEU-A, 78F0535GB-UEU-A, 78F0536GB-UEU-A, 78F0537GB-UEU-A, 78F0537DGB-UEU-A[Note]
			(A) grade products	μPD78F0531GB(A)-GAH-AX, 78F0532GB(A)-GAH-AX, 78F0533GB(A)-GAH-AX, 78F0534GB(A)-GAH-AX, 78F0535GB(A)-GAH-AX, 78F0536GB(A)-GAH-AX, 78F0537GB(A)-GAH-AX
			(A2) grade products	μPD78F0531GB(A2)-GAH-AX, 78F0532GB(A2)-GAH-AX, 78F0533GB(A2)-GAH-AX, 78F0534GB(A2)-GAH-AX, 78F0535GB(A2)-GAH-AX, 78F0536GB(A2)-GAH-AX, 78F0537GB(A2)-GAH-AX
		Expanded-specification products	Standard products	μPD78F0531AGB-GAH-AX, 78F0532AGB-GAH-AX, 78F0533AGB-GAH-AX, 78F0534AGB-GAH-AX, 78F0535AGB-GAH-AX, 78F0536AGB-GAH-AX, 78F0537AGB-GAH-AX, 78F0537DAGB-GAH-AX[Note]
			(A) grade products	μPD78F0531AGBA-GAH-G, 78F0532AGBA-GAH-G, 78F0533AGBA-GAH-G, 78F0534AGBA-GAH-G, 78F0535AGBA-GAH-G, 78F0536AGBA-GAH-G, 78F0537AGBA-GAH-G
			(A2) grade products	μPD78F0531AGBA2-GAH-G, 78F0532AGBA2-GAH-G, 78F0533AGBA2-GAH-G, 78F0534AGBA2-GAH-G, 78F0535AGBA2-GAH-G, 78F0536AGBA2-GAH-G, 78F0537AGBA2-GAH-G

Note The μPD78F0537D and 78F0537DA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call and return instructions are executed or the register is saved/reset upon generation of an interrupt request.

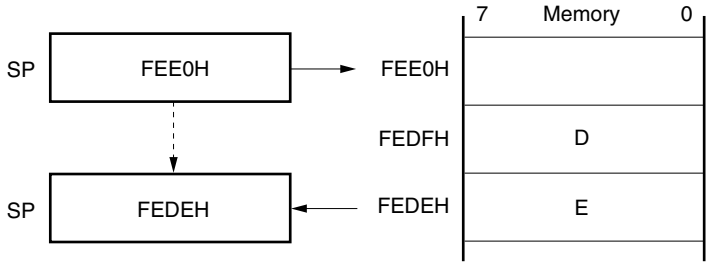
With stack addressing, only the internal high-speed RAM area can be accessed.

[Description example]

PUSH DE; when saving DE register

Operation code	1	0	1	1	0	1	0	1

[Illustration]

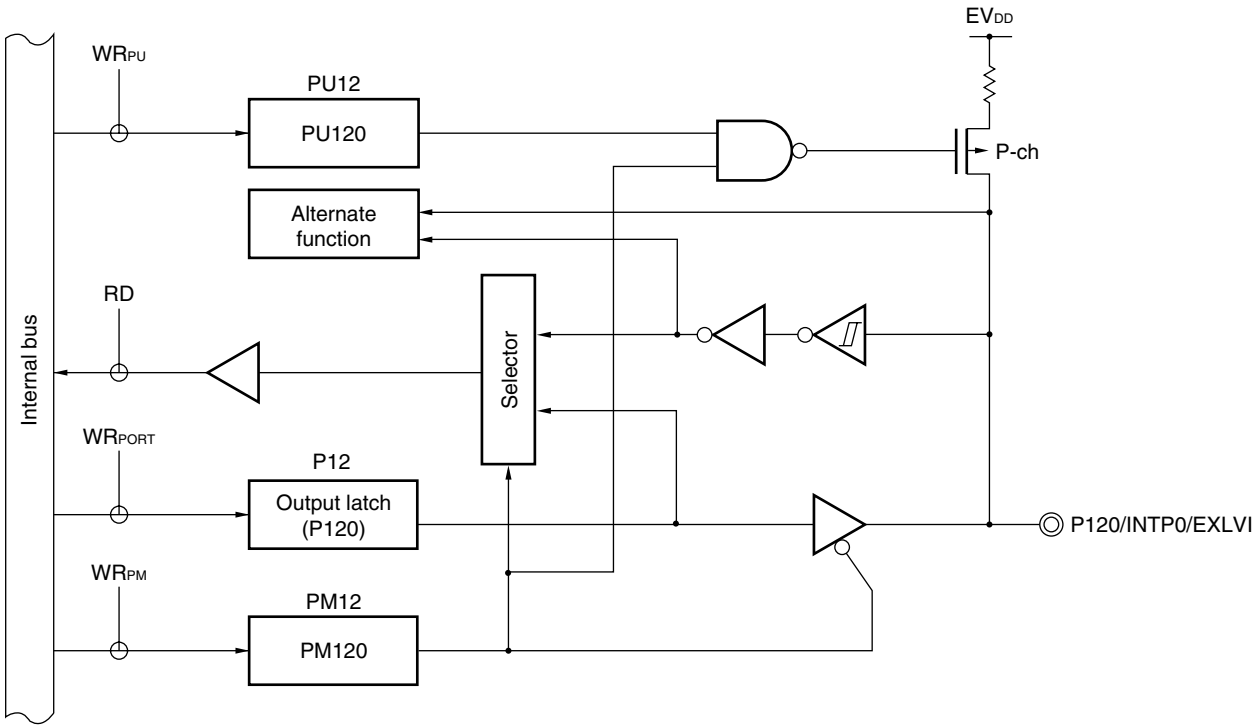


Caution 2. Process the P121/X1/OCD0A pin of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P121/X1/OCD0A
Flash memory programmer connection		Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset	
	During reset released	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

Remark X1 and X2 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD AND 78F05xxDA ONLY).**

Figure 5-22. Block Diagram of P120



P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

(8) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 6-11. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				fx = 10 MHz	fx = 20 MHz
0	0	1	2^{11}/fx	204.8 μs	102.4 μs
0	1	0	2^{13}/fx	819.2 μs	409.6 μs
0	1	1	2^{14}/fx	1.64 ms	819.2 μs
1	0	0	2^{15}/fx	3.27 ms	1.64 ms
1	0	1	2^{16}/fx	6.55 ms	3.27 ms
Other than above			Setting prohibited		

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

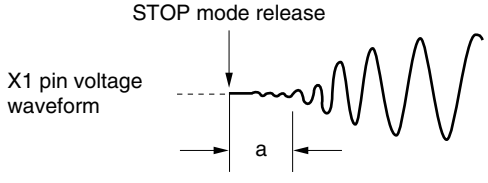
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

7.4.3 External event counter operation

When bits 1 and 0 (PRM0n1 and PRM0n0) of the prescaler mode register 0n (PRM0n) are set to 11 (for counting up with the valid edge of the TI00n pin) and bits 3 and 2 (TMC0n3 and TMC0n2) of 16-bit timer mode control register 0n (TMC0n) are set to 11, the valid edge of an external event input is counted, and a match interrupt signal indicating matching between TM0n and CR00n (INTTM00n) is generated.

To input the external event, the TI00n pin is used. Therefore, the timer/event counter cannot be used as an external event counter in the clear & start mode entered by the TI00n pin valid edge input (when TMC0n3 and TMC0n2 = 10).

The INTTM00n signal is generated with the following timing.

- Timing of generation of INTTM00n signal (second time or later)
  = Number of times of detection of valid edge of external event × (Set value of CR00n + 1)

However, the first match interrupt immediately after the timer/event counter has started operating is generated with the following timing.

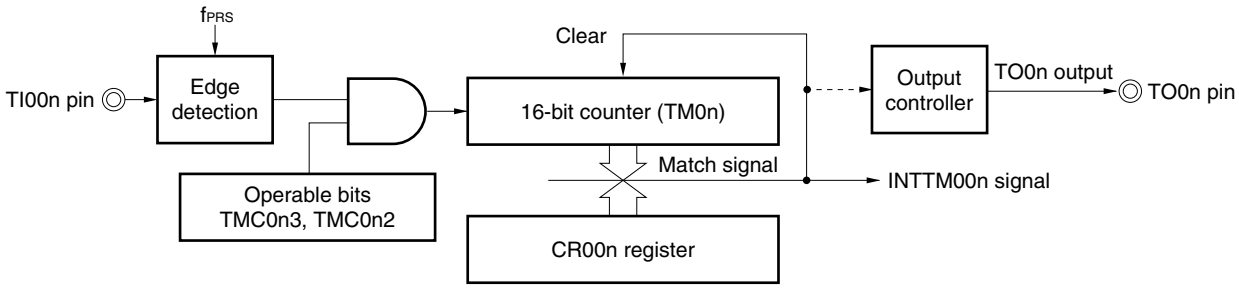
- Timing of generation of INTTM00n signal (first time only)
  = Number of times of detection of valid edge of external event input × (Set value of CR00n + 2)

To detect the valid edge, the signal input to the TI00n pin is sampled during the clock cycle of f_{PRS}. The valid edge is not detected until it is detected two times in a row. Therefore, a noise with a short pulse width can be eliminated.

Remarks 1. For the setting of I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 7-24. Block Diagram of External Event Counter Operation



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(5) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 pins to analog input of A/D converter or digital I/O of port.

ADPC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark ANI0 to ANI3: 78K0/KB2
ANI0 to ANI5: 38-pin products of the 78K0/KC2
ANI0 to ANI7: Products other than above

Figure 13-9. Format of A/D Port Configuration Register (ADPC)

Address: FF2FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

Products other than the right: Note 1
38-pin products of KC2: Note 1, Note 2
KB2: Note 1, Note 2

ADPC3	ADPC2	ADPC1	ADPC0	Digital I/O (D)/analog input (A) switching							
				P27/ ANI7	P26/ ANI6	P25/ ANI5	P24/ ANI4	P23/ ANI3	P22/ ANI2	P21/ ANI1	P20/ ANI0
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	A	A	A	A	A	A	D
0	0	1	0	A	A	A	A	A	A	D	D
0	0	1	1	A	A	A	A	A	D	D	D
0	1	0	0	A	A	A	A	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

Notes 1. Setting permitted
2. Setting prohibited

Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 (PM2).
2. If data is written to ADPC, a wait cycle is generated. Do not write data to ADPC when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

Figure 18-2 shows a serial bus configuration example.

Figure 18-2. Serial Bus Configuration Example Using I²C Bus

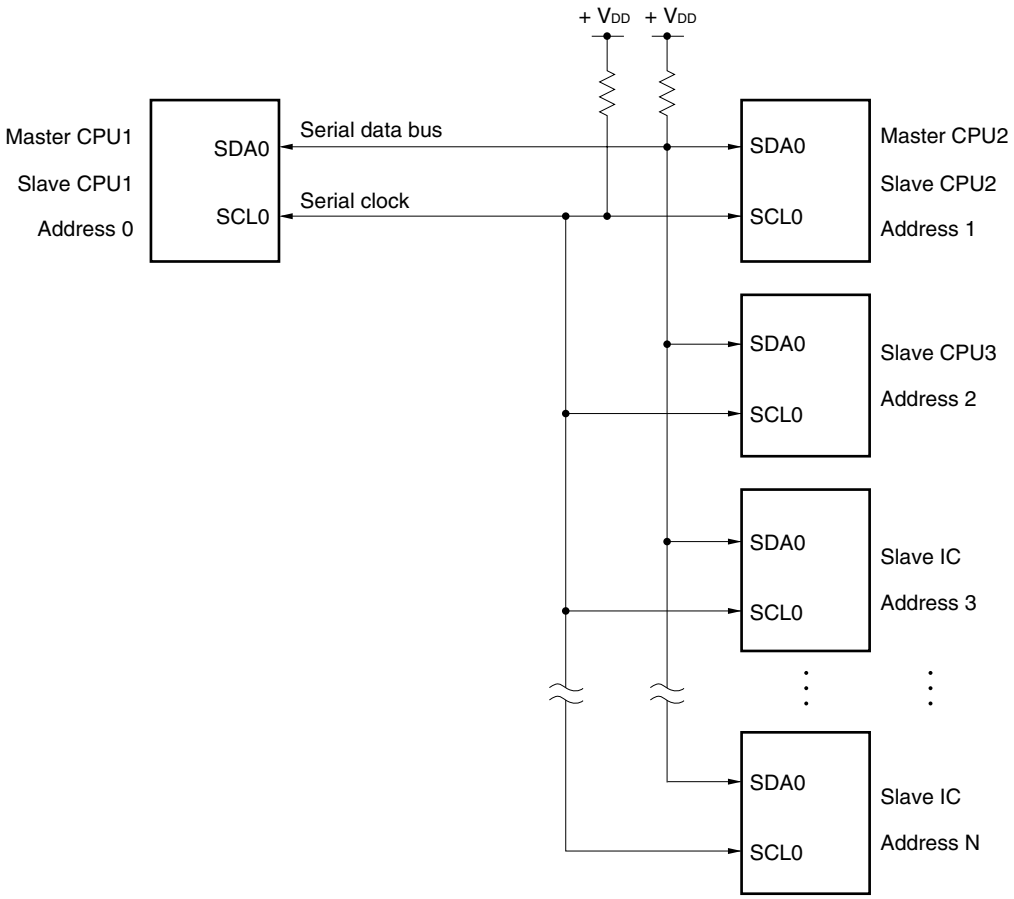


Figure 18-7. Format of IIC Flag Register 0 (IICF0)

Address: FFABH After reset: 00H R/W[Note]

Symbol	<7>	<6>	5	4	3	2	<1>	<0>
IICF0	STCF	IICBSY	0	0	0	0	STCEN	IICRSV

STCF	STT0 clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear STT0 flag

Condition for clearing (STCF = 0)	Condition for setting (STCF = 1)
• Cleared by STT0 = 1 • When IICE0 = 0 (operation stop) • Reset	• Generating start condition unsuccessful and STT0 bit cleared to 0 when communication reservation is disabled (IICRSV = 1).

IICBSY	I^2C bus status flag
0	Bus release status (communication initial status when STCEN = 1)
1	Bus communication status (communication initial status when STCEN = 0)

Condition for clearing (IICBSY = 0)	Condition for setting (IICBSY = 1)
• Detection of stop condition • When IICE0 = 0 (operation stop) • Reset	• Detection of start condition • Setting of IICE0 bit when STCEN = 0

STCEN	Initial start enable trigger
0	After operation is enabled (IICE0 = 1), enable generation of a start condition upon detection of a stop condition.
1	After operation is enabled (IICE0 = 1), enable generation of a start condition without detecting a stop condition.

Condition for clearing (STCEN = 0)	Condition for setting (STCEN = 1)
• Detection of start condition • Reset	• Set by instruction

IICRSV	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation

Condition for clearing (IICRSV = 0)	Condition for setting (IICRSV = 1)
• Cleared by instruction • Reset	• Set by instruction

Note Bits 6 and 7 are read-only.

Cautions 1. Write to STCEN bit only when the operation is stopped (IICE0 = 0).

2. As the bus release status (IICBSY = 0) is recognized regardless of the actual bus status when STCEN = 1, when generating the first start condition (STT0 = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.

3. Write to IICRSV bit only when the operation is stopped (IICE0 = 0).

Remark STT0: Bit 1 of IIC control register 0 (IICC0)
IICE0: Bit 7 of IIC control register 0 (IICC0)

Figure 20-3. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KC2)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	DUALIF0 CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	0	PIF6 Note 1	WTIF	KRIF	TMIF51	WTIIF	SRIF0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
IF1H	0	0	0	0	0	0	0	IICIF0 DMUIF Note 2

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Notes 1. 48-pin products only.

2. Products whose flash memory is at least 48 KB only.

Cautions 1. Be sure to clear bits 6 and 7 of IF1L to 0 in the 38-pin and 44-pin products.
Be sure to clear bit 7 of IF1L to 0 in the 48-pin products.

2. Be sure to clear bits 1 to 7 of IF1H to 0.

Figure 20-4. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KD2)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	DUALIF0 CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	0	PIF6	WTIF	KRIF	TMIF51	WTIIF	SRIF0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
IF1H	0	0	0	0	0	0	0	IICIF0 DMUIF Note

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Note Products whose flash memory is at least 48 KB only.

Caution Be sure to clear bit 7 of 1F1L and bits 1 to 7 of IF1H to 0.

Figure 20-17. Format of External Interrupt Rising Edge Enable Register (EGP) and External Interrupt Falling Edge Enable Register (EGN) (1/2)

(1) 78K0/KB2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

(2) 38-pin and 44-pin products of 78K0/KC2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

(3) 48-pin products of 78K0/KC2, 78K0/KD2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Caution Be sure to clear bits 6 and 7 of EGP and EGN to 0 in 78K0/KB2, and 38-pin and 44-pin products of 78K0/KC2.
Be sure to clear bit 7 of EGP and EGN to 0 in 78K0/KD2, and 48-pin products of 78K0/KC2.

Remark n = 0 to 5: 78K0/KB2, 38-pin and 44-pin products of 78K0/KC2
n = 0 to 6: 78K0/KD2, 48-pin products of 78K0/KC2

22.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For the registers that start, stop, or select the clock, see **CHAPTER 6 CLOCK GENERATOR**.

(1) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter. When X1 clock oscillation starts with the internal high-speed oscillation clock or subsystem clock used as the CPU clock, the X1 clock oscillation stabilization time can be checked.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, and WDT), the STOP instruction and MSTOP (bit 7 of MOC register) = 1 clear OSTC to 00H.

25.4.2 When used as interrupt

(1) When detecting level of supply voltage (V_{DD})

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).
  - <3> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <4> Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <5> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <6> Use software to wait for an operation stabilization time (10 μs (MIN.)).
  - <7> Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, at bit 0 (LVIF) of LVIM.
  - <8> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <9> Release the interrupt mask flag of LVI (LVIMK).
  - <10> Execute the EI instruction (when vector interrupts are used).

  Figure 25-7 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <9> above.

- When stopping operation
  Either of the following procedures must be executed.

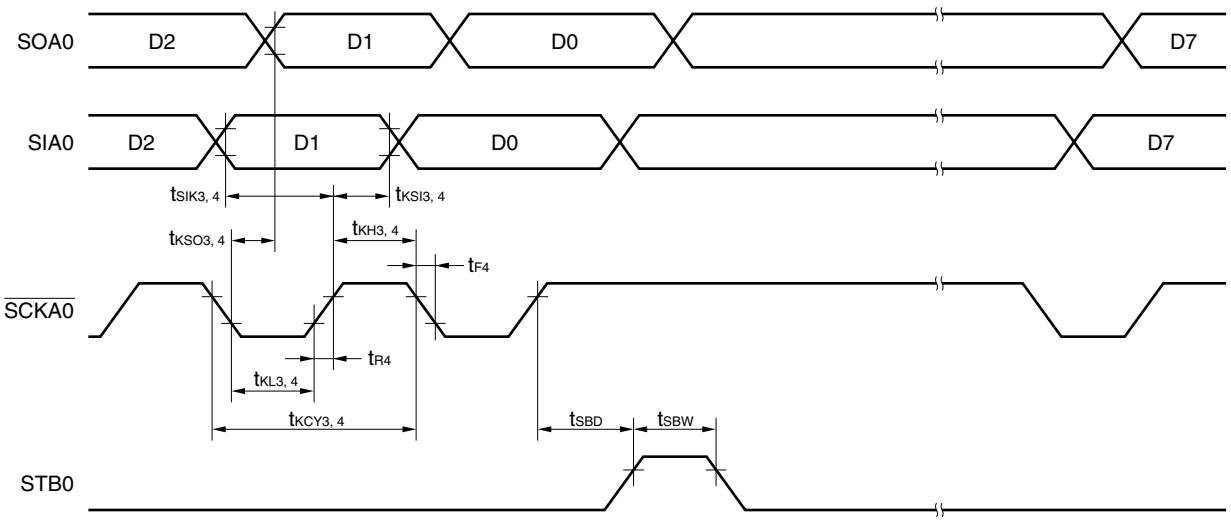
  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVION to 0.

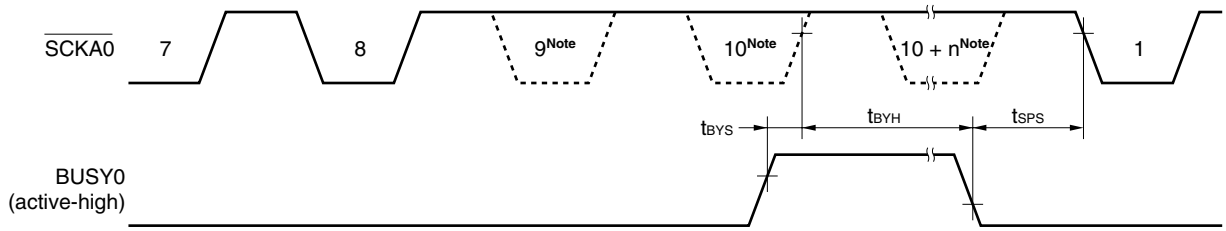
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Serial Transfer Timing (2/2)

CSIA0:



CSIA0 (busy processing):



Note SCKA0 does not become low level here, but the timing is illustrated so that the timing specifications can be shown.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

(2) Serial interface

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

(a) UART6 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(c) IIC0

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{SCL}		0	100	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7	–	0.6	–	μs
Hold time[Note 1]	$t_{HD:STA}$		4.0	–	0.6	–	μs
Hold time when SCL0 = "L"	t_{LOW}	Internal clock operation	4.7	–	1.3	–	μs
		EXSCL0 clock (6.4 MHz) operation	4.7	–	1.25	–	μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0	–	0.6	–	μs
Data setup time (reception)	$t_{SU:DAT}$		250	–	100	–	ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	$f_W = f_{XH}/2^N$ or $f_W = f_{EXSCL0}$ selected[Note 3]	0	3.45	0	0.9[Note 4]	μs
						1.00[Note 5]	
		$f_W = f_{RH}/2^N$ selected[Note 3]	0	3.45	0	1.05	μs
Setup time of stop condition	$t_{SU:STO}$		4.0	–	0.6	–	μs
Bus free time	t_{BUF}		4.7	–	1.3	–	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. f_W indicates the IIC0 transfer clock selected by the IICCL and IICX0 registers.

4. When $f_W \geq 4.4$ MHz is selected

5. When $f_W < 4.4$ MHz is selected

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

- **Basic characteristics**

Parameter		Symbol	Conditions				MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}	f_{XP} = 10 MHz (TYP.), 20 MHz (MAX.)					4.5	11.0	mA
Erase time Notes 1, 2	All block	T_{eraca}						20	200	ms
	Block unit	T_{erasa}						20	200	ms
Write time (in 8-bit units) Note 1		T_{wrwa}						10	100	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite Note 3	Expanded-specification Products (μPD78F05xxA (A))	• When a flash memory programmer is used, and the libraries Note 4 provided by Renesas Electronics are used • For program update	Retention: 15 years	1000			Times
					• When the EEPROM emulation libraries Note 5 provided by Renesas Electronics are used • The rewritable ROM size: 4 KB • For data update	Retention: 5 years	10000			Times
				Expanded-specification Products (μPD78F05xxA (A))	Conditions other than the above Note 6	Retention: 10 years	100			Times
				Conventional-specification Products (μPD78F05xx (A))						

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP4 or PG-FP5, is used and the rewrite time during self programming, see **Tables 27-12** to **27-14**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

4. The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) is excluded.

5. The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) is excluded.

6. These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) and the sample program specified by **the 78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) are used.

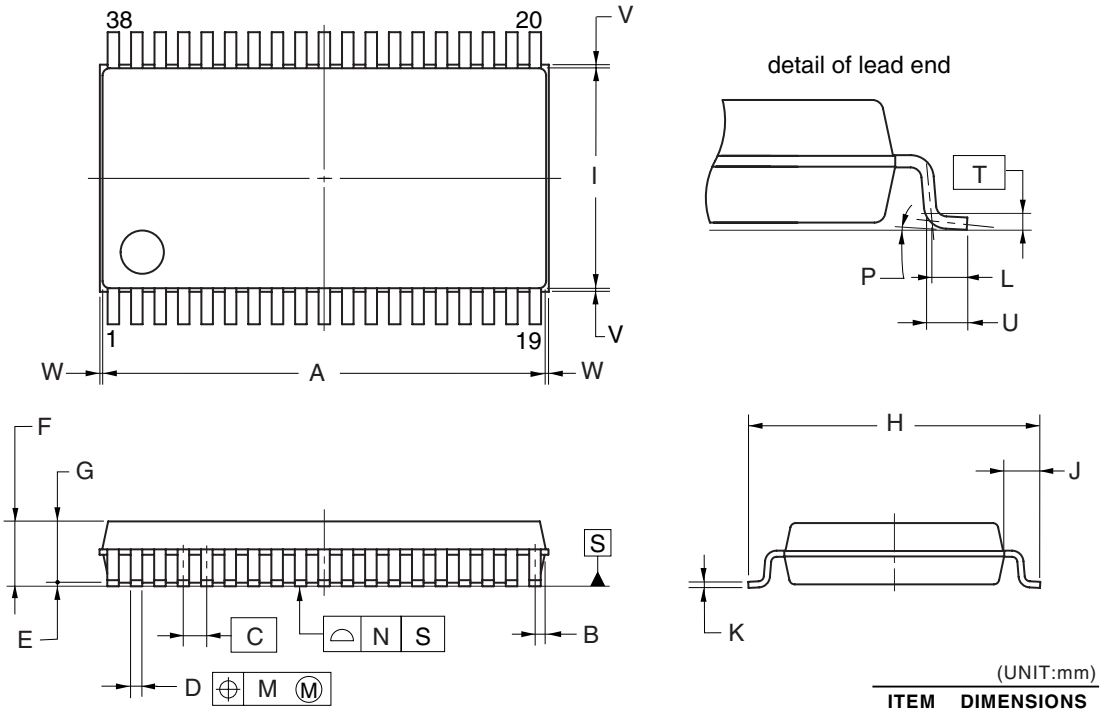
Remarks 1. f_{XP}: Main system clock oscillation frequency

2. For serial write operation characteristics, refer to **78K0/Kx2 Flash Memory Programming (Programmer) Application Note (**Document No.: **U17739E)**.

34.2 78K0/KC2

- μPD78F0511AMC-GAA-AX, 78F0512AMC-GAA-AX, 78F0513AMC-GAA-AX, 78F0513DAMC-GAA-AX
- μPD78F0511AMCA-GAA-G, 78F0512AMCA-GAA-G, 78F0513AMCA-GAA-G
- μPD78F0511AMCA2-GAA-G, 78F0512AMCA2-GAA-G, 78F0513AMCA2-GAA-G

38-PIN PLASTIC SSOP (7.62mm (300))



(UNIT:mm)

ITEM	DIMENSIONS
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	$0.30^{+0.10}_{-0.05}$
E	0.125±0.075
F	2.00 MAX.
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.10}_{-0.05}$
L	0.50
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P38MC-65-GAA

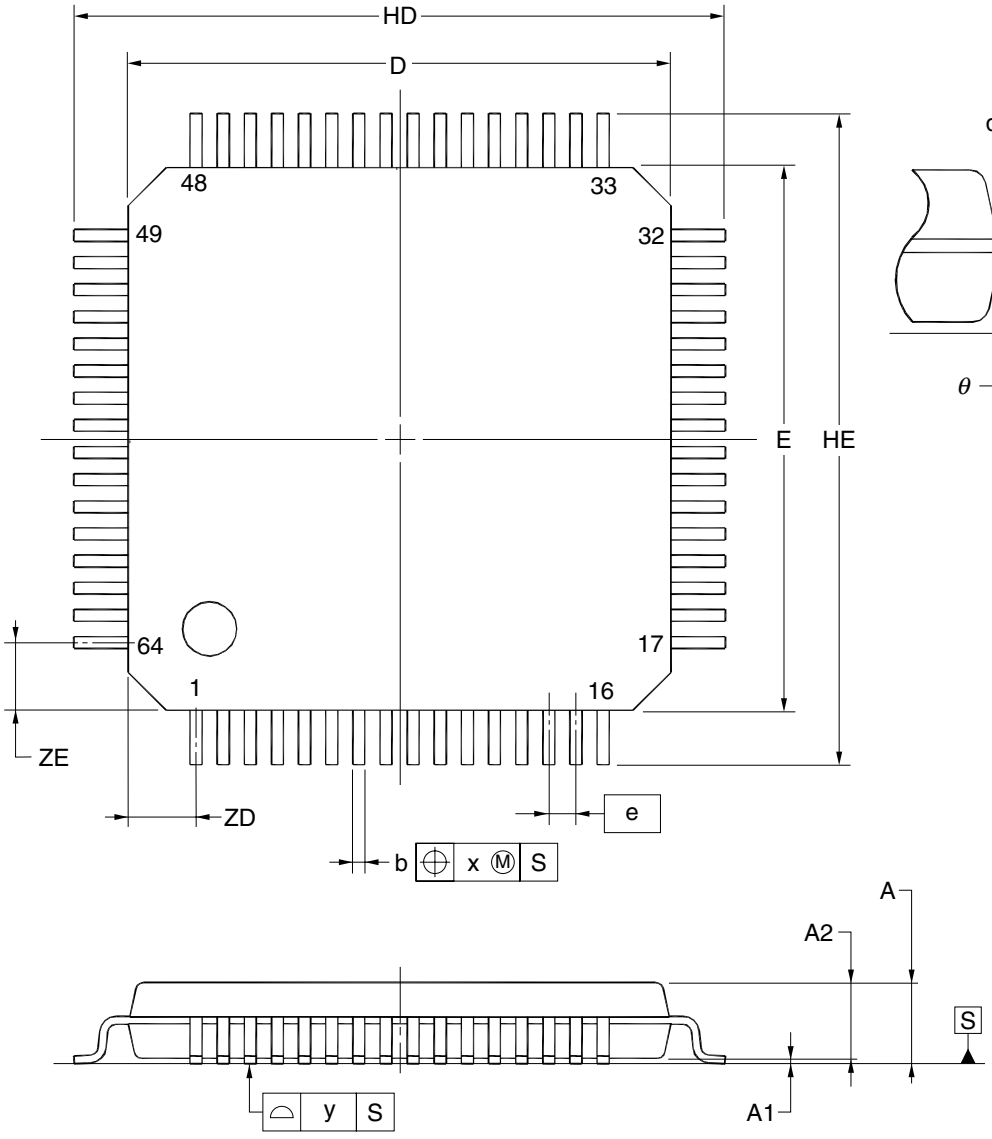
NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

34.4 78K0/KE2

- μPD78F0531GB-UEU-A, 78F0532GB-UEU-A, 78F0533GB-UEU-A, 78F0534GB-UEU-A, 78F0535GB-UEU-A, 78F0536GB-UEU-A, 78F0537GB-UEU-A, 78F0537DGB-UEU-A

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.55}_{-0.45}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P64GB-50-UEU

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

(26/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 24	Soft	Power-on-clear circuit	In 2.7 V/1.59 V POC mode	A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the supply voltage reaches 1.59 V (TYP.). If the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) within 1.93 ms, the power supply oscillation stabilization time of 0 to 5.39 ms is automatically generated before reset processing.	p. 695 ☐
			Cautions for power-on-clear circuit	In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.	p. 696 ☐
Chapter 25	Soft	Low-voltage detector	LVIM: Low-voltage detection register	To stop LVI, follow either of the procedures below. • When using 8-bit memory manipulation instruction: Write 00H to LVIM. • When using 1-bit memory manipulation instruction: Clear LVION to 0.	p. 700 ☐
	Hard			Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.	p. 700 ☐
	Soft			When using LVI as an interrupt, if LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.	p. 701 ☐
			LVIM and LVIS	With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.	p. 701 ☐
			LVIS: Low-voltage detection level selection register	Be sure to clear bits 4 to 7 to "0".	p. 701 ☐
				Do not change the value of LVIS during LVI operation.	p. 701 ☐
				When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.	p. 701 ☐
				With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.	p. 701 ☐
			When used as reset (When detecting level of supply voltage (V_{DD}))	<1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <4>.	p. 703 ☐
				If supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.	p. 703 ☐
			When used as reset (When detecting level of input voltage from external input pin (EXLVI))	<1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.	p. 706 ☐
				If input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.)) when LVIMD is set to 1, an internal reset signal is not generated.	p. 706 ☐
	Hard			Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.	p. 706 ☐
			When used as interrupt (When detecting level of input voltage from external input pin (EXLVI))	Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.	p. 711 ☐
	Soft		Cautions for low-voltage detector	In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used. (1) When used as reset The system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking action (1) below. (2) When used as interrupt Interrupt requests may be frequently generated. Take (b) of action (2) below.	p. 713 ☐
Chapter 26	Soft	Option byte	0082H, 0083H/1082H, 1083H	Be sure to set 00H to 0082H and 0083H (0082H/1082H and 0083H/1083H when the boot swap function is used).	p. 716 ☐
			0080H/1080H	Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.	p. 716 ☐