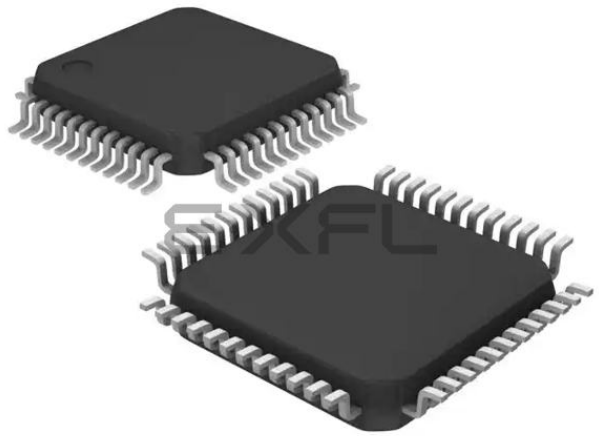
Renesas Electronics America Inc - UPD78F0512AGA-GAM-AX Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0512aga-gam-ax

Differences Between Conventional-specification Products and Expanded-specification Products

The differences between the conventional-specification products (μPD78F05xx, 78F05xxD) and expanded-specification products (μPD78F05xxA, 78F05xxDA) of the 78K0/Kx2 microcontrollers are described below.

- A/D conversion time
- X1 oscillator characteristics
- Instruction cycle, peripheral hardware clock frequency, external main system clock frequency, external main system clock input high-level width, and external main system clock input low-level width (AC characteristics)
- The number of flash memory rewrites and retention time
- Processing time of the self programming library
- Interrupt response time of the self programming library

For details, see **1.1 Differences Between Conventional-specification Products (μPD78F05xx, 78F05xxD) and Expanded-specification Products (μPD78F05xxA, 78F05xxDA).**

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The manual for the 78K0/Kx2 microcontrollers is separated into two parts: this manual and the instructions edition (common to the 78K0 microcontrollers).

78K0/Kx2 User's Manual (This Manual)	**78K/0 Series User's Manual Instructions**
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- When using this manual as the manual for (A) grade products and (A2) grade products of the 78K0/Kx2 microcontrollers:
  → Only the quality grade differs between standard products and (A), (A2) grade products. Read the part number as follows.
  - μPD78F05xx→ μPD78F05xx(A), 78F05xx(A2)
  - μPD78F05xxA→ μPD78F05xxA(A), 78F05xxA(A2)
- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.
- To check the details of a register when you know the register name:
  → See **APPENDIX C REGISTER INDEX**.

1.4 Ordering Information

[Part Number]

μPD78F05xy X X XX (X) - XXX - XX

	Semiconductor	
A	Lead-free	Product contains no lead in any area
AX, G		Product contains no lead in any area (Terminal finish is Ni/Pd/Au plating)

	Quality Grade
None	Standard (T_A = −40 to +85°C)
(A), A	Special (T_A = −40 to +85°C)
(A2), A2	Special (T_A = −40 to +125°C)

		Package Type
50y (KB2)	MC-5A4	30-pin plastic SSOP (7.62 mm (300))
	MC-CAB	
	FC-AA3	36-pin plastic FLGA (4x4)
51y (KC2)	MC-GAA	38-pin plastic SSOP (7.62 mm (300))
	GB-UES	44-pin plastic LQFP (10x10)
	GB-GAF	
	GA-8EU	48-pin plastic LQFP (fine pitch) (7x7)
	GA-GAM	
52y (KD2)	GB-UET	52-pin plastic LQFP (10x10)
	GB-GAG	
53y (KE2)	GB-UEU	64-pin plastic LQFP (fine pitch) (10x10)
	GB-GAH	
	GC-UBS	64-pin plastic LQFP (14x14)
	GC-GAL	
	GK-UET	64-pin plastic LQFP (12x12)
	GK-GAJ	
	GA-9EV	64-pin plastic TQFP (fine pitch) (7x7)
	GA-HAB	
	FC-AA1	64-pin plastic FLGA (5x5)
	F1-AA2	64-pin plastic FBGA (4x4)
54y (KF2)	GC-UBT	80-pin plastic LQFP (14x14)
	GC-GAD	
	GK-8EU	80-pin plastic LQFP (fine pitch) (12x12)
	GK-GAK	

	Product Type
None	Conventional-specification products
A	Expanded-specification products

	On-chip Debug Function
None	Not mounted
D	Mounted

	High-speed RAM Capacity	Expansion RAM Capacity	Flash Memory Capacity
5x0	512 bytes	–	8 KB
5x1	768 bytes	–	16 KB
5x2	1 KB	–	24 KB
5x3	1 KB	–	32 KB
5x4	1 KB	1 KB	48 KB
5x5	1 KB	2 KB	60 KB
5x6	1 KB	4 KB	96 KB
5x7	1 KB	6 KB	128 KB

	Product Type
F	Flash memory version

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by Renesas Electronics to know the specification of quality grade on the devices and its recommended applications.

(1) Port functions (2/2): 78K0/KF2

Function Name	I/O	Function	After Reset	Alternate Function
P70 to P77	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR7
P120	I/O	Port 12. 5-bit I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121				X1/OCD0A Note
P122				X2/EXCLK/OCD0B Note
P123				XT1
P124				XT2/EXCLKS
P130	Output	Port 13. 1-bit output-only port.	Output port	–
P140	I/O	Port 14. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCL/INTP6
P141				BUZ/BUSY0/INTP7
P142				$\overline{\text{SCKA0}}$
P143				SIA0
P144				SOA0
P145				STB0

Note μPD78F0547D and 78F0547DA (product with on-chip debug function) only

(2) Non-port functions (1/3): 78K0/KF2

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Analog input	P20 to P27
BUSY0	Input	CSIA0 busy input	Input port	P141/BUZ/INTP7
BUZ	Output	Buzzer output	Input port	P141/BUSY0/INTP7
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
EXSCL0	Input	External clock input for I^2C. To input an external clock, input a clock of 6.4 MHz.	Input port	P62
FLMD0	–	Flash memory programming mode setting	–	–
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P30
INTP2				P31/OCD1A Note
INTP3				P32/OCD1B Note
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
INTP6				P140/PCL
INTP7				P141/BUZ/BUSY0
KR0 to KR7	Input	Key interrupt input	Input port	P70 to P77

Note μPD78F0547D and 78F0547DA (product with on-chip debug function) only

Table 2-3. Pin I/O Circuit Types (2/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P30/INTP1	5-AQ	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P31/INTP2/OCD1A[Note 1]			
P32/INTP3/OCD1B			
P33/TI51/TO51/INTP4			
P40 to P47	5-AG		
P50 to P57			
P60/SCL0	13-AI		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor, or connect directly to EV_{SS}. Output: Leave this pin open at low-level output after clearing the output latch of the port to 0.
P61/SDA0			
P62/EXSCL0			
P63	13-P		
P64 to P67	5-AG		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P70/KR0 to P77/KR7	5-AQ		
P120/INTP0/EXLVI			
P121/X1/OCD0A[Notes 1, 2]	37		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P122/X2/EXCLK/ OCD0B[Notes 2]			
P123/XT1[Note 2]			
P124/XT2/EXCLKS[Note 2]			
P130	3-C	Output	Leave open.

Notes 1. Process the P31/INTP2/OCD1A and P121/X1/OCD0A pins of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

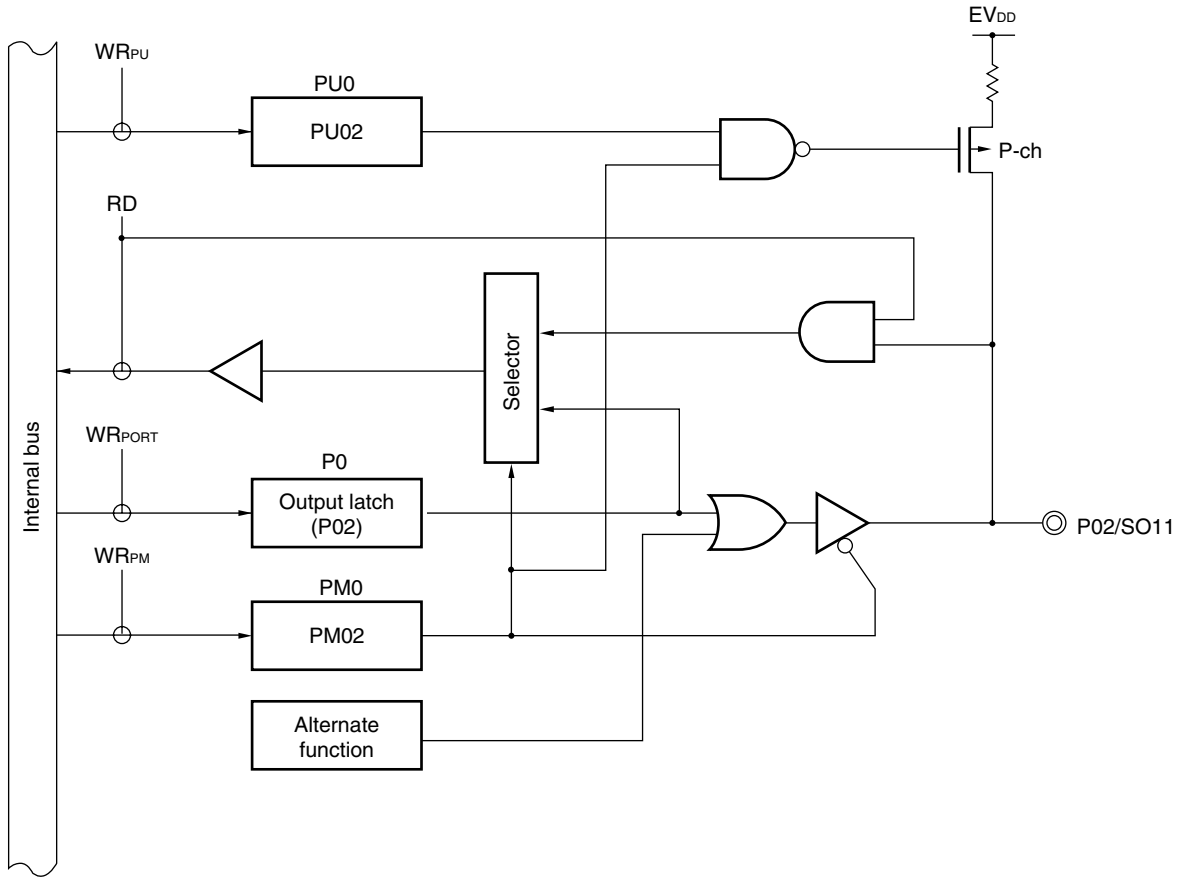
		P31/INTP2/OCD1A	P121/X1/OCD0A
Flash memory programmer connection		Connect to EV_{SS} via a resistor.	Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset		
	During reset released	Input: Connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

2. Use recommended connection above in I/O port mode (see **Figure 6-3** and **Figure 6-4 Format of Clock Operation Mode Select Register (OSCCTL)**) when these pins are not used.

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-3. Block Diagram of P02 (2/2)

(2) 78K0/KE2 products whose flash memory is at least 48 KB and 78K0/KF2



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

7.4.5 Free-running timer operation

When bits 3 and 2 (TMC0n3 and TMC0n2) of 16-bit timer mode control register 0n (TMC0n) are set to 01 (free-running timer mode), 16-bit timer/event counter 0n continues counting up in synchronization with the count clock. When it has counted up to FFFFH, the overflow flag (OVF0n) is set to 1 at the next clock, and TM0n is cleared (to 0000H) and continues counting. Clear OVF0n to 0 by executing the CLR instruction via software.

The following three types of free-running timer operations are available.

- Both CR00n and CR01n are used as compare registers.
- One of CR00n or CR01n is used as a compare register and the other is used as a capture register.
- Both CR00n and CR01n are used as capture registers.

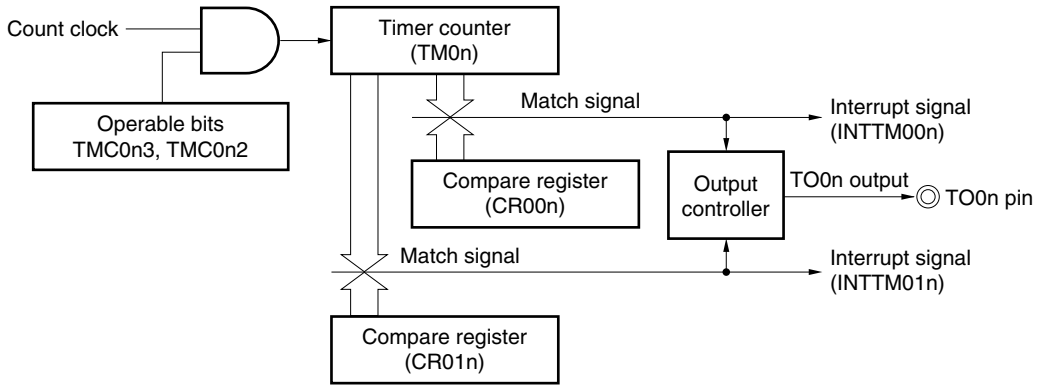
Remarks 1. For the setting of the I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

(1) Free-running timer mode operation

(CR00n: compare register, CR01n: compare register)

Figure 7-37. Block Diagram of Free-Running Timer Mode
(CR00n: Compare Register, CR01n: Compare Register)



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 12-4. Format of Clock Output Selection Register (CKS) (78K0/KE2, 78K0/KF2)

Address: FF40H After reset: 00H R/W

Symbol	<7>	6	5	<4>	3	2	1	0
CKS	BZOE	BCS1	BCS0	CLOE	CCS3	CCS2	CCS1	CCS0

BZOE	BUZ output enable/disable specification
0	Clock division circuit operation stopped. BUZ fixed to low level.
1	Clock division circuit operation enabled. BUZ output enabled.

BCS1	BCS0	BUZ output clock selection[Note 1]		
			f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	0	$f_{PRS}/2^{10}$	9.77 kHz	19.54 kHz
0	1	$f_{PRS}/2^{11}$	4.88 kHz	9.77 kHz
1	0	$f_{PRS}/2^{12}$	2.44 kHz	4.88 kHz
1	1	$f_{PRS}/2^{13}$	1.22 kHz	2.44 kHz

CLOE	PCL output enable/disable specification
0	Clock division circuit operation stopped. PCL fixed to low level.
1	Clock division circuit operation enabled. PCL output enabled.

CCS3	CCS2	CCS1	CCS0	PCL output clock selection[Note 1]			
					f_{SUB} = 32.768 kHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	0	0	0	f_{PRS}[Note 2]	–	10 MHz	Setting prohibited[Note 3]
0	0	0	1	$f_{PRS}/2$		5 MHz	10 MHz
0	0	1	0	$f_{PRS}/2^2$		2.5 MHz	5 MHz
0	0	1	1	$f_{PRS}/2^3$		1.25 MHz	2.5 MHz
0	1	0	0	$f_{PRS}/2^4$		625 kHz	1.25 MHz
0	1	0	1	$f_{PRS}/2^5$		312.5 kHz	625 kHz
0	1	1	0	$f_{PRS}/2^6$		156.25 kHz	312.5 kHz
0	1	1	1	$f_{PRS}/2^7$		78.125 kHz	156.25 kHz
1	0	0	0	f_{SUB}	32.768 kHz	–	
Other than above				Setting prohibited			

Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when f_{PRS} = f_{XH} (XSEL = 1).)

18.5.6 Wait

The wait is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCL0 pin to low level notifies the communication partner of the wait state. When wait state has been canceled for both the master and slave devices, the next data transfer can begin.

Figure 18-18. Wait (1/2)

(1) When master device has a nine-clock wait and slave device has an eight-clock wait (master transmits, slave receives, and ACKE0 = 1)

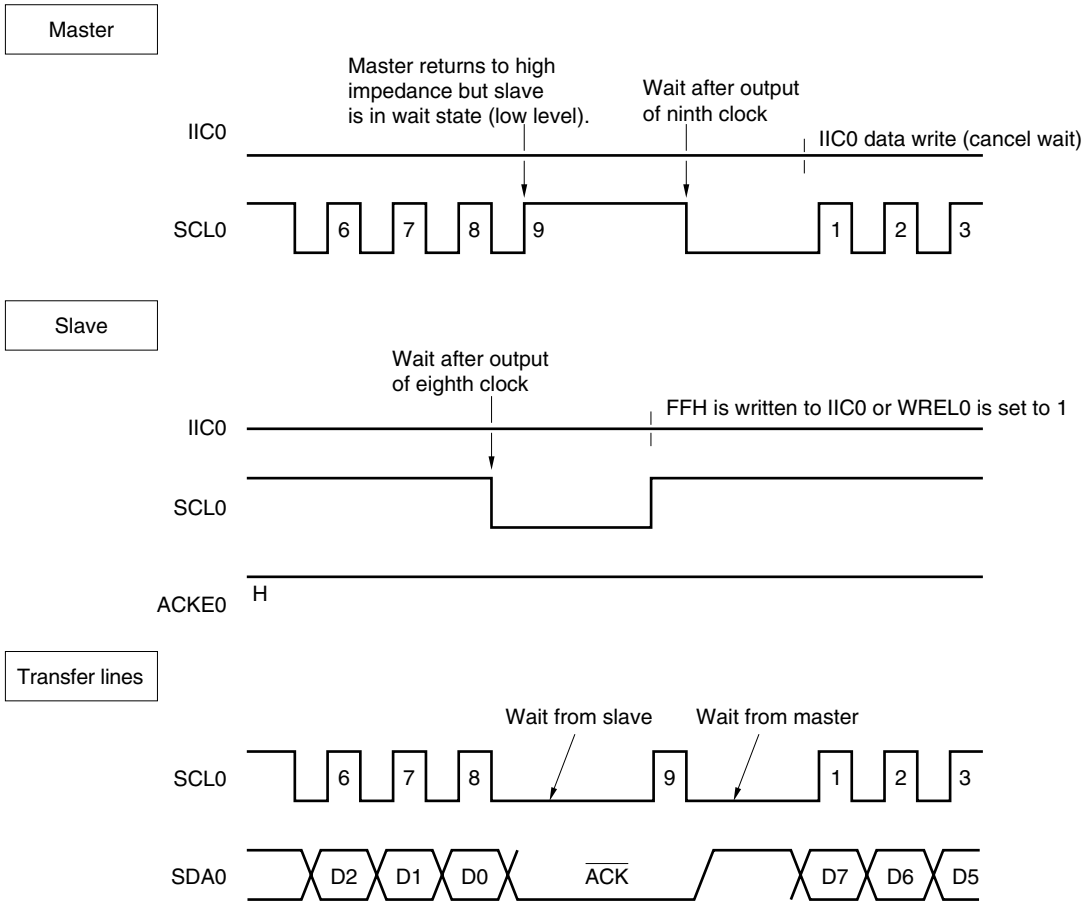


Figure 18-24. Master Operation in Multi-Master System (2/3)

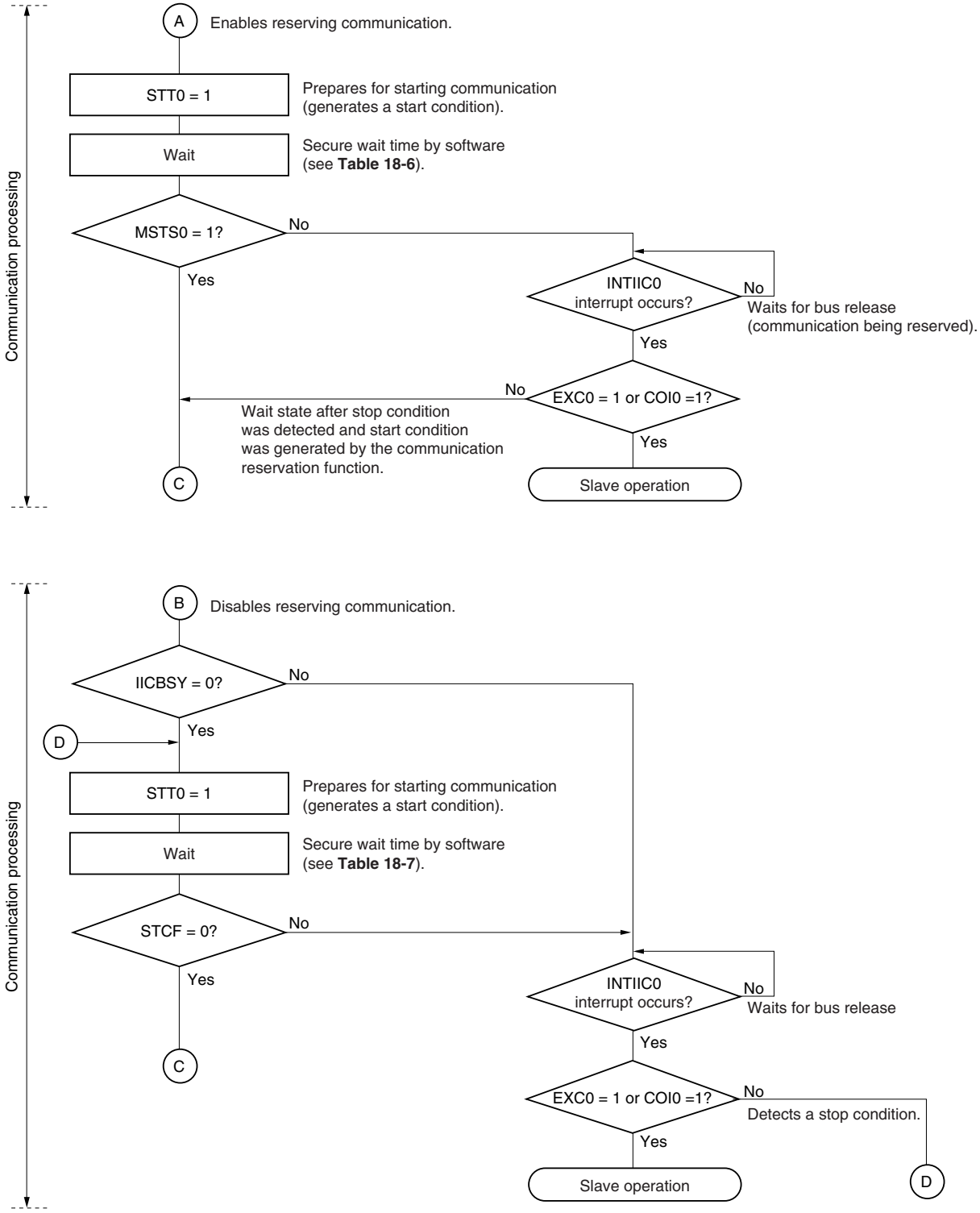


Figure 20-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KB2)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	DUALIF0 CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	7	6	5	4	<3>	2	<1>	<0>
IF1L	0	0	0	0	TMIF51	0	SRIF0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
IF1H	0	0	0	0	0	0	0	IICIF0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Caution Be sure to clear bits 2, 4 to 7 of IF1L and bits 1 to 7 of IF1H to 0.

(2) Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

MK0L, MK0H, MK1L, and MK1H are set by a 1-bit or 8-bit memory manipulation instruction. When MK0L and MK0H, and MK1L and MK1H are combined to form 16-bit registers MK0 and MK1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 20-7. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KB2)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	SREMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK010	TMMK000	TMMK50	TMMKH0	TMMKH1	DUALMK0 CSIMK10 STMK0	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	7	6	5	4	<3>	2	<1>	<0>
MK1L	1	1	1	1	TMMK51	1	SRMK0	ADMK

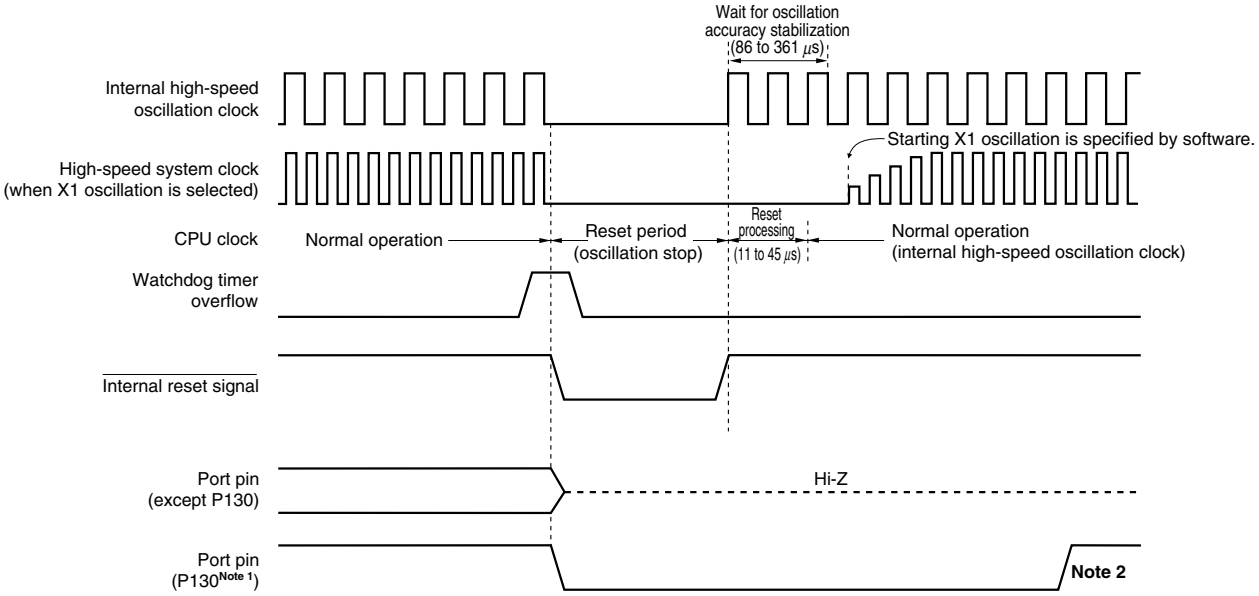
Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	<0>
MK1H	1	1	1	1	1	1	1	IICMK0

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution Be sure to set bits 2, 4 to 7 of MK1L and bits 1 to 7 of MK1H to 1.

Figure 23-3. Timing of Reset Due to Watchdog Timer Overflow



Notes 1. P130 pin is not mounted onto 78K0/KB2, and 38-pin and 44-pin products of the 78K0/KC2.

2. Set P130 to high-level output by software.

Caution A watchdog timer internal reset resets the watchdog timer.

Remark When reset is effected, P130 outputs a low level. If P130 is set to output a high level before reset is effected, the output signal of P130 can be dummy-output as the CPU reset signal.

Table 23-1. Operation Statuses During Reset Period

Item			During Reset Period
System clock			Clock supply to the CPU is stopped.
	Main system clock	f_{RH}	Operation stopped
		f_X	Operation stopped (pin is I/O port mode)
		f_{EXCLK}	Clock input invalid (pin is I/O port mode)
	Subsystem clock	f_{XT}	Operation stopped (pin is I/O port mode)
		f_{EXCLKS}	Clock input invalid (pin is I/O port mode)
	f_{RL}		Operation stopped
CPU			
Flash memory			
RAM			
Port (latch)			
16-bit timer/event counter		00	
		01	
8-bit timer/event counter		50	
		51	
8-bit timer		H0	
		H1	
Watch timer			
Watchdog timer			
Clock output			
Buzzer output			
A/D converter			
Serial interface		UART0	
		UART6	
		CSI10	
		CSI11	
		CSIA0	
		IIC0	
Multiplier/divider			
Power-on-clear function			Operable
Low-voltage detection function			Operation stopped
External interrupt			

Remarks 1. f_{RH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{XT}: XT1 clock
f_{EXCLKS}: External subsystem clock, f_{RL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. See **1.7 Block Diagram** and **1.8 Outline of Functions**.

27.3 Writing with Flash Memory Programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the 78K0/Kx2 microcontrollers have been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

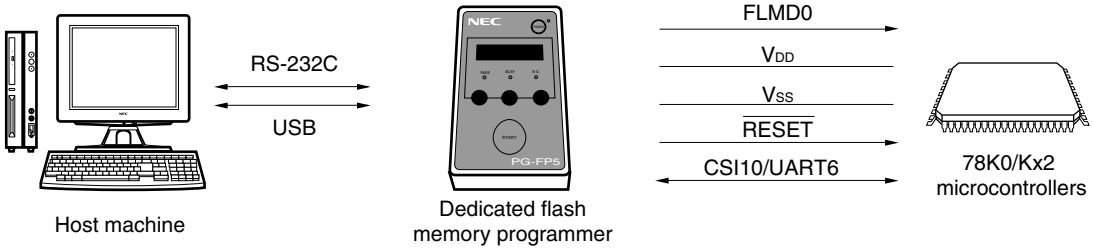
Data can be written to the flash memory with a dedicated program adapter (FA series) before the 78K0/Kx2 microcontrollers are mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

27.4 Programming Environment

The environment required for writing a program to the flash memory of the 78K0/Kx2 microcontrollers are illustrated below.

Figure 27-3. Environment for Writing Program to Flash Memory



A host machine that controls the dedicated flash memory programmer is necessary.

To interface between the dedicated flash memory programmer and the 78K0/Kx2 microcontrollers, CSI10 or UART6 is used for manipulation such as writing and erasing. To write the flash memory off-board, a dedicated program adapter (FA series) is necessary.

Table 27-14. Processing Time for Self Programming Library (Expanded-specification Products (μPD78F05xxA and 78F05xxDA)) (3/3)

(4) When high-speed system clock (X1 oscillation or external clock input) is used and entry RAM is located in short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		34/f_{CPU}			
Initialize library		55/f_{CPU} + 272			
Mode check library		36/f_{CPU} + 173		30/f_{CPU} + 173	
Block blank check library		179/f_{CPU} + 6108		136/f_{CPU} + 6108	
Block erase library		179/f_{CPU} + 19371	179/f_{CPU} + 267738	136/f_{CPU} + 19371	136/f_{CPU} + 267738
Word write library		333/f_{CPU} + 247 + 136 × w	333/f_{CPU} + 247 + 1647 × w	272/f_{CPU} + 247 + 136 × w	272/f_{CPU} + 247 + 1647 × w
Block verify library		179/f_{CPU}+12964		136/f_{CPU}+12964	
Self programming end library		34/f_{CPU}			
Get information library	Option value: 03H	180/f_{CPU} + 261		134/f_{CPU} + 261	
	Option value: 04H	190/f_{CPU} + 254		144/f_{CPU} + 254	
	Option value: 05H	350/f_{CPU} + 213		304/f_{CPU} + 213	
Set information library		80/f_{CPU} + 42839	80/f_{CPU} + 572592	72/f_{CPU} + 42839	72/f_{CPU} + 572592
EEPROM write library		333/f_{CPU} + 516 + 209 × w	333/f_{CPU} + 516 + 1722 × w	268/f_{CPU} + 516 + 209 × w	268/f_{CPU} + 516 + 1722 × w

Remarks 1. The above processing times are those when a write start address structure is located in the internal high-speed RAM and during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

3. f_{CPU}: CPU operation clock frequency

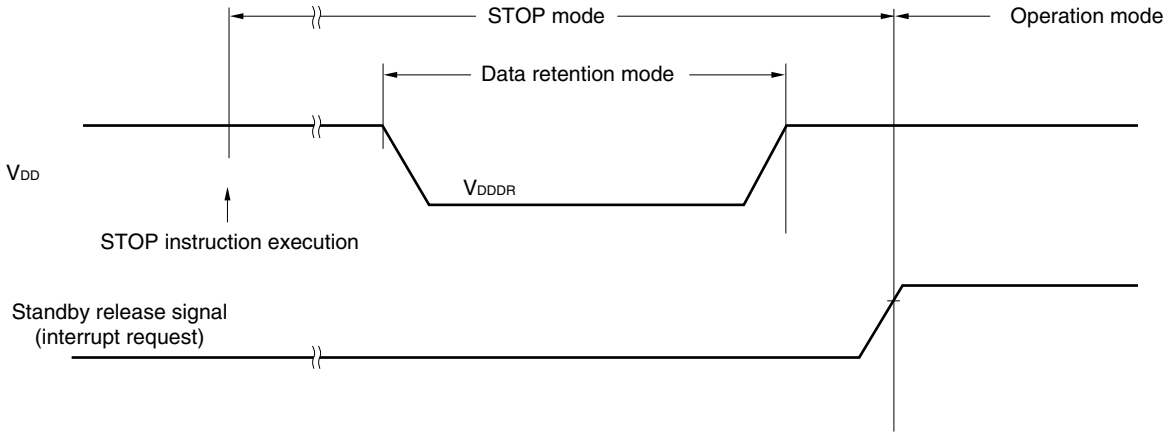
4. w: Number of words in write data (1 word = 4 bytes)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Notes 1. Total current flowing into the internal power supply (V_{DD}, EV_{DD}), including the peripheral operation current and the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, the current flowing into the pull-up resistors and the output current of the port are not included.

2. Not including the operating current of the 8 MHz internal oscillator, 240 kHz internal oscillator, and XT1 oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

3. When AMPH (bit 0 of clock operation mode select register (OSCCTL)) = 0.

4. Not including the operating current of the X1 oscillator, XT1 oscillator, and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

5. Not including the operating current of the X1 oscillation, 8 MHz internal oscillator and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

6. Not including the operating current of the 240 kHz internal oscillator and XT1 oscillation, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

7. Current flowing only to the A/D converter (AV_{REF}). The current value of the 78K0/Kx2 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

8. Current flowing only to the watchdog timer (including the operating current of the 240 kHz internal oscillator). The current value of the 78K0/Kx2 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

9. Current flowing only to the LVI circuit. The current value of the 78K0/Kx2 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(1) Basic operation (2/2)

(T_A = –40 to +110°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
External subsystem clock frequency[Note 1]	f_{EXCLKS}		32	32.768	35	kHz
External subsystem clock input high-level width, low-level width[Note 1]	$t_{EXCLKSH}$, $t_{EXCLKSL}$		12			μs
TI000, TI010, TI001, TI011 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$ + 0.1[Note 2]			μs
		2.7 V ≤ V_{DD} < 4.0 V	$2/f_{sam}$ + 0.2[Note 2]			μs
TI50, TI51 input frequency	f_{TI5}				10	MHz
TI50, TI51 input high-level width, low-level width	t_{TIH5}, t_{TIL5}		50			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}		1			μs
Key interrupt input low-level width	t_{KR}		250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

Notes 1. The 78K0/KB2 is not provided with a subsystem clock.

2. Selection of f_{sam} = f_{PRS}, $f_{PRS}/4$, $f_{PRS}/256$, or f_{PRS}, $f_{PRS}/16$, $f_{PRS}/64$ is possible using bits 0 and 1 (PRM000, PRM001 or PRM010, PRM011) of prescaler mode registers 00 and 01 (PRM00, PRM01). Note that when selecting the TI000 or TI001 valid edge as the count clock, f_{sam} = f_{PRS}.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

DC Characteristics (4/4)

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		3.2	8.3	mA
				Resonator connection		4.5	10.5	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		1.6	4.2	mA
				Resonator connection		2.3	5.9	mA
			f_{XH} = 10 MHz V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		1.5	4.1	mA
				Resonator connection		2.2	4.8	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.9	2.4	mA
				Resonator connection		1.3	3.0	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			1.4	3.8	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		6	138	μA
				Resonator connection		15	145	μA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		0.8	3.9	mA
				Resonator connection		2.0	6.6	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		0.4	2.0	mA
				Resonator connection		1.0	3.6	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.2	1.0	mA
				Resonator connection		0.5	1.7	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			0.4	1.8	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		3.0	133	μA
				Resonator connection		12	138	μA
	I_{DD3}[Note 6]	STOP mode				1	100	μA
			T_A = −40 to +70 °C			1	10	μA
A/D converter operating current	I_{ADC}[Note 7]	2.7 V ≤ AV_{REF} ≤ V_{DD}, ADCS = 1				0.86	2.9	mA
Watchdog timer operating current	I_{WDT}[Note 8]	During 240 kHz internal low-speed oscillation clock operation				5	15	μA
LVI operating current	I_{LVI}[Note 9]					9	27	μA

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or external subsystem clock frequency)

(Notes on next page)

78K0/Kx2

Renesas Electronics Corporation

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