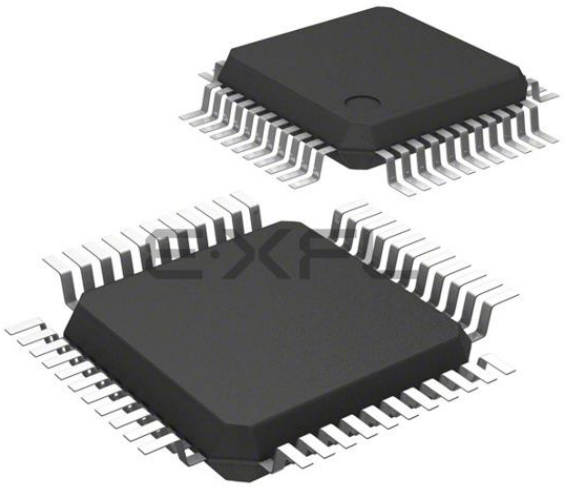
Renesas Electronics America Inc - UPD78F0512AGB-GAF-AX Datasheet



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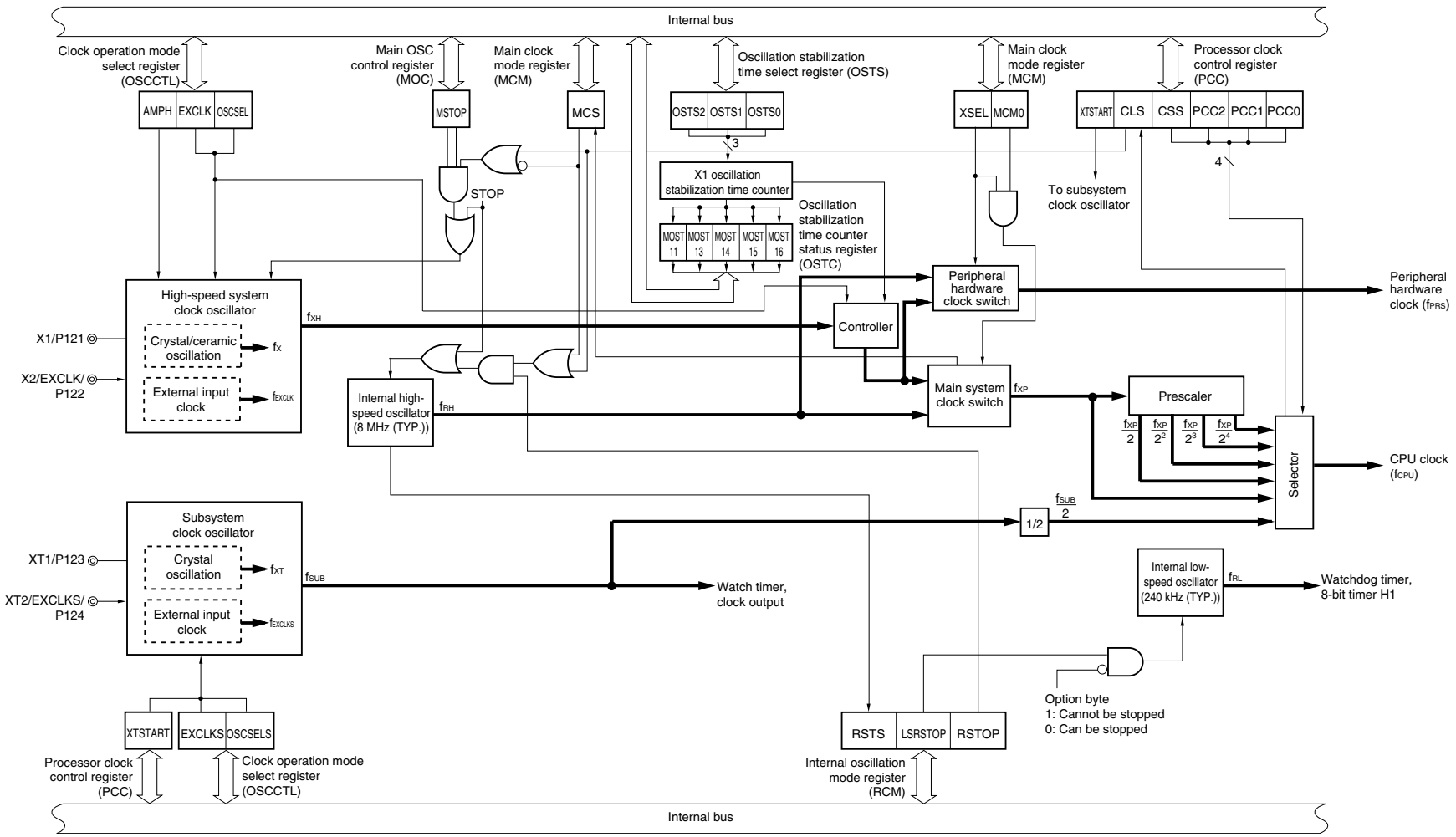
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0512agb-gaf-ax

Figure 6-2. Block Diagram of Clock Generator (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)



Notes 4. When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

5. The 78K0/KB2 is not provided with a subsystem clock.

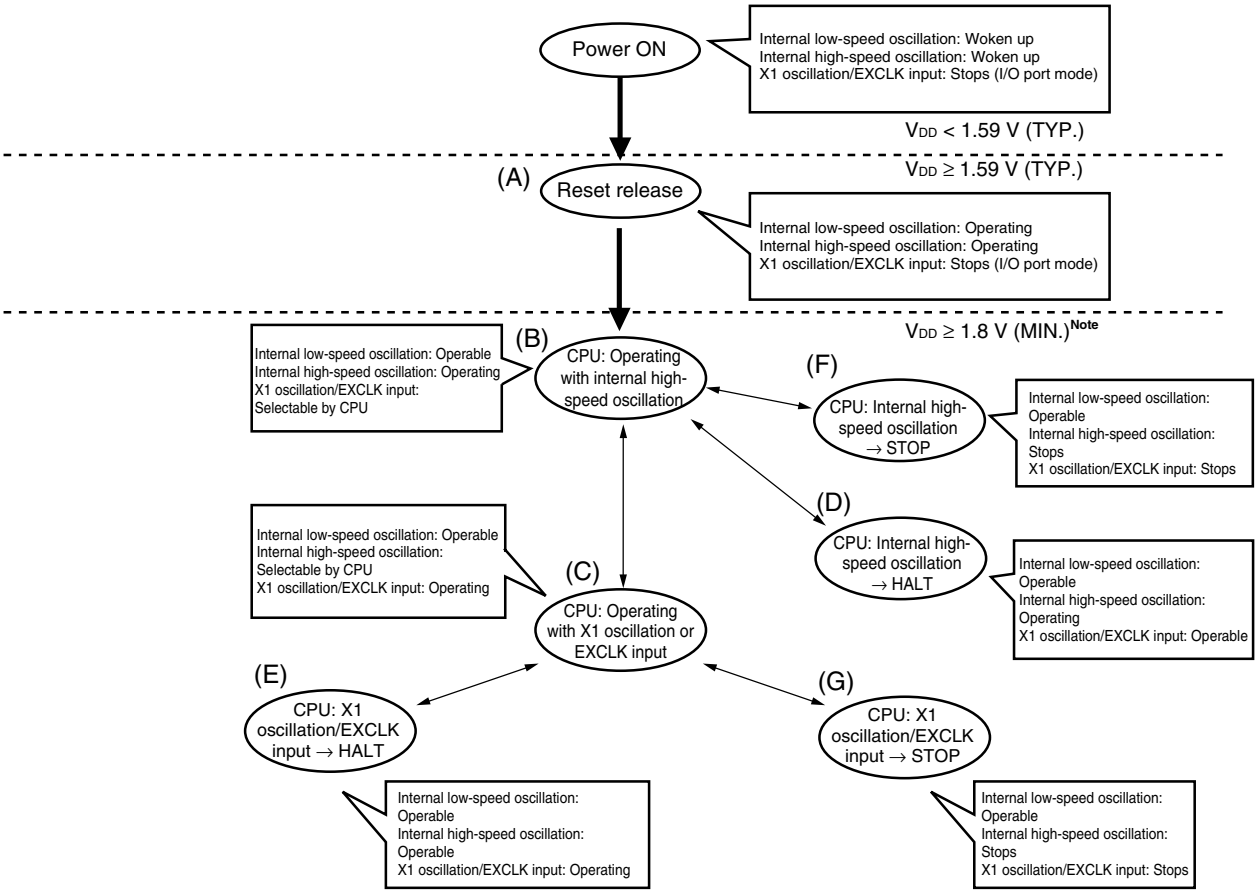
Caution It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK and EXCLKS pins is used.

Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing the STOP instruction (see **(4)** in **6.6.1 Example of controlling high-speed system clock**, **(3)** in **6.6.2 Example of controlling internal high-speed oscillation clock**, and **(4)** in **6.6.3 Example of controlling subsystem clock**).

6.6.6 CPU clock status transition diagram

Figure 6-17 and 6-18 shows the CPU clock status transition diagram of this product.

Figure 6-17. CPU Clock Status Transition Diagram
(When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0), 78K0/KB2)

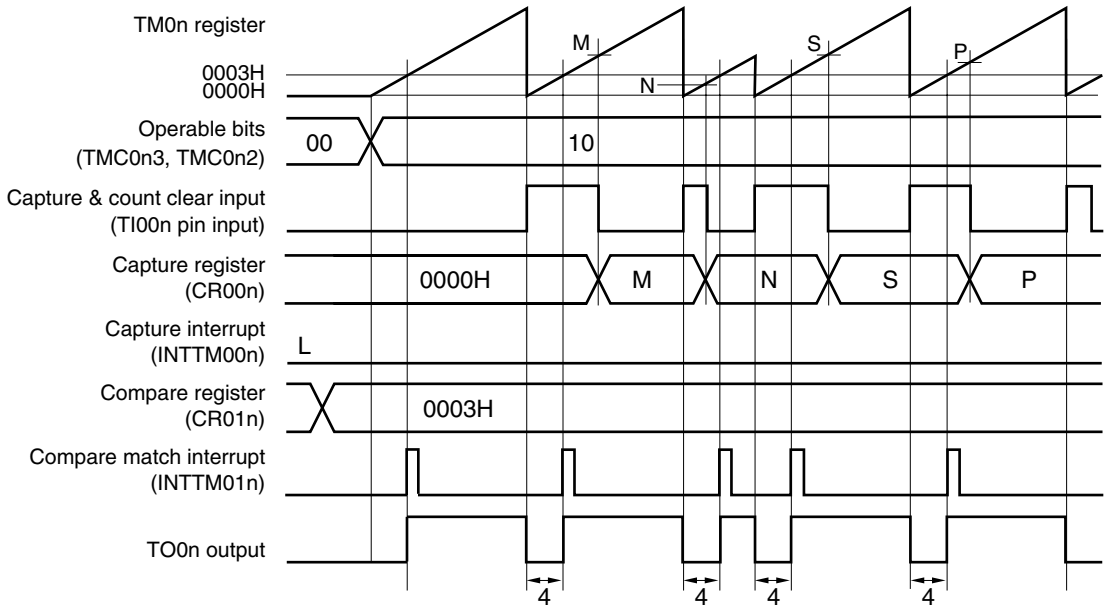


Note Standard and (A) grade products: 1.8 V,
(A2) grade products: 2.7 V

Remark In the 2.7 V/1.59 V POC mode (option byte: POCMODE = 1), the CPU clock status changes to (A) in the above figure when the supply voltage exceeds 2.7 V (TYP.), and to (B) after reset processing (11 to 45 μs).

Figure 7-32. Timing Example of Clear & Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register, CR01n: Compare Register) (2/2)

(b) TOC0n = 13H, PRM0n = 10H, CRC0n, = 03H, TMC0n = 0AH, CR01n = 0003H



This is an application example where the width set to CR01n (4 clocks in this example) is to be output from the TO0n pin when the count value has been captured & cleared.

TM0n is cleared (to 0000H) at the rising edge detection of the TI00n pin and captured to CR00n at the falling edge detection of the TI00n pin. The TO0n output level is inverted when TM0n is cleared (to 0000H) because the rising edge of the TI00n pin has been detected or when the value of TM0n matches that of a compare register (CR01n).

When bit 1 (CRC0n1) of capture/compare control register 0n (CRC0n) is 1, the count value of TM0n is captured to CR00n in the phase reverse to that of the input signal of the TI00n pin, but the capture interrupt signal (INTTM00n) is not generated. However, the INTTM00n interrupt is generated when the valid edge of the TI01n pin is detected. Mask the INTTM00n signal when it is not used.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

7.4.7 One-shot pulse output operation

A one-shot pulse can be output by setting bits 3 and 2 (TMC0n3 and TMC0n2) of the 16-bit timer mode control register 0n (TMC0n) to 01 (free-running timer mode) or to 10 (clear & start mode entered by the TI00n pin valid edge) and setting bit 5 (OSPE0n) of 16-bit timer output control register 0n (TOC0n) to 1.

When bit 6 (OSPT0n) of TOC0n is set to 1 or when the valid edge is input to the TI00n pin during timer operation, clearing & starting of TM0n is triggered, and a pulse of the difference between the values of CR00n and CR01n is output only once from the TO0n pin.

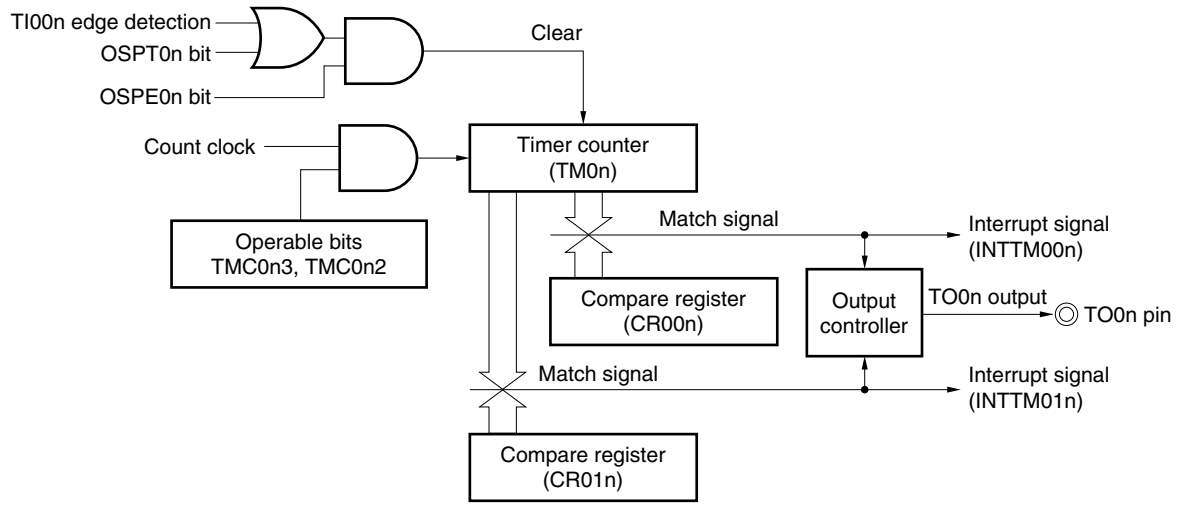
Cautions 1. Do not input the trigger again (setting OSPT0n to 1 or detecting the valid edge of the TI00n pin) while the one-shot pulse is output. To output the one-shot pulse again, generate the trigger after the current one-shot pulse output has completed.

2. To use only the setting of OSPT0n to 1 as the trigger of one-shot pulse output, do not change the level of the TI00n pin or its alternate function port pin. Otherwise, the pulse will be unexpectedly output.

Remarks 1. For the setting of the I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 7-48. Block Diagram of One-Shot Pulse Output Operation



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(b) Parity types and operation

The parity bit is used to detect a bit error in communication data. Usually, the same type of parity bit is used on both the transmission and reception sides. With even parity and odd parity, a 1-bit (odd number) error can be detected. With zero parity and no parity, an error cannot be detected.

(i) Even parity

- Transmission

  Transmit data, including the parity bit, is controlled so that the number of bits that are "1" is even.
  The value of the parity bit is as follows.

  If transmit data has an odd number of bits that are "1": 1
  If transmit data has an even number of bits that are "1": 0

- Reception

  The number of bits that are "1" in the receive data, including the parity bit, is counted. If it is odd, a parity error occurs.

(ii) Odd parity

- Transmission

  Unlike even parity, transmit data, including the parity bit, is controlled so that the number of bits that are "1" is odd.

  If transmit data has an odd number of bits that are "1": 0
  If transmit data has an even number of bits that are "1": 1

- Reception

  The number of bits that are "1" in the receive data, including the parity bit, is counted. If it is even, a parity error occurs.

(iii) 0 parity

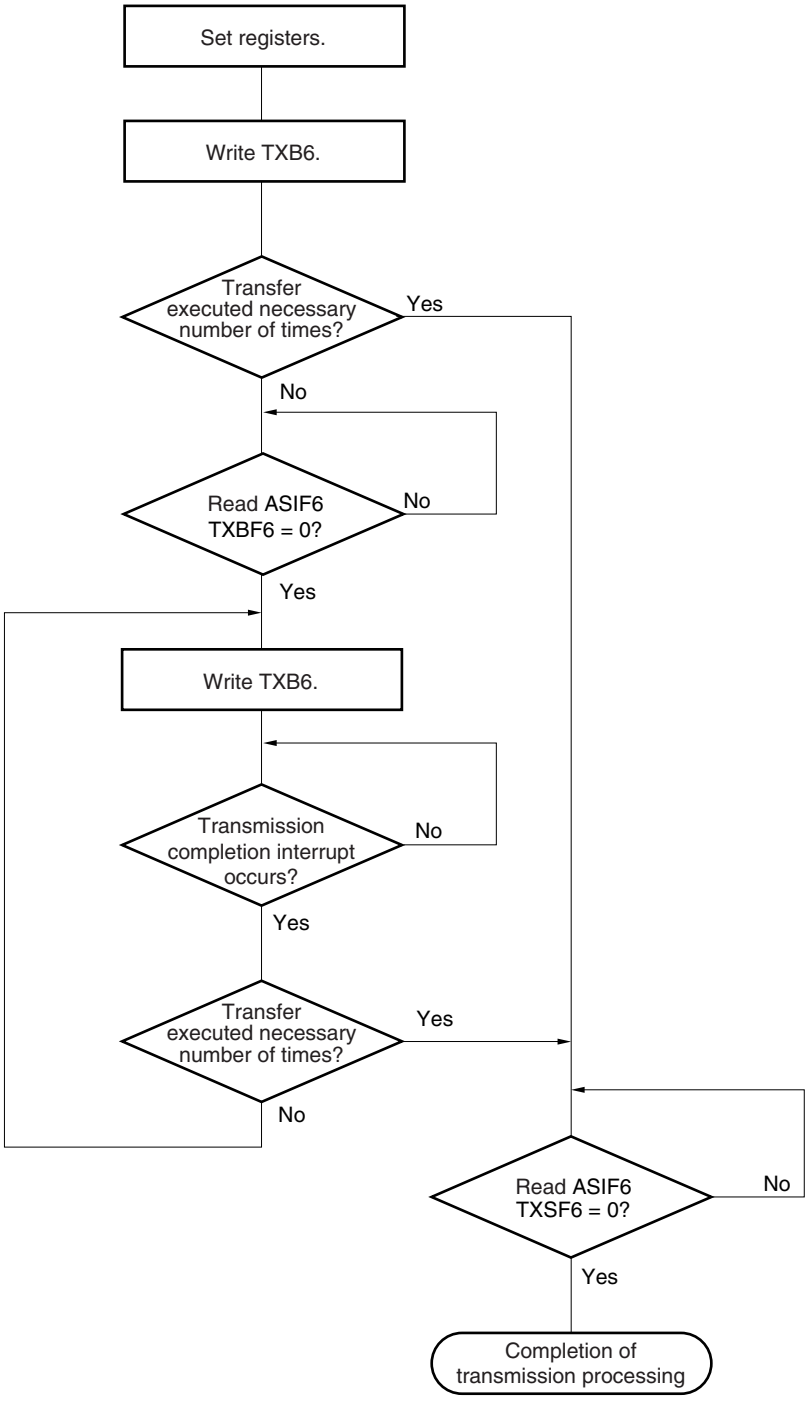
The parity bit is cleared to 0 when data is transmitted, regardless of the transmit data.
The parity bit is not detected when the data is received. Therefore, a parity error does not occur regardless of whether the parity bit is "0" or "1".

(iv) No parity

No parity bit is appended to the transmit data.
Reception is performed assuming that there is no parity bit when data is received. Because there is no parity bit, a parity error does not occur.

Figure 15-16 shows an example of the continuous transmission processing flow.

Figure 15-16. Example of Continuous Transmission Processing Flow



Remark TXB6: Transmit buffer register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6 (transmit buffer data flag)
TXSF6: Bit 0 of ASIF6 (transmit shift register data flag)

(5) IIC function expansion register 0 (IICX0)

This register sets the function expansion of I^2C.

IICX0 is set by a 1-bit or 8-bit memory manipulation instruction. The CLX0 bit is set in combination with bits 3, 1, and 0 (SMC0, CL01, and CL00) of IIC clock selection register 0 (IICCL0) (see **18.3 (6) I^2C transfer clock setting method**).

Set IICX0 while bit 7 (IICE0) of IIC control register 0 (IICC0) is 0.

Reset signal generation clears IICX0 to 00H.

Figure 18-9. Format of IIC Function Expansion Register 0 (IICX0)

Address: FFA9H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
IICX0	0	0	0	0	0	0	0	CLX0

(6) I^2C transfer clock setting method

The I^2C transfer clock frequency (f_{SCL}) is calculated using the following expression.

$$f_{SCL} = 1/(m \times T + t_R + t_F)$$

m = 12, 18, 24, 44, 66, 86 (see **Table 18-2 Selection Clock Setting**)

T: $1/f_W$

t_R: SCL0 rise time

t_F: SCL0 fall time

For example, the I^2C transfer clock frequency (f_{SCL}) when $f_W = f_{PRS}/2 = 4.19$ MHz, m = 86, $t_R = 200$ ns, and $t_F = 50$ ns is calculated using following expression.

$$f_{SCL} = 1/(88 \times 238.7 \text{ ns} + 200 \text{ ns} + 50 \text{ ns}) \cong 48.1 \text{ kHz}$$

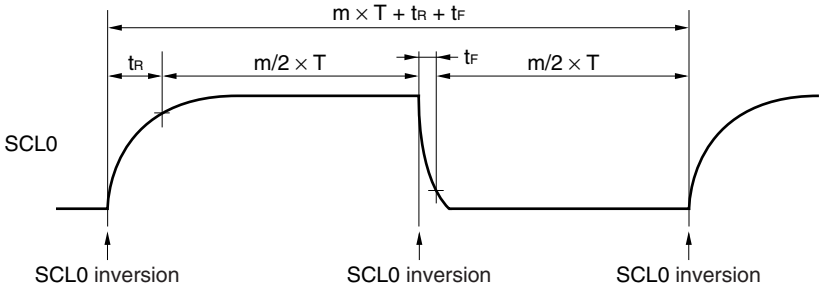


Figure 18-24. Master Operation in Multi-Master System (2/3)

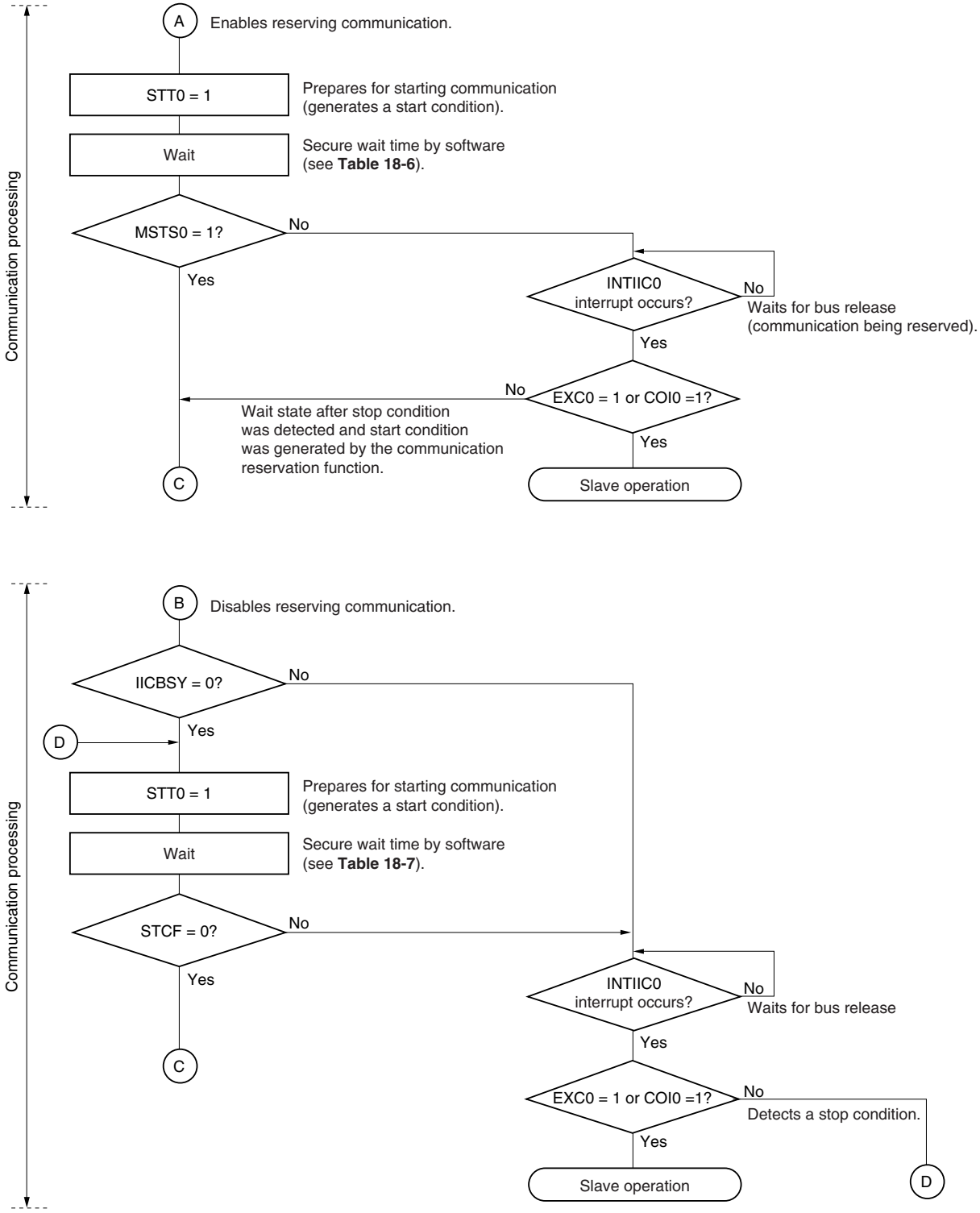


Table 22-2. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	HALT mode held
Reset	–	–	×	×	Reset processing

×: don't care

22.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

Caution Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

The operating statuses in the STOP mode are shown below.

Table 23-2. Hardware Statuses After Reset Acknowledgment (4/4)

Hardware		Status After Reset Acknowledgment[Note 1]
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 2]
	Low-voltage detection level selection register (LVIS)	00H[Note 2]
Interrupt	Request flag registers 0L, 0H, 1L, 1H (IF0L, IF0H, IF1L, IF1H)	00H
	Mask flag registers 0L, 0H, 1L, 1H (MK0L, MK0H, MK1L, MK1H)	FFH
	Priority specification flag registers 0L, 0H, 1L, 1H (PR0L, PR0H, PR1L, PR1H)	FFH
	External interrupt rising edge enable register (EGP)	00H
	External interrupt falling edge enable register (EGN)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
RESF	WDTRF flag	Cleared (0)	Cleared (0)	Set (1)	Held
	LVIRF flag			Held	Set (1)
LVIM		Cleared (00H)	Cleared (00H)	Cleared (00H)	Held
LVIS					

Remark The special function register (SFR) mounted depend on the product. See **3.2.3 Special function registers (SFRs)**.

(3) Port mode register 12 (PM12)

When using the P120/EXLVI/INTP0 pin for external low-voltage detection potential input, set PM120 to 1. At this time, the output latch of P120 may be 0 or 1.

PM12 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM12 to FFH.

Figure 25-4. Format of Port Mode Register 12 (PM12)

Address: FF2CH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	PM124	PM123	PM122	PM121	PM120

PM12n	P12n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The format of port mode register 12 of 78K0/KB2 products is different from the above format. See **5.3 Registers Controlling Port Function (1) Port mode registers (PMxx)**.

25.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

(1) Used as reset (LVIMD = 1)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), generates an internal reset signal when $V_{DD} < V_{LVI}$, and releases internal reset when $V_{DD} \geq V_{LVI}$.
- If LVISEL = 1, compares the input voltage from external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V (TYP.)), generates an internal reset signal when EXLVI < V_{EXLVI}, and releases internal reset when EXLVI ≥ V_{EXLVI}.

(2) Used as interrupt (LVIMD = 0)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}). When V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$), generates an interrupt signal (INTLVI).
- If LVISEL = 1, compares the input voltage from external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V (TYP.)). When EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}), generates an interrupt signal (INTLVI).

While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

Remark LVIMD: Bit 1 of low-voltage detection register (LVIM)
LVISEL: Bit 2 of LVIM

CHAPTER 29 INSTRUCTION SET

This chapter lists each instruction set of the 78K0/Kx2 microcontrollers in table form. For details of each operation and operation code, refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

29.1 Conventions Used in Operation List

29.1.1 Operand identifiers and specification methods

Operands are written in the "Operand" column of each instruction in accordance with the specification method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more methods, select one of them. Uppercase letters and the symbols #, !, $ and [ ] are keywords and must be written as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to write the #, !, $, and [ ] symbols.

For operand register identifiers r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for specification.

Table 29-1. Operand Identifiers and Specification Methods

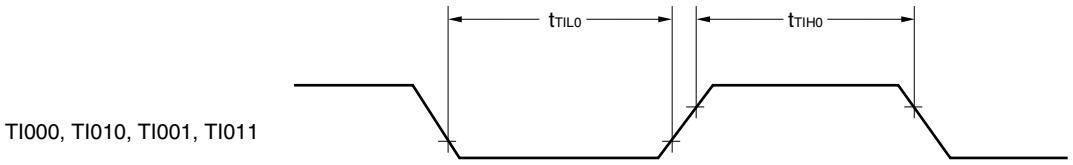
Identifier	Specification Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol[Note]
sfrp	Special function register symbol (16-bit manipulatable register even addresses only)[Note]
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even address only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr11	0800H to 0FFFH Immediate data or labels
addr5	0040H to 007FH Immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

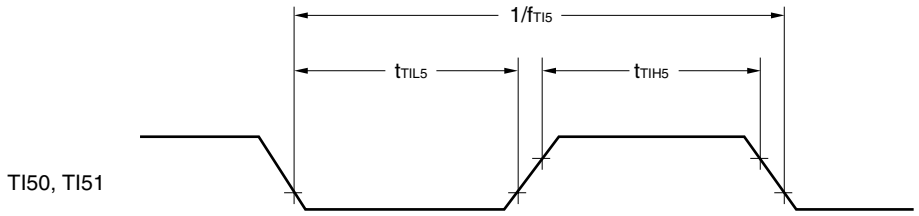
Note Addresses from FFD0H to FFDFH cannot be accessed with these operands.

Remark For special function register symbols, see **Table 3-8 Special Function Register List**.

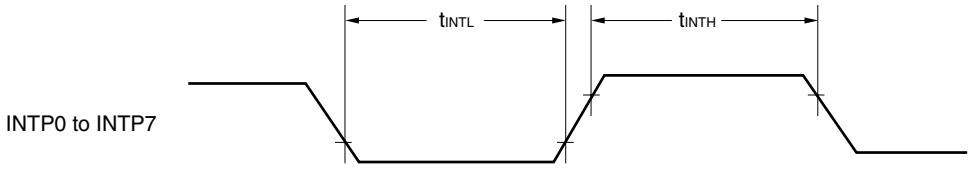
Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

TI Timing

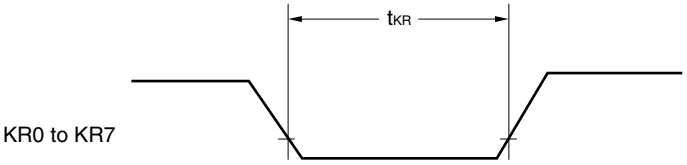




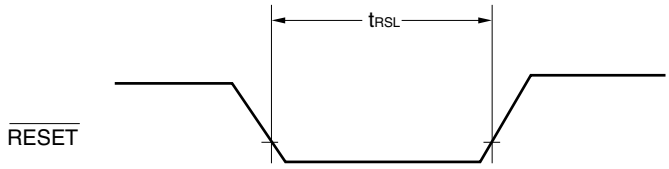
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

2.7 V POC Circuit Characteristics (T_A = –40 to +125°C, V_{SS} = EV_{SS} = 0 V)

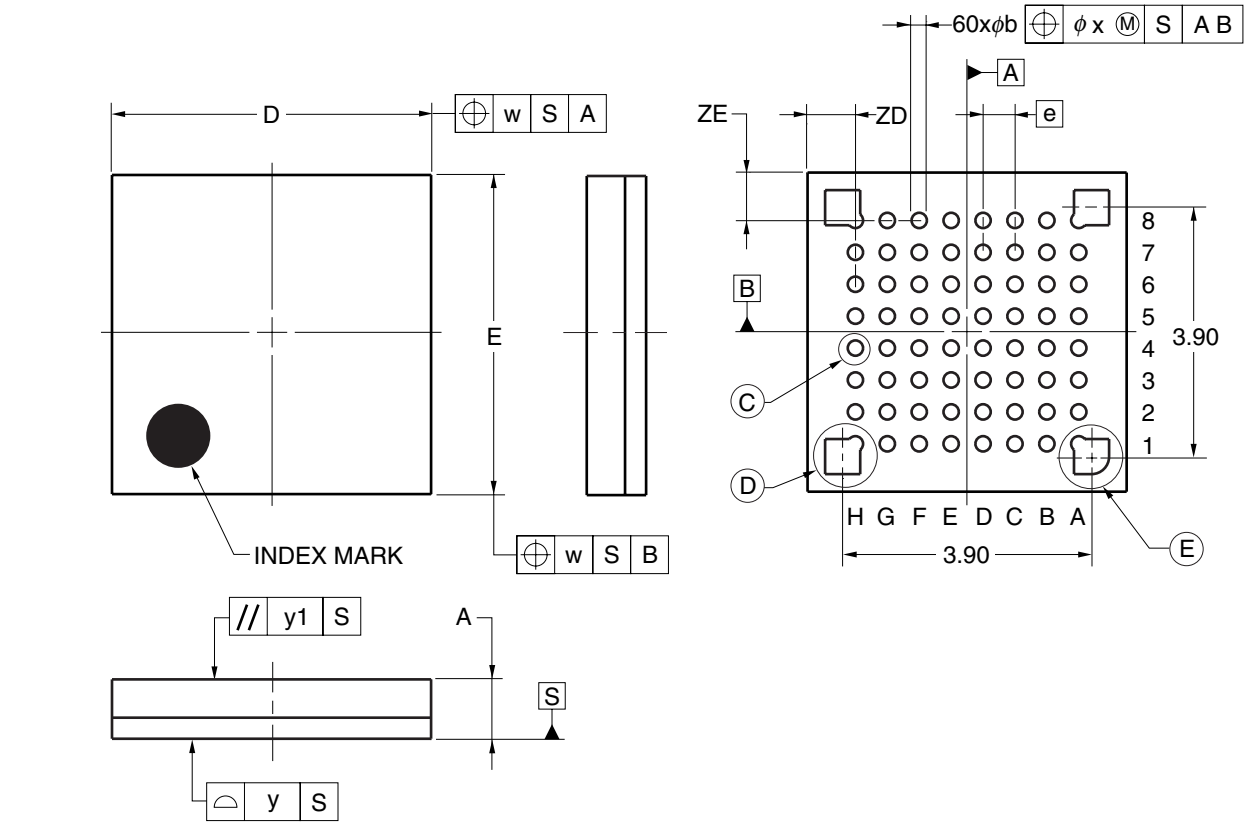
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option bye) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

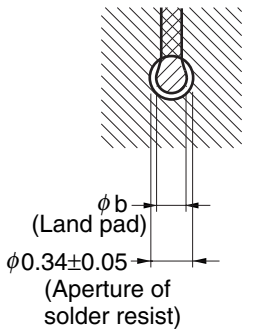
Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until V_{POC} = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC}, similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until V_{DDPOC} = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at V_{POC} = 1.59 V (TYP.) and not at V_{DDPOC}. The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH}.

- μPD78F0531FC-AA1-A, 78F0532FC-AA1-A, 78F0533FC-AA1-A, 78F0534FC-AA1-A, 78F0535FC-AA1-A, 78F0536FC-AA1-A, 78F0537FC-AA1-A, 78F0537DFC-AA1-A
- μPD78F0531AFC-AA1-A, 78F0532AFC-AA1-A, 78F0533AFC-AA1-A, 78F0534AFC-AA1-A, 78F0535AFC-AA1-A, 78F0536AFC-AA1-A, 78F0537AFC-AA1-A, 78F0537DAFC-AA1-A

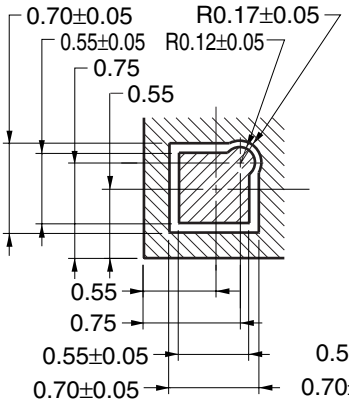
64-PIN PLASTIC FLGA(5x5)



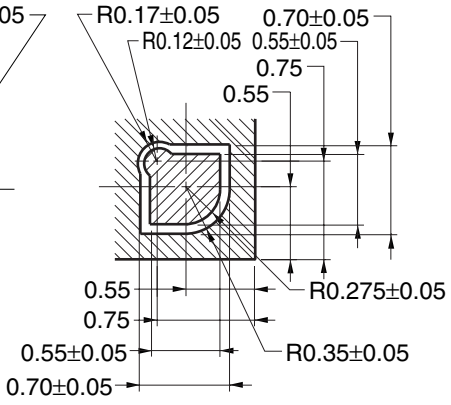
DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART



DETAIL OF Ⓔ PART

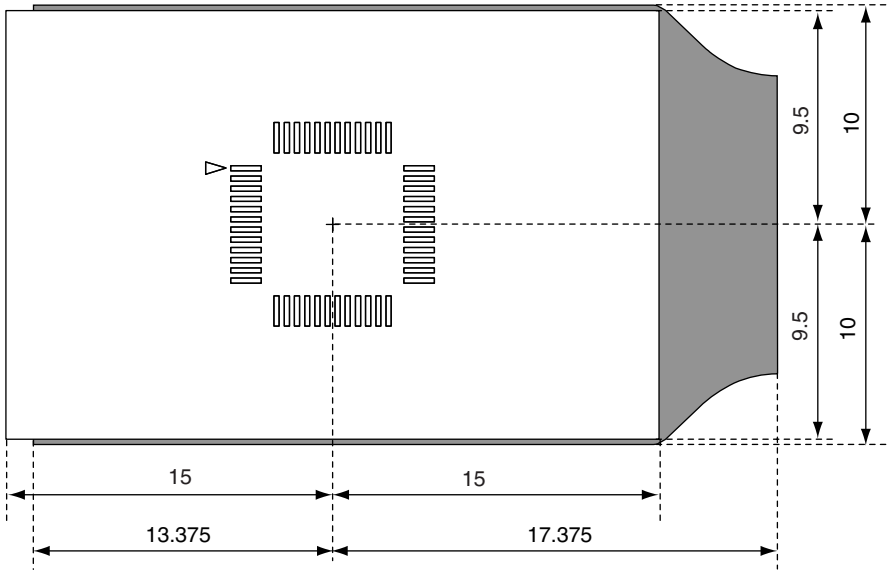


(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.91±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AA1-1

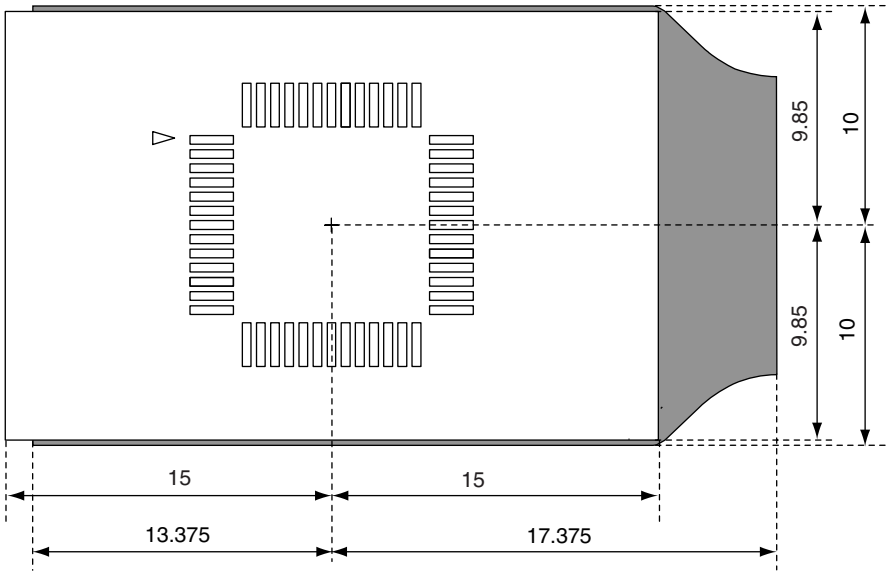
Figure B-4. For 48-Pin GA Package



□: Exchange adapter area: Components up to 17.45 mm in height can be mounted[Note]
■: Emulation probe tip area: Components up to 24.45 mm in height can be mounted[Note]

Note Height can be adjusted by using space adapters (each adds 2.4 mm)

Figure B-5. For 52-Pin GB Package



□: Exchange adapter area: Components up to 17.45 mm in height can be mounted[Note]
■: Emulation probe tip area: Components up to 24.45 mm in height can be mounted[Note]

Note Height can be adjusted by using space adapters (each adds 2.4 mm)

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 7	Soft	16-bit timer/event counters 00, 01	PRM0n: Prescaler mode register 0n	Do not apply the following setting when setting the PRM0n1 and PRM0n0 bits to 11 (to specify the valid edge of the TI00n pin as a count clock). • Clear & start mode entered by the TI00n pin valid edge • Setting the TI00n pin as a capture trigger	p. 285 ☐
				If the operation of the 16-bit timer/event counter 0n is enabled when the TI00n or TI01n pin is at high level and when the valid edge of the TI00n or TI01n pin is specified to be the rising edge or both edges, the high level of the TI00n or TI01n pin is detected as a rising edge. Note this when the TI00n or TI01n pin is pulled up. However, the rising edge is not detected when the timer operation has been once stopped and then is enabled again.	p. 285 ☐
	Hard			The valid edge of TI010 and timer output (TO00) cannot be used for the P01 pin at the same time, and the valid edge of TI011 and timer output (TO01) cannot be used for the P06 pin at the same time. Select either of the functions.	p. 285 ☐
	Soft		Clear & start mode entered by TI00n pin valid edge input	Do not set the count clock as the valid edge of the TI00n pin (PRM0n1 and PRM0n0 = 11). When PRM0n1 and PRM0n0 = 11, TM0n may be cleared.	p. 299 ☐
			PPG output	To change the duty factor (value of CR01n) during operation, see 7.5.1 Rewriting CR01n during TM0n operation.	p. 321 ☐
				Set values to CR00n and CR01n such that the condition 0000H ≤ CR01n < CR00n ≤ FFFFH is satisfied.	p. 323 ☐
			One-shot pulse output	Do not input the trigger again (setting OSPT0n to 1 or detecting the valid edge of the TI00n pin) while the one-shot pulse is output. To output the one-shot pulse again, generate the trigger after the current one-shot pulse output has completed.	p. 325 ☐
				To use only the setting of OSPT0n to 1 as the trigger of one-shot pulse output, do not change the level of the TI00n pin or its alternate function port pin. Otherwise, the pulse will be unexpectedly output.	p. 325 ☐
				Do not set the same value to CR00n and CR01n.	p. 327 ☐
			LVS0n, LVRn0	Be sure to set LVS0n and LVR0n following steps <1>, <2>, and <3> above. Step <2> can be performed after <1> and before <3>.	p. 339 ☐
			–	Table 7-3 shows the restrictions for each channel.	p. 340 ☐
	Hard		Timer start errors	An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM0n is started asynchronously to the count pulse.	p. 340 ☐
	Soft		CR00n, CR01n: 16-bit timer capture/compare registers 00n, 01n	Set a value other than 0000H to CR00n and CR01n in clear & start mode entered upon a match between TM0n and CR00n (TM0n cannot count one pulse when it is used as an external event counter).	p. 340 ☐
				When the valid edge is input to the TI00n/TI01n pin and the reverse phase of the TI00n pin is detected while CR00n/CR01n is read, CR01n performs a capture operation but the read value of CR00n/CR01n is not guaranteed. At this time, an interrupt signal (INTTM00n/INTTM01n) is generated when the valid edge of the TI00n/TI01n pin is detected (the interrupt signal is not generated when the reverse-phase edge of the TI00n pin is detected). When the count value is captured because the valid edge of the TI00n/TI01n pin was detected, read the value of CR00n/CR01n after INTTM00n/INTTM01n is generated.	p. 341 ☐
				The values of CR00n and CR01n are not guaranteed after 16-bit timer/event counter 0n stops.	p. 341 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 14	Soft	Serial interface UART0	UART mode	If clock supply to serial interface UART0 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART0 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD0 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER0 = 0, RXE0 = 0, and TXE0 = 0.	p. 432 ☐
				Set POWER0 = 1 and then set TXE0 = 1 (transmission) or RXE0 = 1 (reception) to start communication.	p. 432 ☐
				TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.	p. 432 ☐
				Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.	pp. 432, 435 ☐
			TXS0: Transmit shift register 0	Do not write the next transmit data to TXS0 before the transmission completion interrupt signal (INTST0) is generated.	p. 435 ☐
			ASIM0: Asynchronous serial interface operation mode register 0	To start the transmission, set POWER0 to 1 and then set TXE0 to 1. To stop the transmission, clear TXE0 to 0, and then clear POWER0 to 0.	p. 437 ☐
				To start the reception, set POWER0 to 1 and then set RXE0 to 1. To stop the reception, clear RXE0 to 0, and then clear POWER0 to 0.	p. 437 ☐
				Set POWER0 to 1 and then set RXE0 to 1 while a high level is input to the RxD0 pin. If POWER0 is set to 1 and RXE0 is set to 1 while a low level is input, reception is started.	p. 437 ☐
				TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.	p. 437 ☐
				Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.	p. 437 ☐
				Clear the TXE0 and RXE0 bits to 0 before rewriting the PS01, PS00, and CL0 bits.	p. 437 ☐
				Make sure that TXE0 = 0 when rewriting the SL0 bit. Reception is always performed with “number of stop bits = 1”, and therefore, is not affected by the set value of the SL0 bit.	p. 437 ☐
				Be sure to set bit 0 to 1.	p. 437 ☐
			ASIS0: Asynchronous serial interface reception error status register 0	The operation of the PE0 bit differs depending on the set values of the PS01 and PS00 bits of asynchronous serial interface operation mode register 0 (ASIM0)	p. 438 ☐
				Only the first bit of the receive data is checked as the stop bit, regardless of the number of stop bits.	p. 438 ☐
				If an overrun error occurs, the next receive data is not written to receive buffer register 0 (RXB0) but discarded.	p. 438 ☐
				If data is read from ASIS0, a wait cycle is generated. Do not read data from ASIS0 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.	p. 438 ☐
			BRGC0: Baud rate generator control register 0	Make sure that bit 6 (TXE0) and bit 5 (RXE0) of the ASIM0 register = 0 when rewriting the MDL04 to MDL00 bits.	p. 440 ☐
				Make sure that bit 7 (POWER0) of the ASIM0 register = 0 when rewriting the TPS01 and TPS00 bits.	p. 440 ☐
	Hard			The baud rate value is the output clock of the 5-bit counter divided by 2.	p. 440 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 20	Soft	Interrupt function	1F0L, 1F0L, 1F1L, 1F1H: Interrupt request flag registers	When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.	p. 637 ☐

				When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as “IF0L.0 = 0;” or “_asm(“clr1 IF0L, 0”);” because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).
				If a program is described in C language using an 8-bit memory manipulation instruction such as “IF0L &= 0xfe;” and compiled, it becomes the assembler of three instructions.
				mov a, IF0L
				and a, #0FEH
				mov IF0L, a
				In this case, even if the request flag of another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between “mov a, IF0L” and “mov IF0L, a”, the flag is cleared to 0 at “mov IF0L, a”. Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.
					p. 637 ☐

				Be sure to clear bits 2, 4 to 7 of IF1L and bits 1 to 7 of IF1H to 0. (78K0/KB2)	p. 638 ☐
				Be sure to clear bits 6 and 7 of IF1L to 0 in the 38-pin and 44-pin products. Be sure to clear bit 7 of IF1L to 0 in the 48-pin products.	p. 639 ☐
				Be sure to clear bits 1 to 7 of IF1H to 0. (78K0/KC2)	p. 639 ☐
				Be sure to clear bit 7 of 1F1L and bits 1 to 7 of IF1H to 0. (78K0/KD2)	p. 640 ☐
				Be sure to clear bits 1 to 7 of IF1H to 0 for the products whose flash memory is less than 32 KB. Be sure to clear bits 4 to 7 of IF1H to 0 for the products whose flash memory is at least 48 KB. (78K0/KE2)	p. 641 ☐
				Be sure to clear bits 5 to 7 of IF1H to 0. (78K0/KF2)	p. 642 ☐
			MK0L, MK0H, MK1L, MK1H: Interrupt mask flag registers	Be sure to set bits 2, 4 to 7 of MK1L and bits 1 to 7 of MK1H to 1. (78K0/KB2)	p. 643 ☐
				Be sure to set bits 6 and 7 of MK1L to 1 in the 38-pin and 44-pin products. Be sure to set bit 7 of MK1L to 1 in the 48-pin products. Be sure to set bits 1 to 7 of MK1H to 1. (78K0/KC2)	p. 644 ☐
				Be sure to set bit 7 of MK1L and bits 1 to 7 of MK1H to 1. (78K0/KD2)	p. 645 ☐
				Be sure to set bits 1 to 7 of MK1H to 1 for the products whose flash memory is less than 32 KB. Be sure to set bits 4 to 7 of MK1H to 1 for the products whose flash memory is at least 48 KB. (78K0/KE2)	p. 646 ☐
				Be sure to set bits 5 to 7 of MK1H to 1. (78K0/KF2)	p. 647 ☐
			PR0L, PR0H, PR1L, PR1H: Priority specification flag registers	Be sure to set bits 2, 4 to 7 of PR1L and bits 1 to 7 of PR1H to 1. (78K0/KB2)	p. 648 ☐
				Be sure to set bits 6 and 7 of PR1L to 1 in the 38-pin and 44-pin products. Be sure to set bit 7 of PR1L to 1 in the 48-pin products. Be sure to set bits 1 to 7 of PR1H to 1. (78K0/KC2)	p. 649 ☐
				Be sure to set bit 7 of PR1L and bits 1 to 7 of PR1H to 1. (78K0/KD2)	p. 650 ☐
				Be sure to set bits 1 to 7 of PR1H to 1 for the products whose flash memory is less than 32 KB. Be sure to set bits 4 to 7 of PR1H to 1 for the products whose flash memory is at least 48 KB. (78K0/KE2)	p. 651 ☐
				Be sure to set bits 5 to 7 of PR1H to 1. (78K0/KF2)	p. 652 ☐