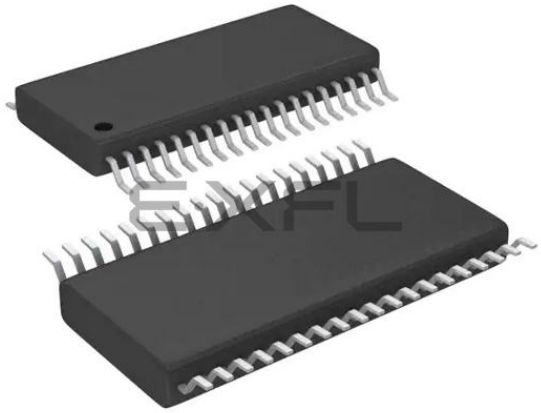
Renesas Electronics America Inc - UPD78F0512AMC-GAA-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TSSOP (0.240", 6.10mm Width)
Supplier Device Package	38-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0512amc-gaa-ax

Documents Related to Development Tools (Software)

Document Name		Document No.
RA78K0 Ver.3.80 Assembler Package User's Manual [Note 1]	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
78K0 Assembler Package RA78K0 Ver.4.01 Operating Precautions (Notification Document) [Note 1]		ZUD-CD-07-0181-E
CC78K0 Ver.3.70 C Compiler User's Manual [Note 2]	Operation	U17201E
	Language	U17200E
78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions (Notification Document) [Note 2]		ZUD-CD-07-0103-E
SM+ System Simulator User's Manual	Operation	U18601E
	User Open Interface	U18212E
ID78K0-QB Ver.2.94 Integrated Debugger User's Manual	Operation	U18330E
ID78K0-QB Ver.3.00 Integrated Debugger User's Manual	Operation	U18492E
PM plus Ver.5.20[Note 3] User's Manual		U16934E
PM+ Ver.6.30[Note 4] User's Manual		U18416E

Notes 1. This document is installed into the PC together with the tool when installing RA78K0 Ver. 4.01. For descriptions not included in "78K0 Assembler Package RA78K0 Ver. 4.01 Operating Precautions", refer to the user's manual of RA78K0 Ver. 3.80.

2. This document is installed into the PC together with the tool when installing CC78K0 Ver. 4.00. For descriptions not included in "78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions", refer to the user's manual of CC78K0 Ver. 3.70.

3. PM plus Ver. 5.20 is the integrated development environment included with RA78K0 Ver. 3.80.

4. PM+ Ver. 6.30 is the integrated development environment included with RA78K0 Ver. 4.01. Software tool (assembler, C compiler, debugger, and simulator) products of different versions can be managed.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE – Products and Packages –	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Device Mount Manual" website (http://www2.renesas.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

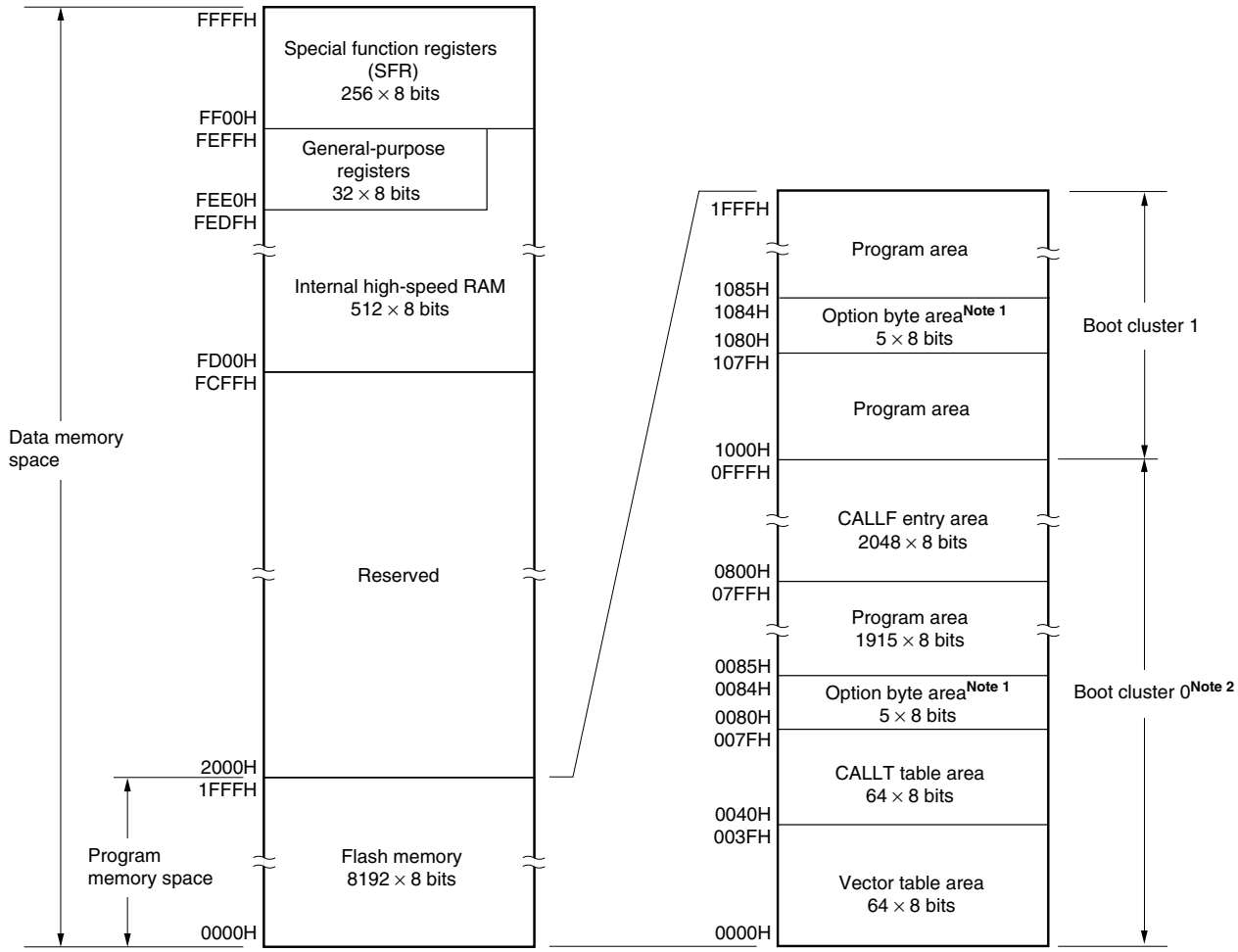
Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

(6/6)

78K0/Kx2 Microcontrollers	Package	Product type	Quality grace	Part Number
78K0/KE2	64-pin plastic FLGA (5x5)	Conventional-specification products	Standard products	μPD78F0531FC-AA1-A, 78F0532FC-AA1-A, 78F0533FC-AA1-A, 78F0534FC-AA1-A, 78F0535FC-AA1-A, 78F0536FC-AA1-A, 78F0537FC-AA1-A, 78F0537DFC-AA1-A[Note]
		Expanded-specification products	Standard products	μPD78F0531AFC-AA1-A, 78F0532AFC-AA1-A, 78F0533AFC-AA1-A, 78F0534AFC-AA1-A, 78F0535AFC-AA1-A, 78F0536AFC-AA1-A, 78F0537AFC-AA1-A, 78F0537DAFC-AA1-A[Note]
<R>	64-pin plastic FBGA (4x4)	Expanded-specification products	Standard products	μPD78F0531AF1-AA2-A, 78F0532AF1-AA2-A, 78F0533AF1-AA2-A, 78F0534AF1-AA2-A, 78F0535AF1-AA2-A, 78F0536AF1-AA2-A, 78F0537AF1-AA2-A, 78F0537DAF1-AA2-A[Note]
78K0/KF2	80-pin plastic LQFP (14x14)	Conventional-specification products	Standard products	μPD78F0544GC-UBT-A, 78F0545GC-UBT-A, 78F0546GC-UBT-A, 78F0547GC-UBT-A, 78F0547DGC-UBT-A[Note]
			(A) grade products	μPD78F0544GC(A)-GAD-AX, 78F0545GC(A)-GAD-AX, 78F0546GC(A)-GAD-AX, 78F0547GC(A)-GAD-AX
			(A2) grade products	μPD78F0544GC(A2)-GAD-AX, 78F0545GC(A2)-GAD-AX, 78F0546GC(A2)-GAD-AX, 78F0547GC(A2)-GAD-AX
		Expanded-specification products	Standard products	μPD78F0544AGC-GAD-AX, 78F0545AGC-GAD-AX, 78F0546AGC-GAD-AX, 78F0547AGC-GAD-AX, 78F0547DAGC-GAD-AX[Note]
			(A) grade products	μPD78F0544AGCA-GAD-G, 78F0545AGCA-GAD-G, 78F0546AGCA-GAD-G, 78F0547AGCA-GAD-G
			(A2) grade products	μPD78F0544AGCA2-GAD-G, 78F0545AGCA2-GAD-G, 78F0546AGCA2-GAD-G, 78F0547AGCA2-GAD-G
	80-pin plastic LQFP (fine pitch) (12x12)	Conventional-specification products	Standard products	μPD78F0544GK-8EU-A, 78F0545GK-8EU-A, 78F0546GK-8EU-A, 78F0547GK-8EU-A, 78F0547DGK-8EU-A[Note]
			(A) grade products	μPD78F0544GK(A)-GAK-AX, 78F0545GK(A)-GAK-AX, 78F0546GK(A)-GAK-AX, 78F0547GK(A)-GAK-AX
			(A2) grade products	μPD78F0544GK(A2)-GAK-AX, 78F0545GK(A2)-GAK-AX, 78F0546GK(A2)-GAK-AX, 78F0547GK(A2)-GAK-AX
		Expanded-specification products	Standard products	μPD78F0544AGK-GAK-AX, 78F0545AGK-GAK-AX, 78F0546AGK-GAK-AX, 78F0547AGK-GAK-AX, 78F0547DAGK-GAK-AX[Note]
			(A) grade products	μPD78F0544AGKA-GAK-G, 78F0545AGKA-GAK-G, 78F0546AGKA-GAK-G, 78F0547AGKA-GAK-G
			(A2) grade products	μPD78F0544AGKA2-GAK-G, 78F0545AGKA2-GAK-G, 78F0546AGKA2-GAK-G, 78F0547AGKA2-GAK-G

Note The μPD78F0537D, 78F0537DA, 78F0547D, and 78F0547DA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

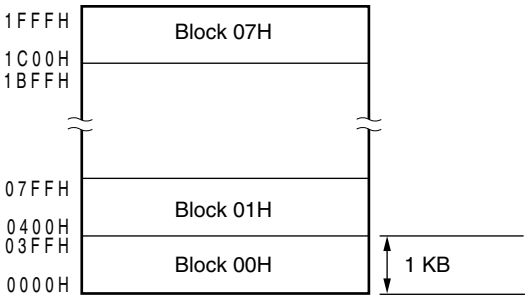
Figure 3-1. Memory Map (μPD78F0500 and 78F0500A)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H.
When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.



CHAPTER 4 MEMORY BANK SELECT FUNCTION (PRODUCTS WHOSE FLASH MEMORY IS AT LEAST 96 KB ONLY)

4.1 Memory Bank

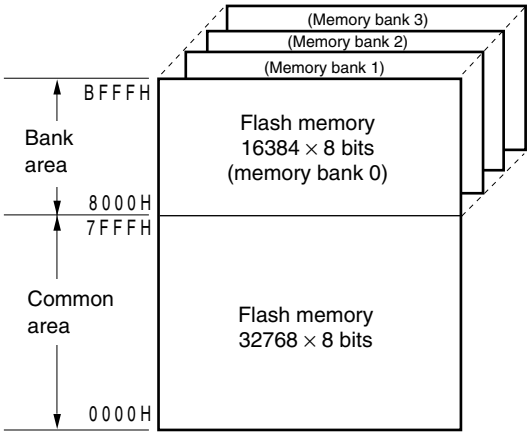
The μPD78F05x6, 78F05x6A, 78F05x7, 78F05x7A, 78F05x7D and 78F05x7DA of 78K0/KD2, 78K0/KE2, and 78K0/KF2 implement a ROM capacity of 96 KB or 128 KB by selecting a memory bank from a memory space of 8000H to BFFFH.

The μPD78F05x6 and 78F05x6A have memory banks 0 to 3, and the μPD78F05x7, 78F05x7A, 78F05x7D and 78F05x7DA have memory banks 0 to 5, as shown below.

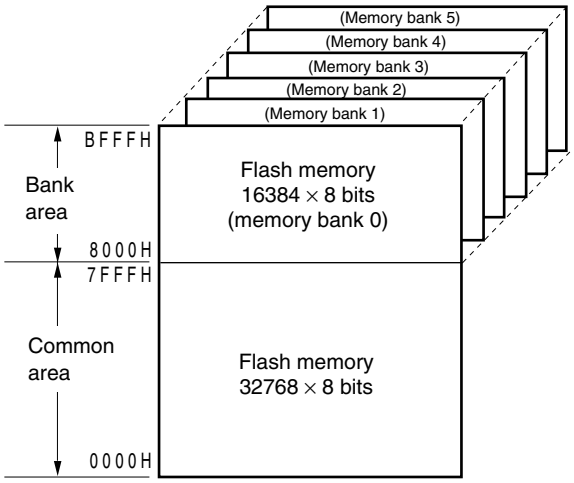
The memory banks are selected by using a memory bank select register (BANK).

Figure 4-1. Internal ROM (Flash Memory) Configuration

(a) μPD78F05x6 and 78F05x6A (products whose flash memory is 96 KB)



(b) μPD78F05x7, 78F05x7A, 78F05x7D, and 78F05x7DA (products whose flash memory is 128 KB)



Remark x = 2 to 4

Figure 5-31. Format of Port Mode Register (78K0/KD2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM4	1	1	1	1	1	1	PM41	PM40	FF24H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FF27H	FFH	R/W
PM12	1	1	1	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W
PM14	1	1	1	1	1	1	1	PM140	FF2EH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 4, 6, 7, 12, 14; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 4 to 7 of PM0, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 5 to 7 of PM12, and bits 1 to 7 of PM14 to 1.

Figure 5-43. Format of Pull-up Resistor Option Register (78K0/KF2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00	FF30H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40	FF34H	00H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	FF35H	00H	R/W
PU6	PU67	PU66	PU65	PU64	0	0	0	0	FF36H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	FF37H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W
PU14	0	0	PU145	PU144	PU143	PU142	PU141	PU140	FF3EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 7, 12, 14; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

(4) A/D port configuration register (ADPC)

This register switches the P20/ANI0 to P27/ANI7 pins to digital I/O of port or analog input of A/D converter.

ADPC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark P20/ANI0 to P23/ANI3 pins: 78K0/KB2
P20/ANI0 to P25/ANI5 pins: 38-pin products of 78K0/KC2
P20/ANI0 to P27/ANI7 pins: Products other than above

6.4 System Clock Oscillator

6.4.1 X1 oscillator

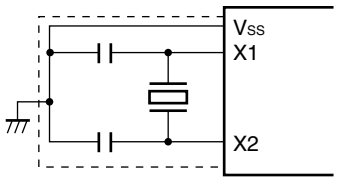
The X1 oscillator oscillates with a crystal resonator or ceramic resonator (1 to 20 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

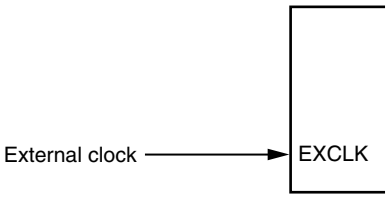
Figure 6-12 shows an example of the external circuit of the X1 oscillator.

Figure 6-12. Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



Cautions are listed on the next page.

6.4.2 XT1 oscillator

The XT1 oscillator[Note] oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

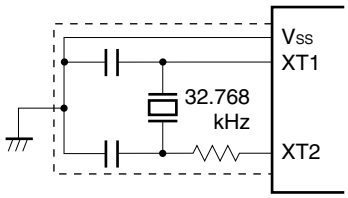
An external clock can also be input. In this case, input the clock signal to the EXCLKS pin.

Figure 6-13 shows an example of the external circuit of the XT1 oscillator.

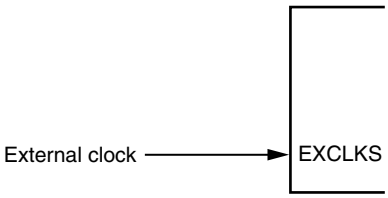
Note The 78K0/KB2 is not provided with an XT1 oscillator.

Figure 6-13. Example of External Circuit of XT1 Oscillator

(a) Crystal oscillation



(b) External clock



Cautions are listed on the next page.

6.6.3 Example of controlling subsystem clock

The following two types of subsystem clocks[Note] are available.

- XT1 clock: Crystal/ceramic resonator is connected across the XT1 and XT2 pins.
- External subsystem clock: External clock is input to the EXCLKS pin.

When the subsystem clock is not used, the XT1/P123 and XT2/EXCLKS/P124 pins can be used as I/O port pins.

Note The 78K0/KB2 is not provided with a subsystem clock.

Cautions 1. The XT1/P123 and XT2/EXCLKS/P124 pins are in the I/O port mode after a reset release.

2. Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

The following describes examples of setting procedures for the following cases.

(1) When oscillating XT1 clock
(2) When using external subsystem clock
(3) When using subsystem clock as CPU clock
(4) When stopping subsystem clock

(1) Example of setting procedure when oscillating the XT1 clock

<1> Setting XT1 and XT2 pins and selecting operation mode (PCC and OSCCTL registers)
When XTSTART, EXCLKS, and OSCSELS are set as any of the following, the mode is switched from port mode to XT1 oscillation mode.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	0	1	XT1 oscillation mode	Crystal/ceramic resonator connection	
1	×	×			

Remark ×: don't care

<2> Waiting for the stabilization of the subsystem clock oscillation
Wait for the oscillation stabilization time of the subsystem clock by software, using a timer function.

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

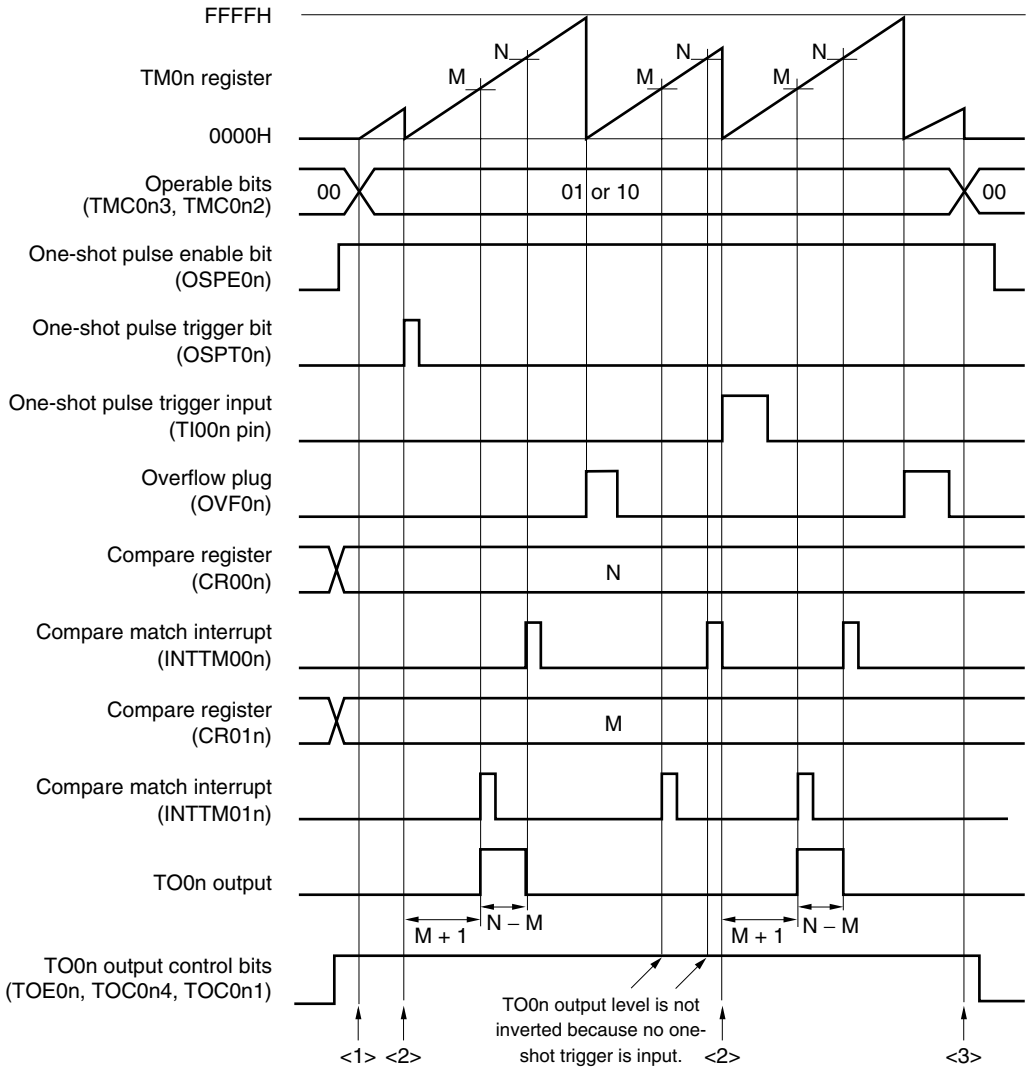
(2) Example of setting procedure when using the external subsystem clock

<1> Setting XT1 and XT2 pins, selecting XT1 clock/external clock and controlling oscillation (PCC and OSCCTL registers)
When XTSTART is cleared to 0 and EXCLKS and OSCSELS are set to 1, the mode is switched from port mode to external clock input mode. In this case, input the external clock to the EXCLKS/XT2/P124 pins.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	1	1	External clock input mode	I/O port	External clock input

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

Figure 7-50. Example of Software Processing for One-Shot Pulse Output Operation (1/2)



- Time from when the one-shot pulse trigger is input until the one-shot pulse is output
  = (M + 1) × Count clock cycle
- One-shot pulse output active level width
  = (N − M) × Count clock cycle

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2,] 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 9-5. Format of 8-Bit Timer H Mode Register 0 (TMHMD0)

Address: FF69H After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD0	TMHE0	CKS02	CKS01	CKS00	TMMD01	TMMD00	TOLEV0	TOEN0

TMHE0	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS02	CKS01	CKS00	Count clock selection[Note 1]				
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz	20 MHz[Note 3]
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
1	0	0	$f_{PRS}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.54 kHz
1	0	1	TM50 output[Note 4]				
Other than above			Setting prohibited				

TMMD01	TMMD00	Timer operation mode
0	0	Interval timer mode
1	0	PWM output mode
Other than above		Setting prohibited

TOLEV0	Timer output level control (in default mode)
0	Low level
1	High level

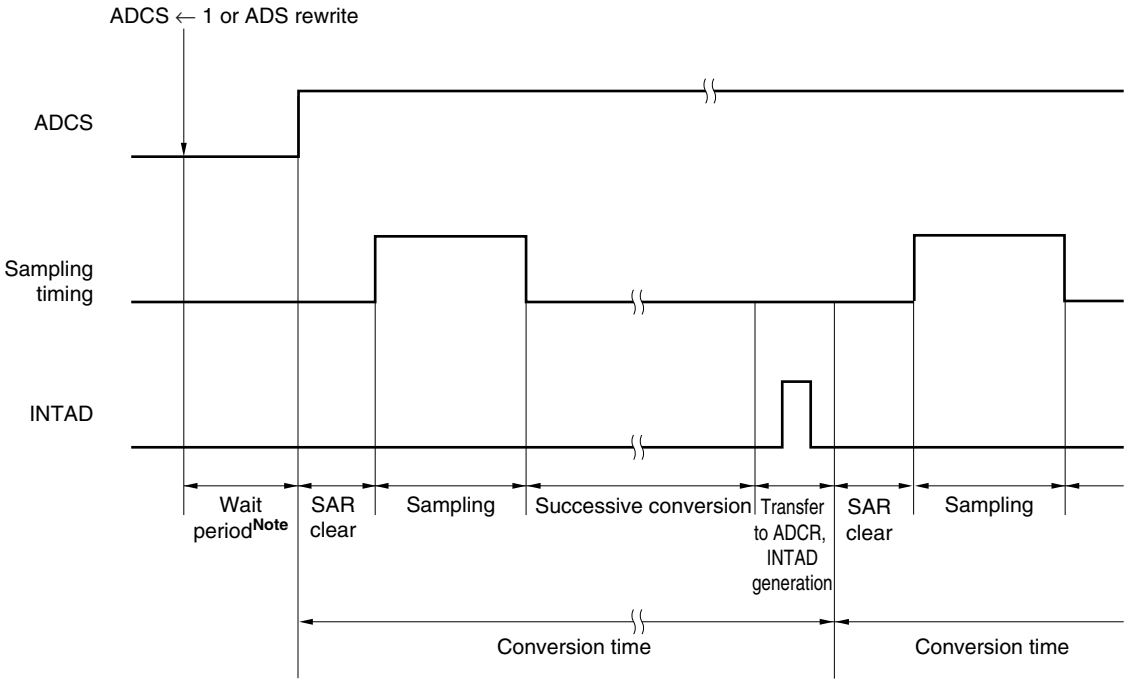
TOEN0	Timer output control
0	Disables output
1	Enables output

Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when $f_{PRS} = f_{XH}$ (XSEL = 1).)

Figure 13-5. A/D Converter Sampling and A/D Conversion Timing



Note For details of wait period, see **CHAPTER 36 CAUTIONS FOR WAIT**.

(2) 10-bit A/D conversion result register (ADCR)

This register is a 16-bit register that stores the A/D conversion result. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register. The higher 8 bits of the conversion result are stored in FF09H and the lower 2 bits are stored in the higher 2 bits of FF08H.

ADCR can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 13-6. Format of 10-Bit A/D Conversion Result Register (ADCR)

Address: FF08H, FF09H After reset: 0000H R

Symbol	FF09H								FF08H							
ADCR											0	0	0	0	0	0

Cautions 1. When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.

2. If data is read from ADCR, a wait cycle is generated. Do not read data from ADCR when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

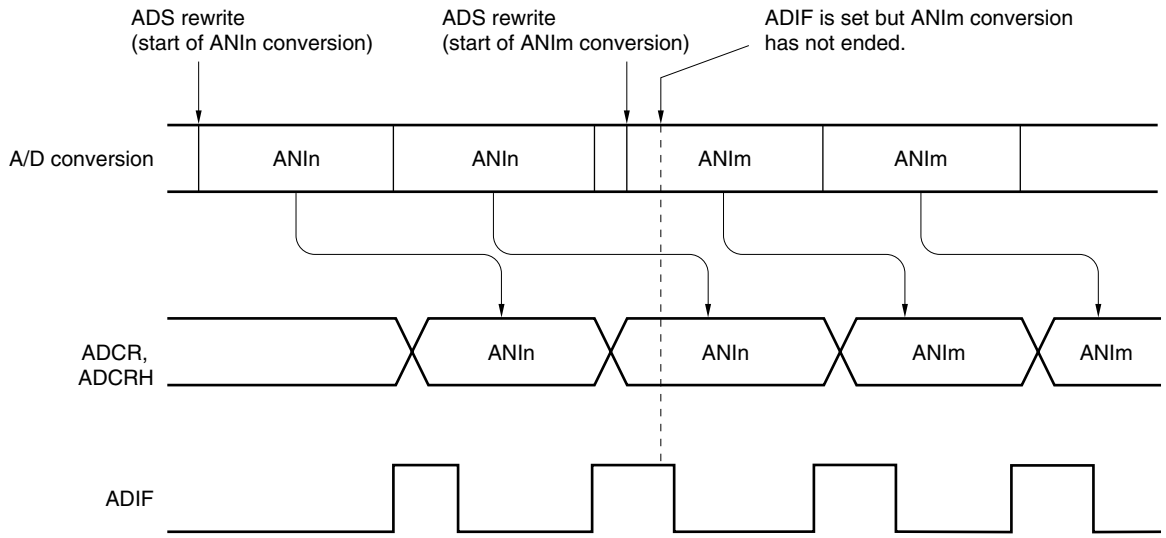
(8) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF for the pre-change analog input may be set just before the ADS rewrite. Caution is therefore required since, at this time, when ADIF is read immediately after the ADS rewrite, ADIF is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF before the A/D conversion operation is resumed.

Figure 13-21. Timing of A/D Conversion End Interrupt Request Generation



Remarks 1. 78K0/KB2: n = 0 to 3, 38-pin products of the 78K0/KC2: n = 0 to 5, other products: n = 0 to 7

2. 78K0/KB2: m = 0 to 3, 38-pin products of the 78K0/KC2: m = 0 to 5, other products: m = 0 to 7

(9) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1, or if the ADCS bit is set to 1 with the ADCE bit = 0. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(10) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using a timing other than the above may cause an incorrect conversion result to be read.

15.4 Operation of Serial Interface UART6

Serial interface UART6 has the following two modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode

15.4.1 Operation stop mode

In this mode, serial communication cannot be executed; therefore, the power consumption can be reduced. In addition, the pins can be used as ordinary port pins in this mode. To set the operation stop mode, clear bits 7, 6, and 5 (POWER6, TXE6, and RXE6) of ASIM6 to 0.

(1) Register used

The operation stop mode is set by asynchronous serial interface operation mode register 6 (ASIM6).

ASIM6 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM6	POWER6	TXE6	RXE6	PS61	PS60	CL6	SL6	ISRM6

POWER6	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].

TXE6	Enables/disables transmission
0	Disables transmission operation (synchronously resets the transmission circuit).

RXE6	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).

Notes 1. If POWER6 = 0 is set while transmitting data, the output of the TxD6 pin will be fixed to high level (if TXDLV6 = 0). Furthermore, the input from the RxD6 pin will be fixed to high level.

2. Asynchronous serial interface reception error status register 6 (ASIS6), asynchronous serial interface transmission status register 6 (ASIF6), bit 7 (SBRF6) and bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6), and receive buffer register 6 (RXB6) are reset.

Caution Clear POWER6 to 0 after clearing TXE6 and RXE6 to 0 to stop the operation.
To start the communication, set POWER6 to 1, and then set TXE6 or RXE6 to 1.

Remark To use the RxD6/P14 and TxD6/P13 pins as general-purpose port pins, see **CHAPTER 5 PORT FUNCTIONS**.

20.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 20-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 20-22 shows multiple interrupt servicing examples.

Table 20-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request				Software Interrupt Request
		PR = 0		PR = 1		
		IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP = 0	○	×	×	×	○
	ISP = 1	○	×	○	×	○
Software interrupt		○	×	○	×	○

Remarks 1. ○: Multiple interrupt servicing enabled

2. ×: Multiple interrupt servicing disabled

3. ISP and IE are flags contained in the PSW.

ISP = 0: An interrupt with higher priority is being serviced.

ISP = 1: No interrupt request has been acknowledged, or an interrupt with a lower priority is being serviced.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

4. PR is a flag contained in PR0L, PR0H, PR1L, and PR1H.

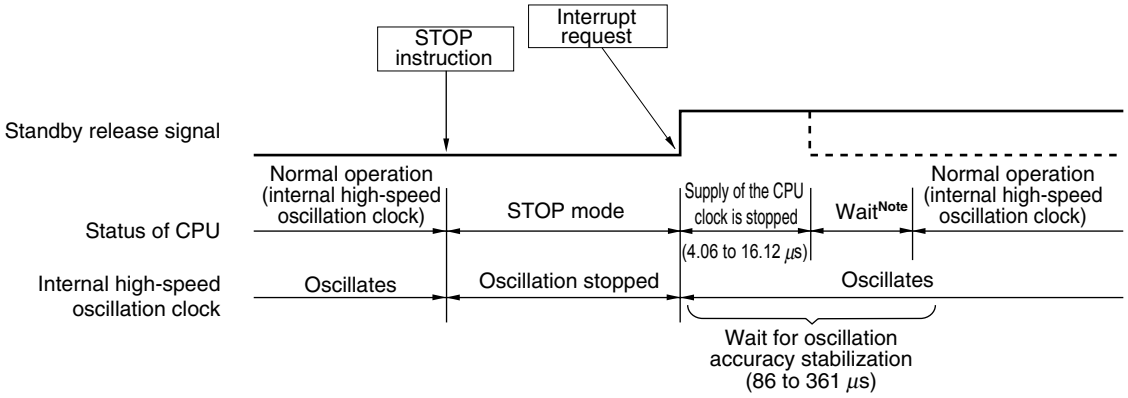
PR = 0: Higher priority level

PR = 1: Lower priority level

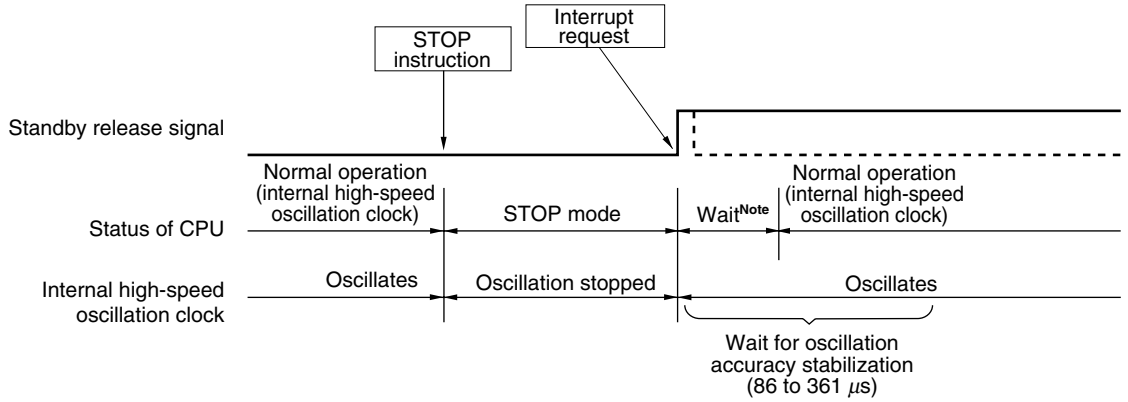
Figure 22-6. STOP Mode Release by Interrupt Request Generation (2/2)

(3) When internal high-speed oscillation clock is used as CPU clock

- When AMPH = 1



- When AMPH = 0



Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks

Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Table 27-1. Internal Memory Size Switching Register Settings

78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2	IMS Setting
μPD78F0500, 78F0500A	–	–	–	–	42H
μPD78F0501, 78F0501A	μPD78F0511, 78F0511A	μPD78F0521, 78F0521A	μPD78F0531, 78F0531A	–	04H
μPD78F0502, 78F0502A	μPD78F0512, 78F0512A	μPD78F0522, 78F0522A	μPD78F0532, 78F0532A	–	C6H
μPD78F0503, 78F0503A, 78F0503D Note 1, 78F0503DA Note 1	μPD78F0513, 78F0513A, 78F0513D Note 1, 78F0513DA Note 1	μPD78F0523, 78F0523A	μPD78F0533, 78F0533A	–	C8H
–	μPD78F0514, 78F0514A	μPD78F0524, 78F0524A	μPD78F0534, 78F0534A	μPD78F0544, 78F0544A	CCH
–	μPD78F0515, 78F0515A, 78F0515D Note 1, 78F0515DA Note 1	μPD78F0525, 78F0525A	μPD78F0535, 78F0535A	μPD78F0545, 78F0545A	CFH
–	–	μPD78F0526, 78F0526A	μPD78F0536, 78F0536A	μPD78F0546, 78F0546A	CCH Note 2
–	–	μPD78F0527, 78F0527A, 78F0527D Note 1, 78F0527DA Note 1	μPD78F0537, 78F0537A, 78F0537D Note 1, 78F0537DA Note 1	μPD78F0547, 78F0547A, 78F0547D Note 1, 78F0547DA Note 1	CCH Note 2

Notes 1. The internal ROM capacity and internal high-speed RAM capacity of the products with the on-chip debug function can be debugged according to the debug target products. Set IMS according to the debug target products.

2. The μPD78F05x6 and 78F05x6A (x = 2 to 4) have internal ROMs of 96 KB, and the μPD78F05x7, 78F05x7A, 78F05x7D, and 78F05x7DA (x = 2 to 4) have those of 128 KB. However, the set value of IMS of these devices is the same as those of the 48 KB product because memory banks are used. For how to set the memory banks, see **4.3 Memory Bank Select Register (BANK)**.

27.2 Internal Expansion RAM Size Switching Register

Select the internal expansion RAM capacity using the internal expansion RAM size switching register (IXS).
IXS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IXS to 0CH.

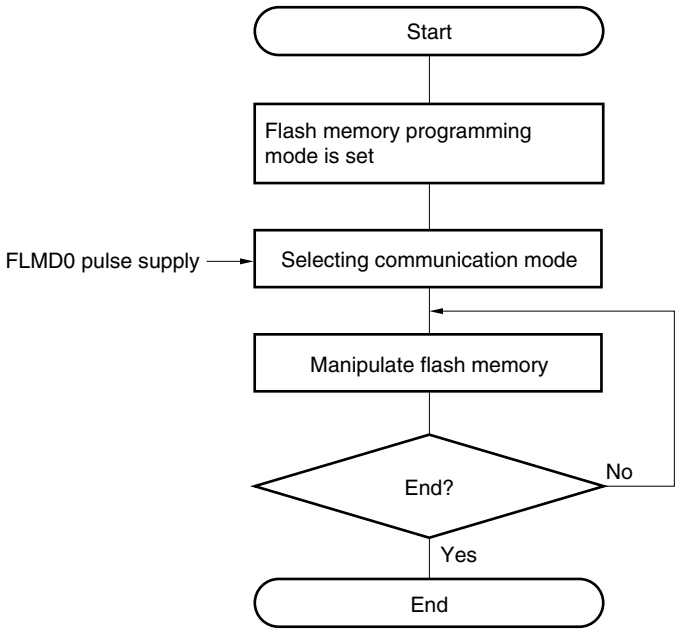
Caution Be sure to set each product to the values shown in Table 27-2 after a reset release.

27.7 Programming Method

27.7.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 27-10. Flash Memory Manipulation Procedure



27.7.2 Flash memory programming mode

To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the 78K0/Kx2 microcontrollers in the flash memory programming mode. To set the mode, set the FLMD0 pin to V_{DD} and clear the reset signal.

Change the mode by using a jumper when writing the flash memory on-board.

Figure 27-11. Flash Memory Programming Mode

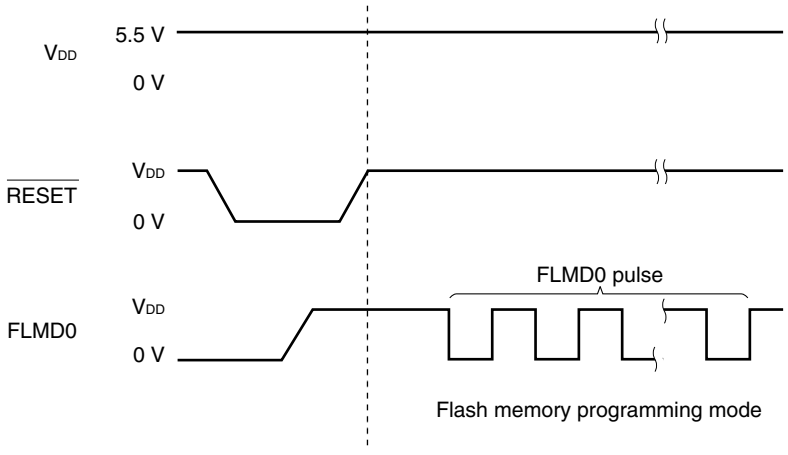


Table 27-6. Relationship Between FLMD0 Pin and Operation Mode After Reset Release

FLMD0	Operation Mode
0	Normal operation mode
V_{DD}	Flash memory programming mode

Table 27-14. Processing Time for Self Programming Library
(Expanded-specification Products (μPD78F05xxA and 78F05xxDA)) (1/3)

(1) When internal high-speed oscillation clock is used and entry RAM is located outside short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		4.0	4.5	4.0	4.5
Initialize library		1105.9	1106.6	1105.9	1106.6
Mode check library		905.7	906.1	904.9	905.3
Block blank check library		12776.1	12778.3	12770.9	12772.6
Block erase library		26050.4	349971.3	26045.3	349965.6
Word write library		1180.1 + 203 × w	1184.3 + 2241 × w	1172.9 + 203 × w	1176.3 + 2241 × w
Block verify library		25337.9	25340.2	25332.8	25334.5
Self programming end library		4.0	4.5	4.0	4.5
Get information library	Option value: 03H	1072.9	1075.2	1067.5	1069.1
	Option value: 04H	1060.2	1062.6	1054.8	1056.6
	Option value: 05H	1023.8	1028.2	1018.3	1022.1
Set information library		70265.9	759995.0	70264.9	759994.0
EEPROM write library		1316.8 + 347 × w	1320.9 + 2385 × w	1309.0 + 347 × w	1312.4 + 2385 × w

(2) When internal high-speed oscillation clock is used and entry RAM is located in short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		4.0	4.5	4.0	4.5
Initialize library		449.5	450.2	449.5	450.2
Mode check library		249.3	249.7	248.6	248.9
Block blank check library		12119.7	12121.9	12114.6	12116.3
Block erase library		25344.7	349266.4	25339.6	349260.8
Word write library		445.8 + 203 × w	449.9 + 2241 × w	438.5 + 203 × w	441.9 + 2241 × w
Block verify library		24682.7	24684.9	24677.6	24679.3
Self programming end library		4.0	4.5	4.0	4.5
Get information library	Option value: 03H	417.6	419.8	412.1	413.8
	Option value: 04H	405.0	407.4	399.5	401.3
	Option value: 05H	367.4	371.8	361.9	365.8
Set information library		69569.3	759297.3	69568.3	759296.2
EEPROM write library		795.1 + 347 × w	799.3 + 2385 × w	787.4 + 347 × w	790.8 + 2385 × w

Remarks 1. The above processing times are those when a write start address structure is located in the internal high-speed RAM and during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

3. w: Number of words in write data (1 word = 4 bytes)

Table 27-14. Processing Time for Self Programming Library (Expanded-specification Products (μPD78F05xxA and 78F05xxDA)) (3/3)

(4) When high-speed system clock (X1 oscillation or external clock input) is used and entry RAM is located in short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		34/f_{CPU}			
Initialize library		55/f_{CPU} + 272			
Mode check library		36/f_{CPU} + 173		30/f_{CPU} + 173	
Block blank check library		179/f_{CPU} + 6108		136/f_{CPU} + 6108	
Block erase library		179/f_{CPU} + 19371	179/f_{CPU} + 267738	136/f_{CPU} + 19371	136/f_{CPU} + 267738
Word write library		333/f_{CPU} + 247 + 136 × w	333/f_{CPU} + 247 + 1647 × w	272/f_{CPU} + 247 + 136 × w	272/f_{CPU} + 247 + 1647 × w
Block verify library		179/f_{CPU}+12964		136/f_{CPU}+12964	
Self programming end library		34/f_{CPU}			
Get information library	Option value: 03H	180/f_{CPU} + 261		134/f_{CPU} + 261	
	Option value: 04H	190/f_{CPU} + 254		144/f_{CPU} + 254	
	Option value: 05H	350/f_{CPU} + 213		304/f_{CPU} + 213	
Set information library		80/f_{CPU} + 42839	80/f_{CPU} + 572592	72/f_{CPU} + 42839	72/f_{CPU} + 572592
EEPROM write library		333/f_{CPU} + 516 + 209 × w	333/f_{CPU} + 516 + 1722 × w	268/f_{CPU} + 516 + 209 × w	268/f_{CPU} + 516 + 1722 × w

Remarks 1. The above processing times are those when a write start address structure is located in the internal high-speed RAM and during stabilized operation of the internal high-speed oscillator (RSTS = 1).

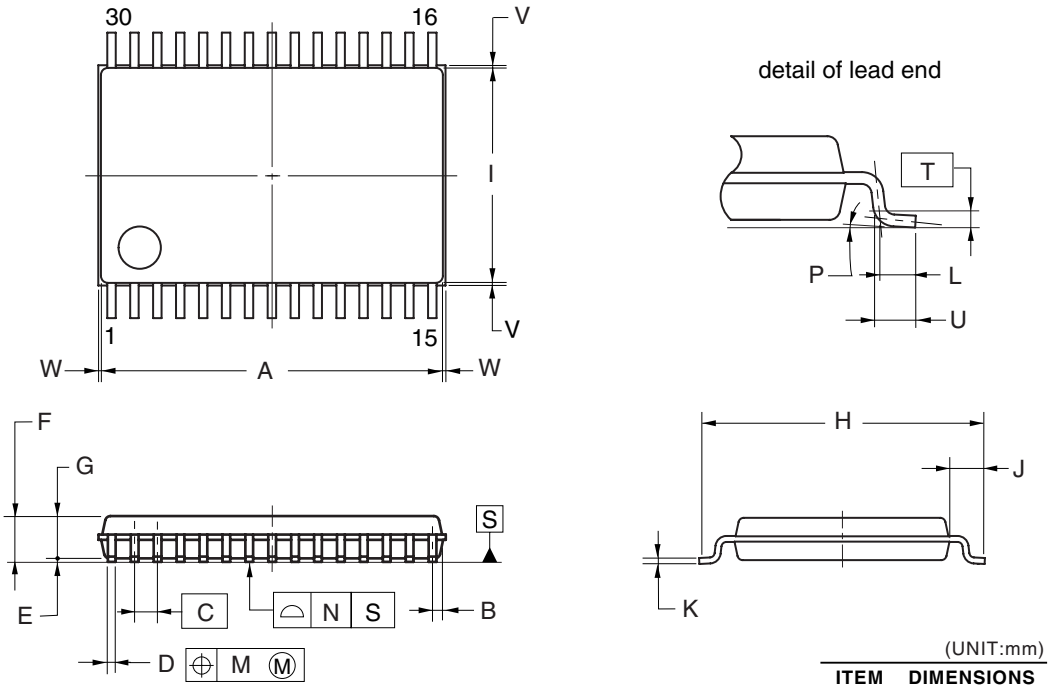
2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

3. f_{CPU}: CPU operation clock frequency

4. w: Number of words in write data (1 word = 4 bytes)

- μPD78F0500MC(A)-CAB-AX, 78F0501MC(A)-CAB-AX, 78F0502MC(A)-CAB-AX, 78F0503MC(A)-CAB-AX
- μPD78F0500MC(A2)-CAB-AX, 78F0501MC(A2)-CAB-AX, 78F0502MC(A2)-CAB-AX, 78F0503MC(A2)-CAB-AX
- μPD78F0500AMC-CAB-AX, 78F0501AMC-CAB-AX, 78F0502AMC-CAB-AX, 78F0503AMC-CAB-AX, 78F0503DAMC-CAB-AX
- μPD78F0500AMCA-CAB-G, 78F0501AMCA-CAB-G, 78F0502AMCA-CAB-G, 78F0503AMCA-CAB-G
- μPD78F0500AMCA2-CAB-G, 78F0501AMCA2-CAB-G, 78F0502AMCA2-CAB-G, 78F0503AMCA2-CAB-G

30-PIN PLASTIC SSOP (7.62mm (300))



(UNIT:mm)

ITEM	DIMENSIONS
A	9.70±0.10
B	0.30
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P30MC-65-CAB

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.