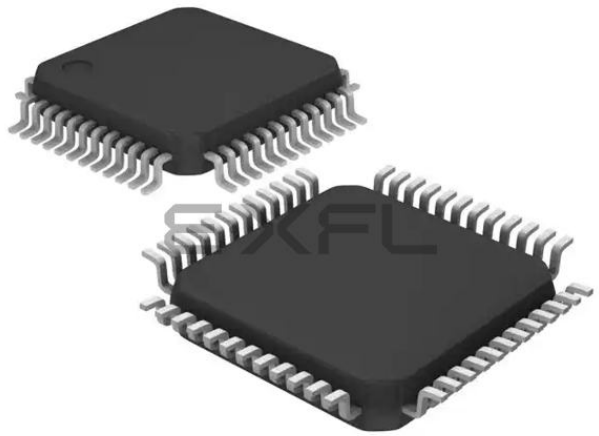
Renesas Electronics America Inc - UPD78F0514AGA-GAM-AX Datasheet



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Applications of "Embedded - Microcontrollers"

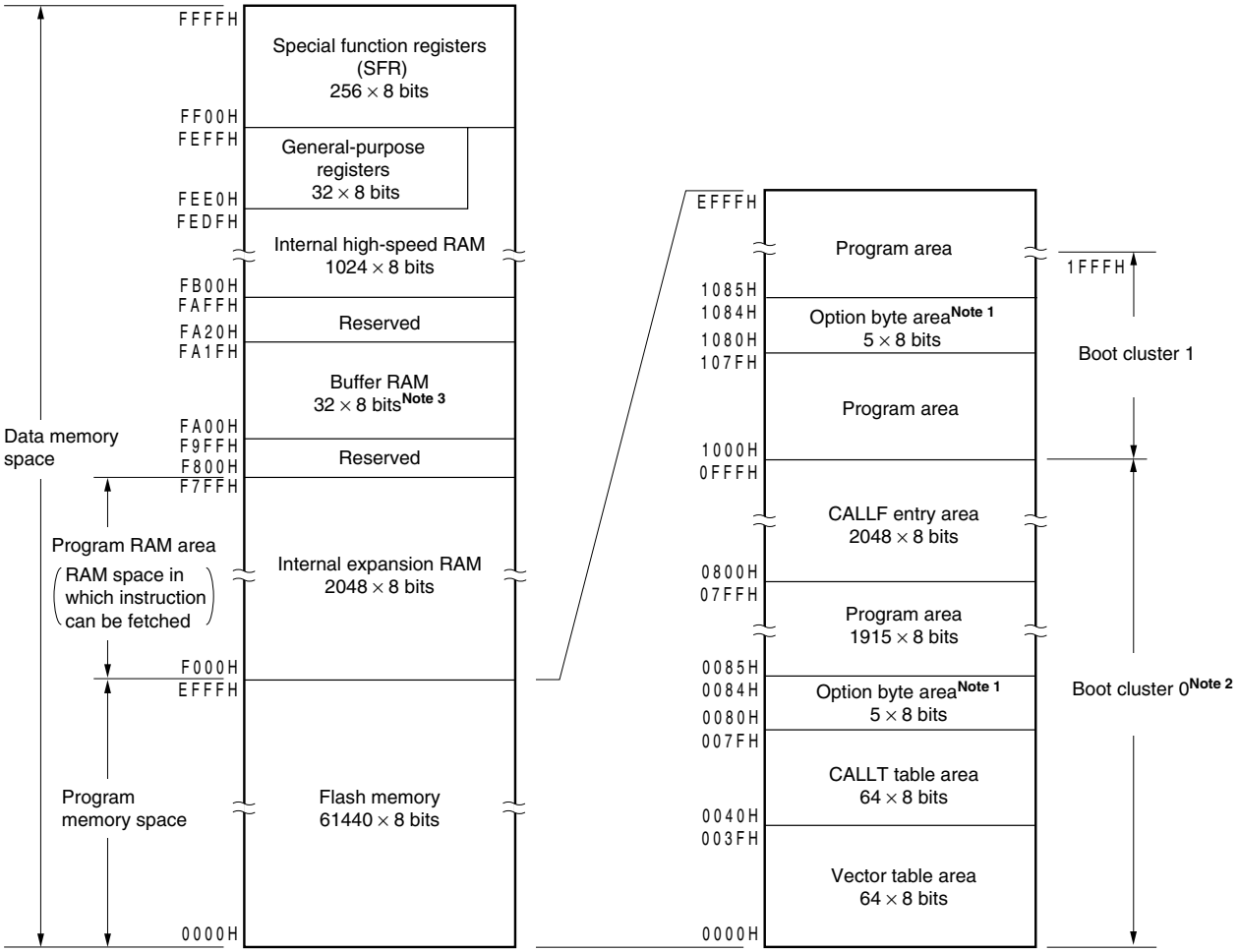
Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0514aga-gam-ax

(2) Non-port functions (3/3): 78K0/KF2

Function Name	I/O	Function	After Reset	Alternate Function
X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A[Note]
X2	–		Input port	P122/EXCLK/OCD0B[Note]
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B[Note]
XT1	–	Connecting resonator for subsystem clock	Input port	P123
XT2	–		Input port	P124/EXCLKS
EXCLKS	Input	External clock input for subsystem clock	Input port	P124/XT2
V_{DD}	–	Positive power supply for P121 to P124 and other than ports	–	–
EV_{DD}	–	Positive power supply for ports other than P20 to P27 and P121 to P124. Make EV_{DD} the same potential as V_{DD}.	–	–
AV_{REF}	–	A/D converter reference voltage input and positive power supply for P20 to P27 and A/D converter	–	–
V_{SS}	–	Ground potential for P121 to P124 and other than ports	–	–
EV_{SS}	–	Ground potential for ports other than P20 to P27 and P121 to P124. Make EV_{SS} the same potential as V_{SS}.	–	–
AV_{SS}	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–
OCD0A[Note]	Input	Connection for on-chip debug mode setting pins (μPD78F0547D and 78F0547DA only)	Input port	P121/X1
OCD1A[Note]				P31/INTP2
OCD0B[Note]	–			P122/X2/EXCLK
OCD1B[Note]				P32/INTP3

Note μPD78F0547D and 78F0547DA (product with on-chip debug function) only

Figure 3-7. Memory Map (μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, 78F0535A, 78F0545, and 78F0545A)

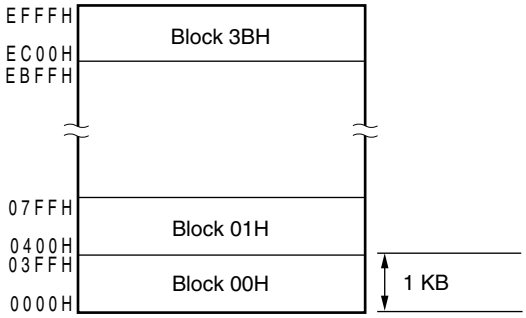


Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H.
When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

3. The buffer RAM is incorporated only in the μPD78F0545 and 78F0545A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, and 78F0535A.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.



3.3 Instruction Address Addressing

An instruction address is determined by contents of the program counter (PC) and memory bank select register (BANK), and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to PC and branched by the following addressing (for details of instructions, refer to the **78K/0 Series Instructions User's Manual (U12326E)**).

3.3.1 Relative addressing

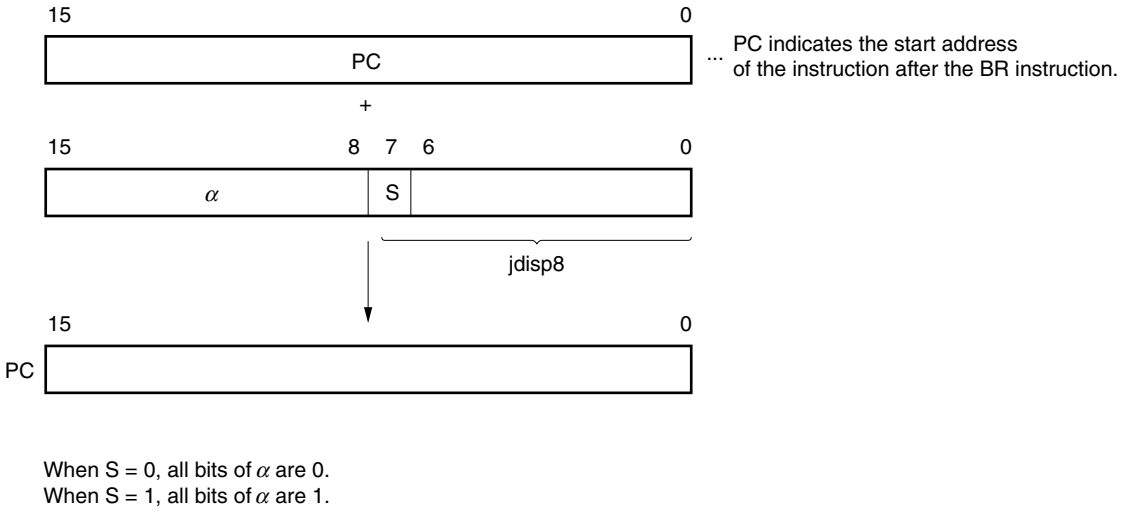
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit.

In other words, relative addressing consists of relative branching from the start address of the following instruction to the −128 to +127 range.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

4.4 Selecting Memory Bank

The memory bank selected by the memory bank select register (BANK) is reflected on the bank area and can be addressed. Therefore, to access a memory bank different from the one currently selected, that memory bank must be selected by using the BANK register.

The value of the BANK register must not be changed in the bank area (8000H to BFFFH). Therefore, to change the memory bank, branch an instruction to the common area (0000H to 7FFFH) and change the value of the BANK register in that area.

Cautions 1. Instructions cannot be fetched between different memory banks.

2. Branching and accessing cannot be directly executed between different memory banks. Execute branching or accessing between different memory banks via the common area.

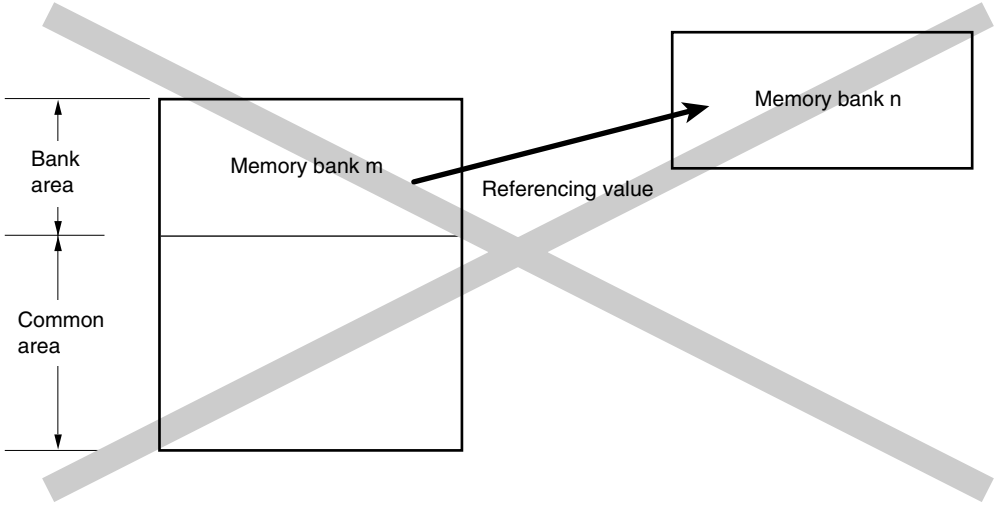
3. Allocate interrupt servicing in the common area.

4. An instruction that extends from 7FFFH to 8000H can only be executed in memory bank 0.

4.4.1 Referencing values between memory banks

Values cannot be directly referenced from one memory bank to another.

To access another memory bank from one memory bank, branch once to the common area (0000H to 7FFFH), change the setting of the BANK register there, and then reference a value.



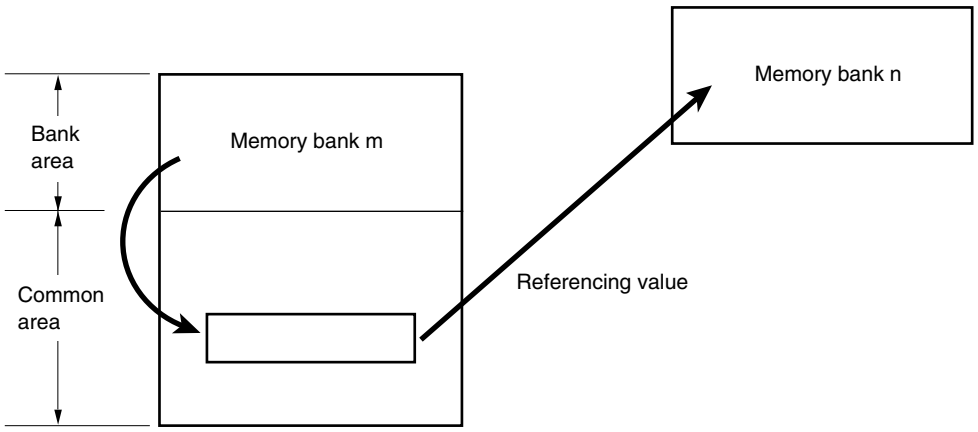
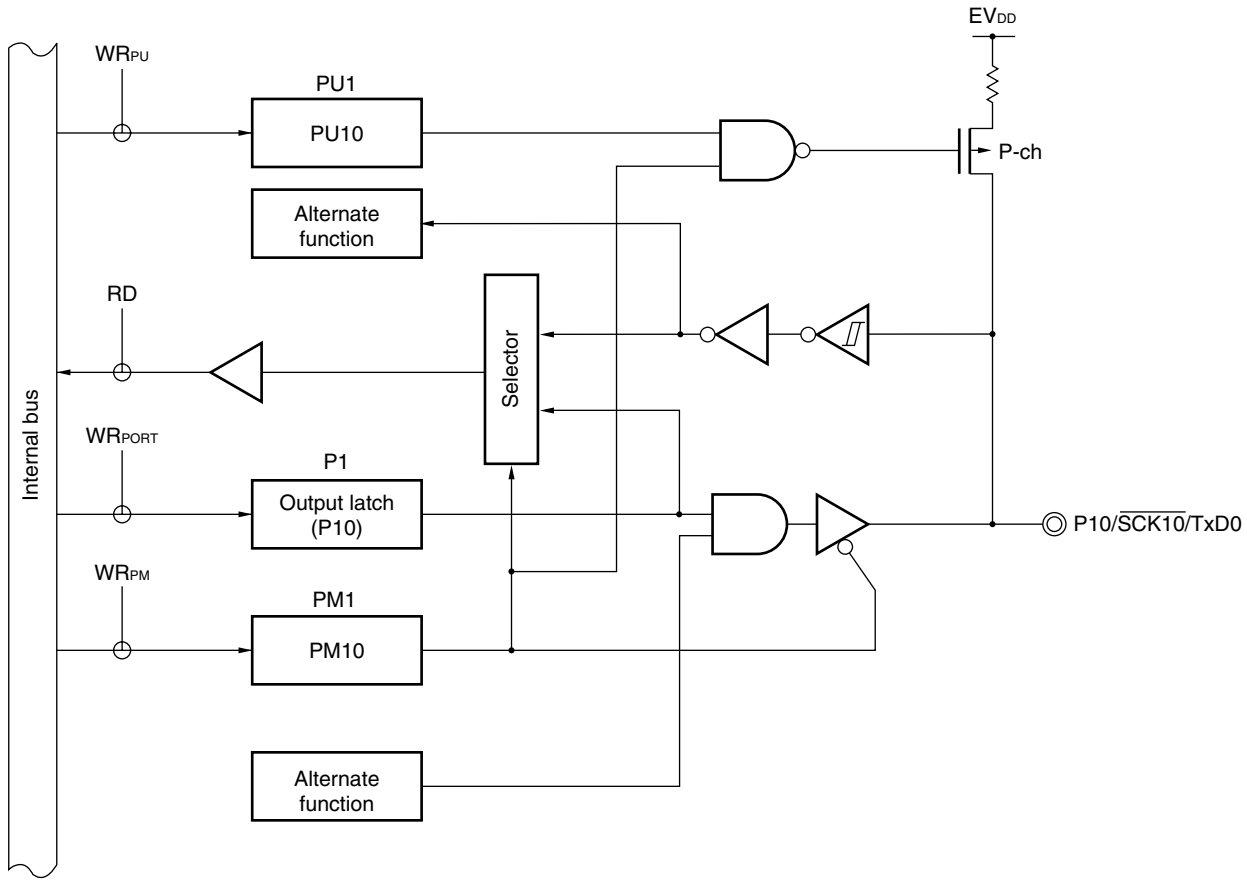


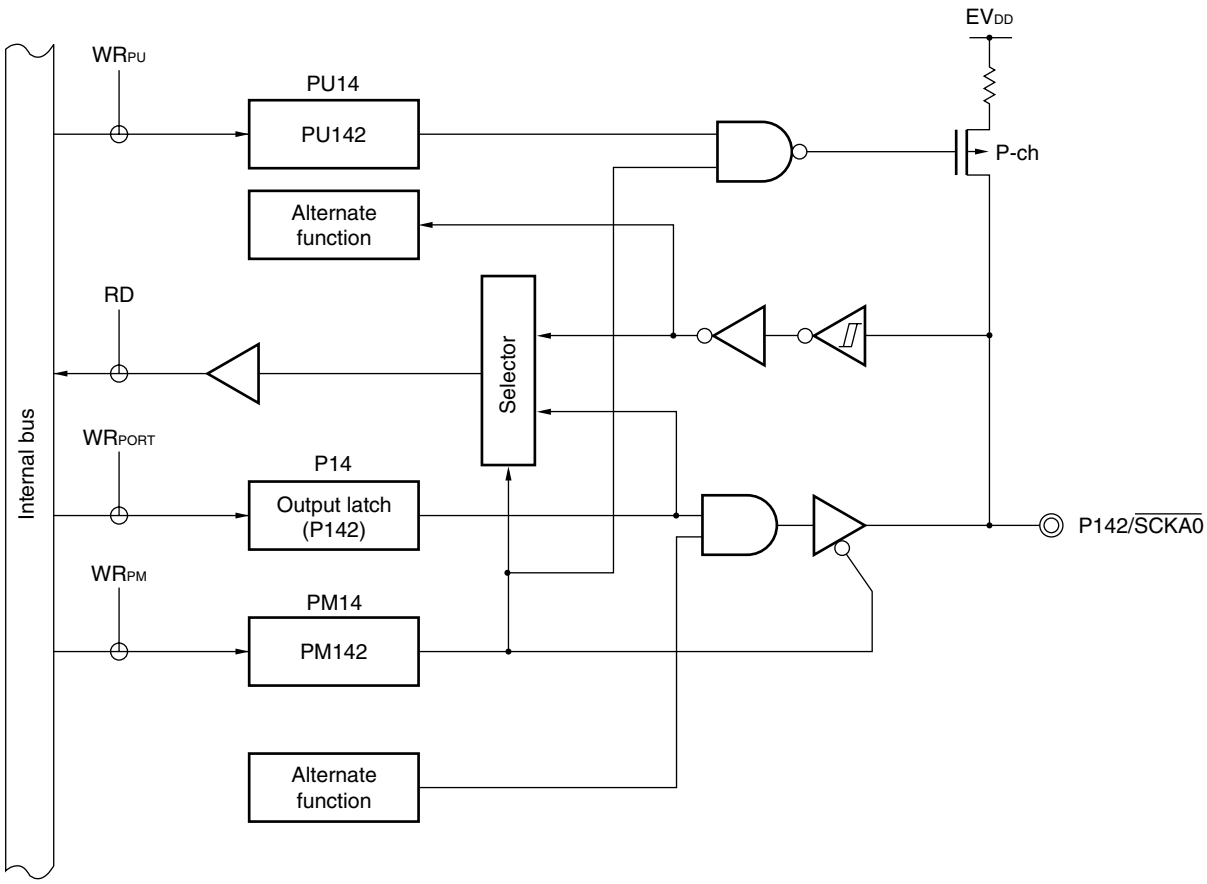
Figure 5-7. Block Diagram of P10



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

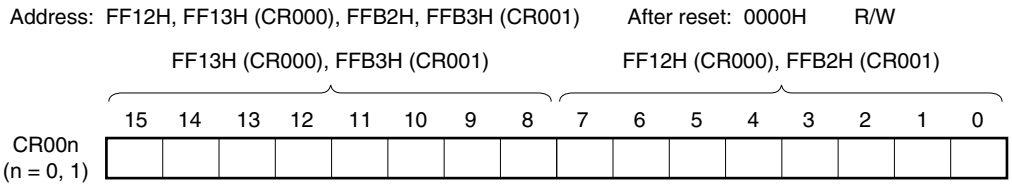
Figure 5-26. Block Diagram of P142



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

Figure 7-4. Format of 16-Bit Timer Capture/Compare Register 00n (CR00n)



(i) When CR00n is used as a compare register

The value set in CR00n is constantly compared with the TM0n count value, and an interrupt request signal (INTTM00n) is generated if they match. The value is held until CR00n is rewritten.

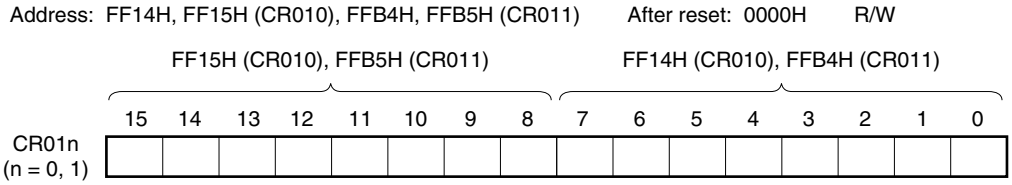
Caution CR00n does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR00n is used as a capture register

The count value of TM0n is captured to CR00n when a capture trigger is input.

As the capture trigger, an edge of a phase reverse to that of the TI00n pin or the valid edge of the TI01n pin can be selected by using CRC0n or PRM0n.

Figure 7-5. Format of 16-Bit Timer Capture/Compare Register 01n (CR01n)



(i) When CR01n is used as a compare register

The value set in CR01n is constantly compared with the TM0n count value, and an interrupt request signal (INTTM01n) is generated if they match.

Caution CR01n does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR01n is used as a capture register

The count value of TM0n is captured to CR01n when a capture trigger is input.

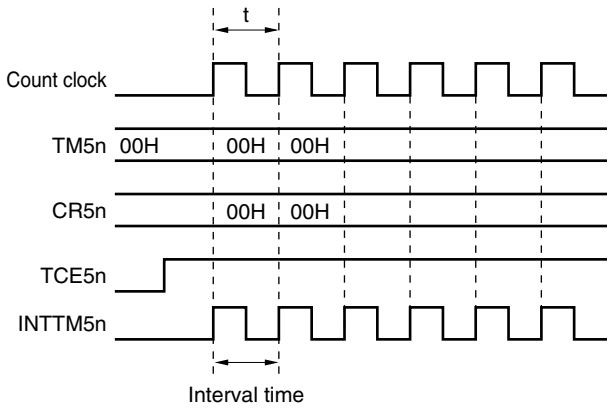
It is possible to select the valid edge of the TI00n pin as the capture trigger. The TI00n pin valid edge is set by PRM0n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

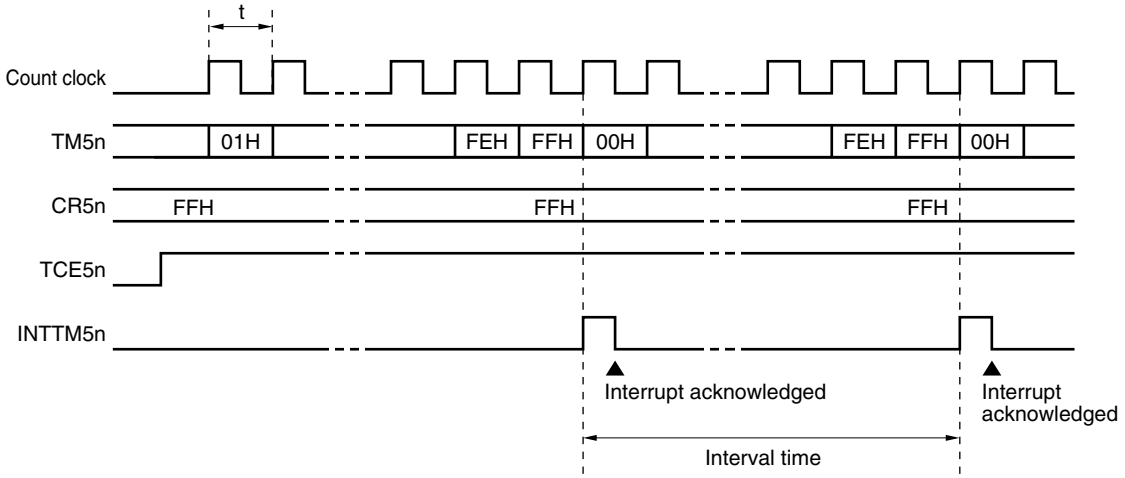
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 8-11. Interval Timer Operation Timing (2/2)

(b) When CR5n = 00H



(c) When CR5n = FFH



Remark n = 0, 1

9.3 Registers Controlling 8-Bit Timers H0 and H1

The following four registers are used to control 8-bit timers H0 and H1.

- 8-bit timer H mode register n (TMHMDn)
- 8-bit timer H carrier control register 1 (TMCYC1)[Note]
- Port mode register 1 (PM1)
- Port register 1 (P1)

Note 8-bit timer H1 only

(1) 8-bit timer H mode register n (TMHMDn)

This register controls the mode of timer H.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark n = 0, 1

Figure 15-8. Format of Clock Selection Register 6 (CKSR6)

Address: FF56H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CKSR6	0	0	0	0	TPS63	TPS62	TPS61	TPS60

TPS63	TPS62	TPS61	TPS60	Base clock (f_{XCLK6}) selection[Note 1]				
					f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz	20 MHz[Note 3]
0	0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz	625 kHz
0	1	1	0	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
0	1	1	1	$f_{PRS}/2^7$	15.625 kHz	39.06 kHz	78.13 kHz	156.25 kHz
1	0	0	0	$f_{PRS}/2^8$	7.813 kHz	19.53 kHz	39.06 kHz	78.13 kHz
1	0	0	1	$f_{PRS}/2^9$	3.906 kHz	9.77 kHz	19.53 kHz	39.06 kHz
1	0	1	0	$f_{PRS}/2^{10}$	1.953 kHz	4.88 kHz	9.77 kHz	19.53 kHz
1	0	1	1	TM50 output[Note 4]				
Other than above				Setting prohibited				

Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when $f_{PRS} = f_{XH}$ (XSEL = 1).)

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V ≤ V_{DD} < 2.7 V, the setting of TPS63 = TPS62 = TPS61 = TPS60 = 0 (base clock: f_{PRS}) is prohibited.

3. This is settable only if 4.0 V ≤ V_{DD} ≤ 5.5 V.

4. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

(c) Normal transmission

When bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and bit 6 (TXE6) of ASIM6 is then set to 1, transmission is enabled. Transmission can be started by writing transmit data to transmit buffer register 6 (TXB6). The start bit, parity bit, and stop bit are automatically appended to the data.

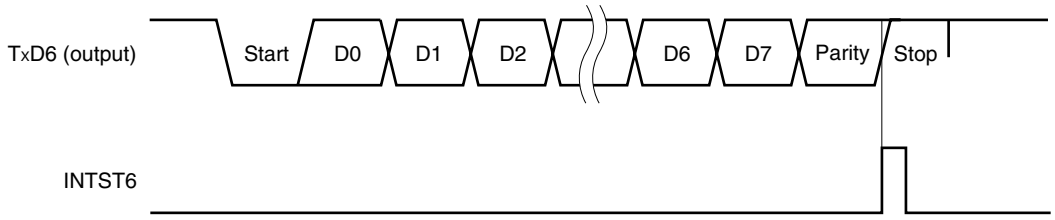
When transmission is started, the data in TXB6 is transferred to transmit shift register 6 (TXS6). After that, the transmit data is sequentially output from TXS6 to the TxD6 pin. When transmission is completed, the parity and stop bits set by ASIM6 are appended and a transmission completion interrupt request (INTST6) is generated.

Transmission is stopped until the data to be transmitted next is written to TXB6.

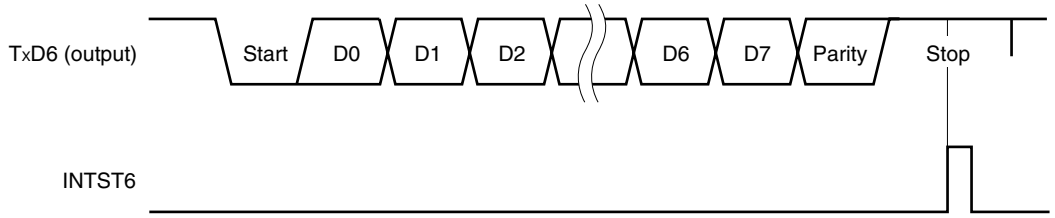
Figure 15-15 shows the timing of the transmission completion interrupt request (INTST6). This interrupt occurs as soon as the last stop bit has been output.

Figure 15-15. Normal Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2



18.4 I^2C Bus Mode Functions

18.4.1 Pin configuration

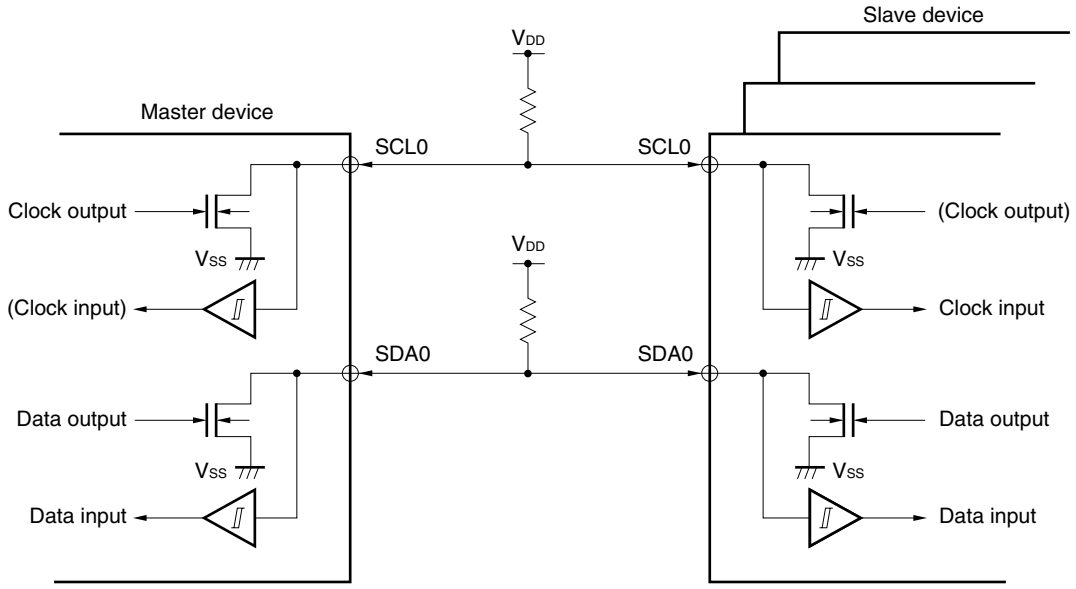
The serial clock pin (SCL0) and serial data bus pin (SDA0) are configured as follows.

(1) SCL0..... This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

(2) SDA0 ..... This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

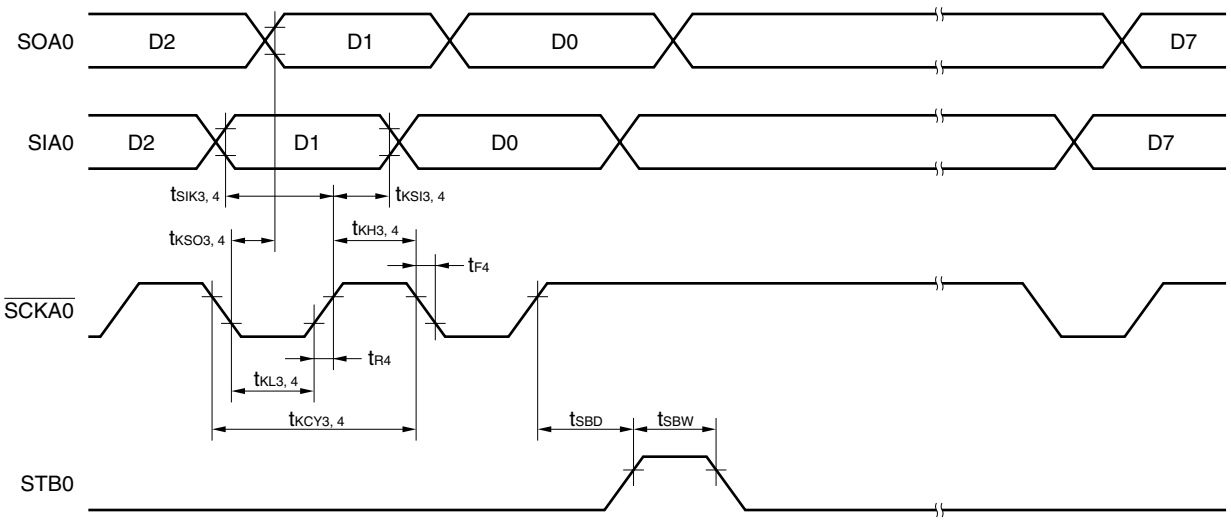
Figure 18-11. Pin Configuration Diagram



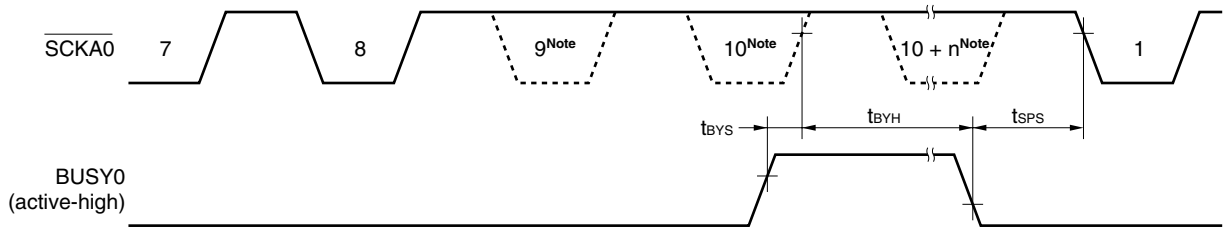
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Serial Transfer Timing (2/2)

CSIA0:



CSIA0 (busy processing):



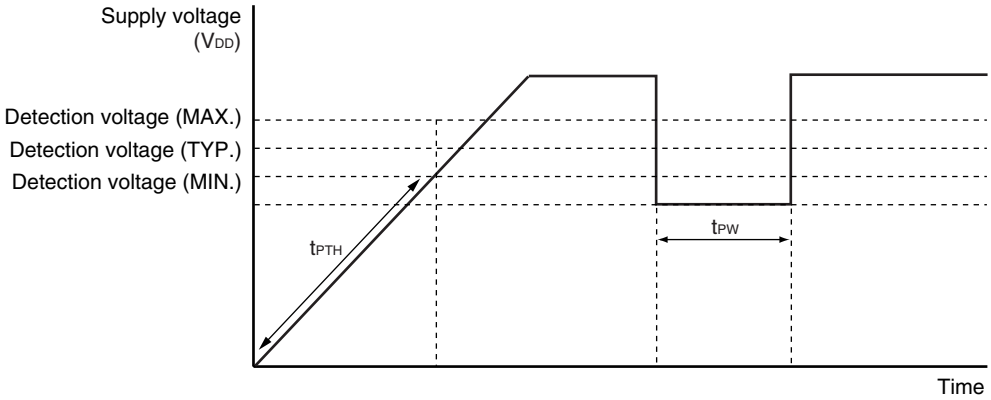
Note SCKA0 does not become low level here, but the timing is illustrated so that the timing specifications can be shown.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

1.59 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		1.44	1.59	1.74	V
Power supply voltage rise inclination	t_{PTH}	V_{DD}: 0 V → change inclination of V_{POC}	0.5			V/ms
Minimum pulse width	t_{PW}		200			μs

1.59 V POC Circuit Timing



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

LVI Circuit Characteristics (T_A = –40 to +110°C, $V_{POC} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $AV_{REF} \leq V_{DD}$, $V_{SS} = EV_{SS}$ = 0 V)

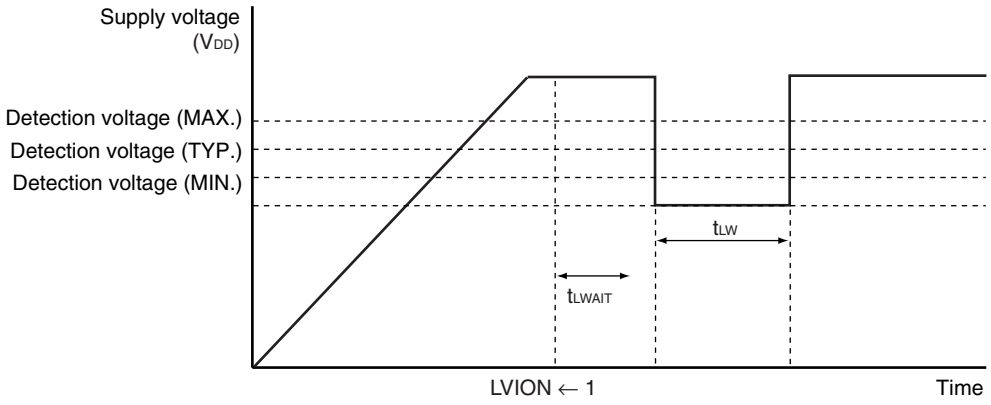
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.14	4.24	4.34	V
		V_{LVI1}		3.99	4.09	4.19	V
		V_{LVI2}		3.83	3.93	4.03	V
		V_{LVI3}		3.68	3.78	3.88	V
		V_{LVI4}		3.52	3.62	3.72	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.06	3.16	3.26	V
		V_{LVI8}		2.91	3.01	3.11	V
		V_{LVI9}		2.75	2.85	2.95	V
	External input pin[Note 1]	EXLVI	EXLVI < V_{DD}, 2.7 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note 2]		t_{LWAIT}		10			μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 9

LVI Circuit Timing



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Internal Oscillator Characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

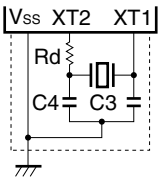
Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
8 MHz internal oscillator	Internal high-speed oscillation clock frequency (f_{RH})[Note]	RSTS = 1	7.6	8.0	8.46	MHz
		RSTS = 0	2.48	5.6	9.86	MHz
240 kHz internal oscillator	Internal low-speed oscillation clock frequency (f_{RL})		216	240	264	kHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Remark RSTS: Bit 7 of the internal oscillation mode register (RCM)

XT1 Oscillator Characteristics[Note 1]

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})[Note 2]		32	32.768	35	kHz

Notes 1. The 78K0/KB2 is not provided with the XT1 oscillator.

2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

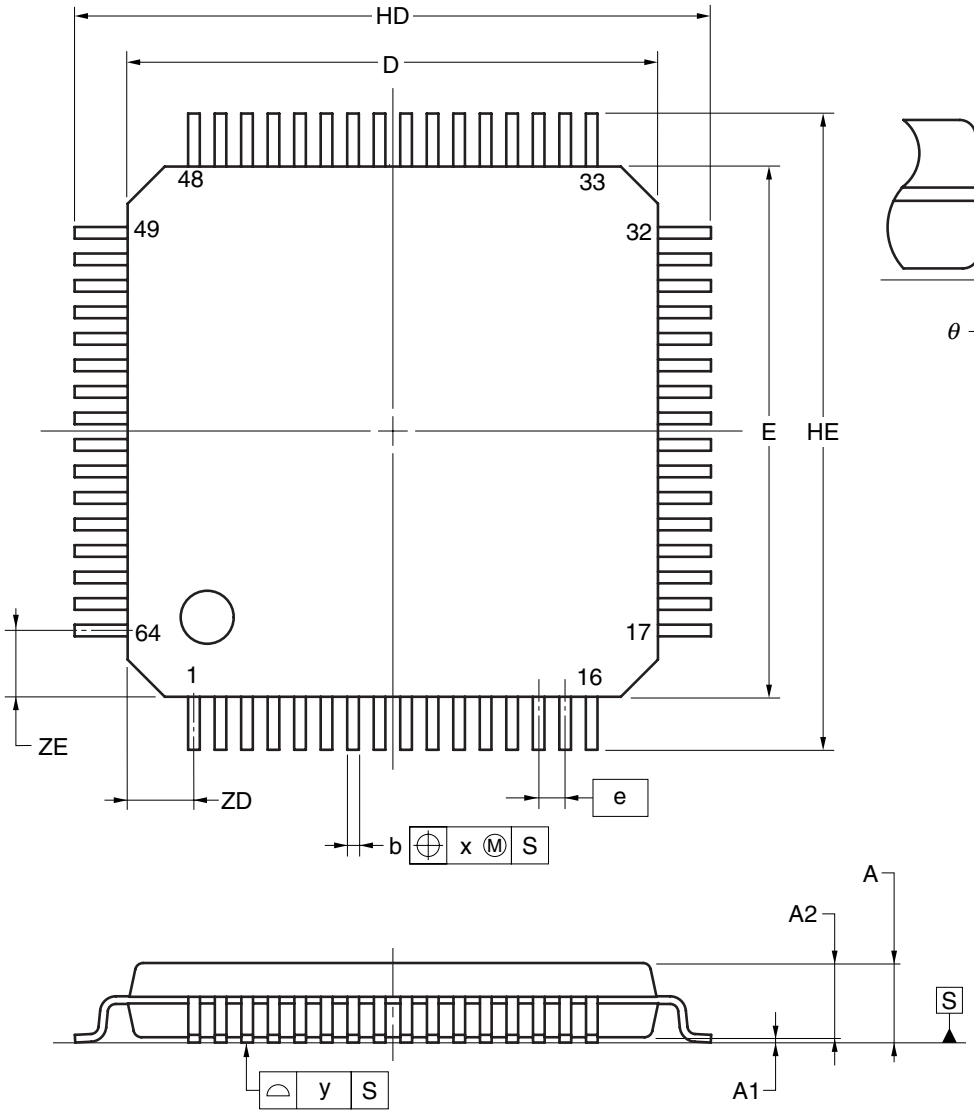
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

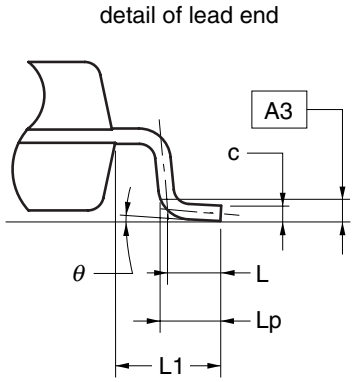
2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

- μPD78F0531GB(A)-GAH-AX, 78F0532GB(A)-GAH-AX, 78F0533GB(A)-GAH-AX, 78F0534GB(A)-GAH-AX, 78F0535GB(A)-GAH-AX, 78F0536GB(A)-GAH-AX, 78F0537GB(A)-GAH-AX
- μPD78F0531GB(A2)-GAH-AX, 78F0532GB(A2)-GAH-AX, 78F0533GB(A2)-GAH-AX, 78F0534GB(A2)-GAH-AX, 78F0535GB(A2)-GAH-AX, 78F0536GB(A2)-GAH-AX, 78F0537GB(A2)-GAH-AX
- μPD78F0531AGB-GAH-AX, 78F0532AGB-GAH-AX, 78F0533AGB-GAH-AX, 78F0534AGB-GAH-AX, 78F0535AGB-GAH-AX, 78F0536AGB-GAH-AX, 78F0537AGB-GAH-AX, 78F0537DAGB-GAH-AX
- μPD78F0531AGBA-GAH-G, 78F0532AGBA-GAH-G, 78F0533AGBA-GAH-G, 78F0534AGBA-GAH-G, 78F0535AGBA-GAH-G, 78F0536AGBA-GAH-G, 78F0537AGBA-GAH-G
- μPD78F0531AGBA2-GAH-G, 78F0532AGBA2-GAH-G, 78F0533AGBA2-GAH-G, 78F0534AGBA2-GAH-G, 78F0535AGBA2-GAH-G, 78F0536AGBA2-GAH-G, 78F0537AGBA2-GAH-G

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)





(UNIT:mm)

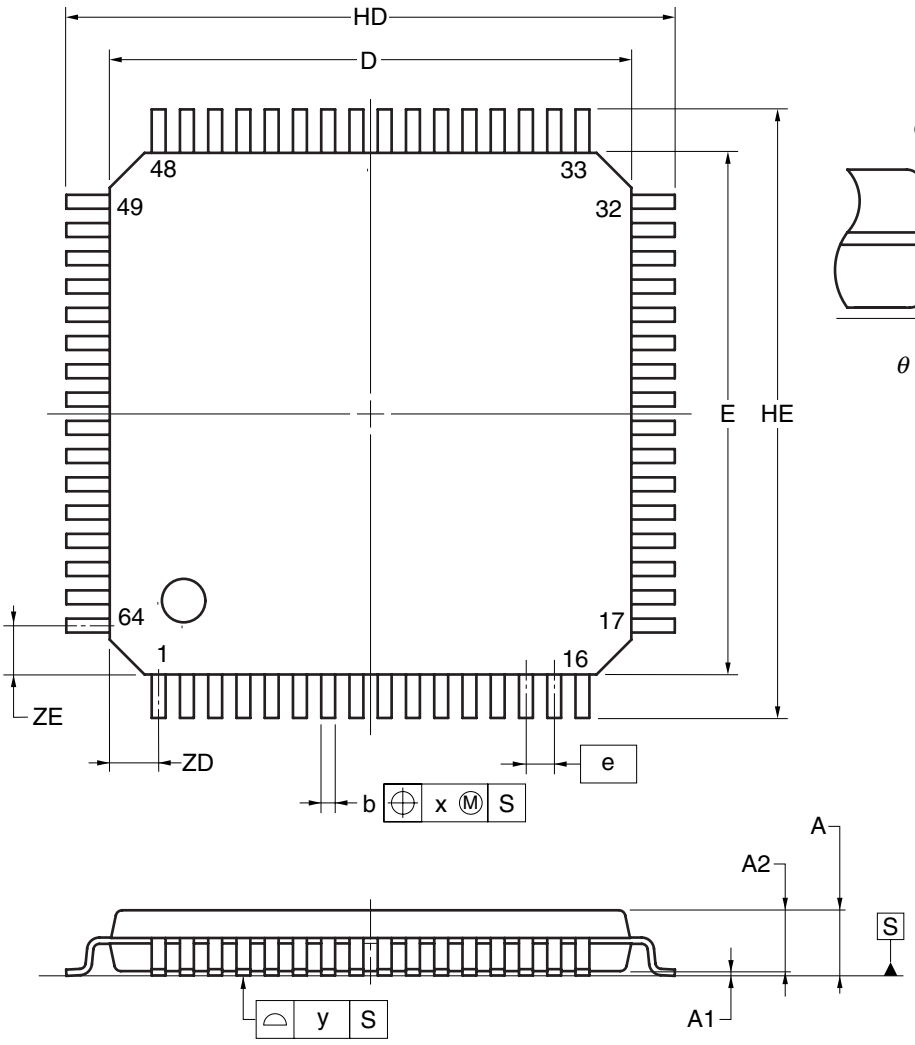
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

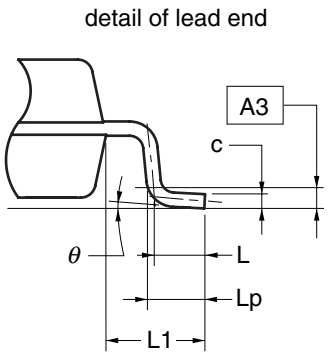
P64GB-50-GAH

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

- μPD78F0531GK(A)-GAJ-AX, 78F0532GK(A)-GAJ-AX, 78F0533GK(A)-GAJ-AX, 78F0534GK(A)-GAJ-AX, 78F0535GK(A)-GAJ-AX, 78F0536GK(A)-GAJ-AX, 78F0537GK(A)-GAJ-AX
- μPD78F0531GK(A2)-GAJ-AX, 78F0532GK(A2)-GAJ-AX, 78F0533GK(A2)-GAJ-AX, 78F0534GK(A2)-GAJ-AX, 78F0535GK(A2)-GAJ-AX, 78F0536GK(A2)-GAJ-AX, 78F0537GK(A2)-GAJ-AX
- μPD78F0531AGK-GAJ-AX, 78F0532AGK-GAJ-AX, 78F0533AGK-GAJ-AX, 78F0534AGK-GAJ-AX, 78F0535AGK-GAJ-AX, 78F0536AGK-GAJ-AX, 78F0537AGK-GAJ-AX, 78F0537DAGK-GAJ-AX
- μPD78F0531AGKA-GAJ-G, 78F0532AGKA-GAJ-G, 78F0533AGKA-GAJ-G, 78F0534AGKA-GAJ-G, 78F0535AGKA-GAJ-G, 78F0536AGKA-GAJ-G, 78F0537AGKA-GAJ-G
- μPD78F0531AGKA2-GAJ-G, 78F0532AGKA2-GAJ-G, 78F0533AGKA2-GAJ-G, 78F0534AGKA2-GAJ-G, 78F0535AGKA2-GAJ-G, 78F0536AGKA2-GAJ-G, 78F0537AGKA2-GAJ-G

64-PIN PLASTIC LQFP (12x12)





(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.75}_{-0.25}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

P64GK-65-GAJ

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

C.2 Register Index (In Alphabetical Order with Respect to Register Symbol)