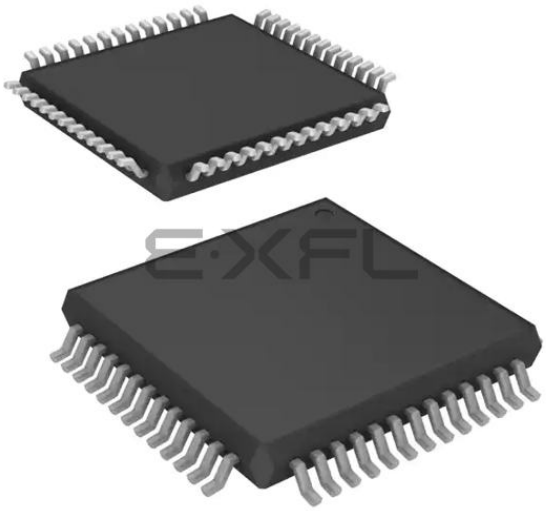
Renesas Electronics America Inc - UPD78F0522AGB-GAG-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0522agb-gag-ax

[List of Part Number]

(1/6)

78K0/Kx2 Microcontrollers	Package	Product type	Quality grace	Part Number
78K0/KB2	30-pin plastic SSOP (7.62 mm (300))	Conventional-specification products	Standard products	μPD78F0500MC-5A4-A, 78F0501MC-5A4-A, 78F0502MC-5A4-A, 78F0503MC-5A4-A, 78F0503DMC-5A4-A[Note]
			(A) grade products	μPD78F0500MC(A)-CAB-AX, 78F0501MC(A)-CAB-AX, 78F0502MC(A)-CAB-AX, 78F0503MC(A)-CAB-AX
			(A2) grade products	μPD78F0500MC(A2)-CAB-AX, 78F0501MC(A2)-CAB-AX, 78F0502MC(A2)-CAB-AX, 78F0503MC(A2)-CAB-AX
		Expanded-specification products	Standard products	μPD78F0500AMC-CAB-AX, 78F0501AMC-CAB-AX, 78F0502AMC-CAB-AX, 78F0503AMC-CAB-AX, 78F0503DAMC-CAB-AX[Note]
			(A) grade products	μPD78F0500AMCA-CAB-G, 78F0501AMCA-CAB-G, 78F0502AMCA-CAB-G, 78F0503AMCA-CAB-G
			(A2) grade products	μPD78F0500AMCA2-CAB-G, 78F0501AMCA2-CAB-G, 78F0502AMCA2-CAB-G, 78F0503AMCA2-CAB-G
	36-pin plastic FLGA (4x4)	Conventional-specification products	Standard products	μPD78F0500FC-AA3-A, 78F0501FC-AA3-A, 78F0502FC-AA3-A, 78F0503FC-AA3-A, 78F0503DFC-AA3-A[Note]
		Expanded-specification products	Standard products	μPD78F0500AFC-AA3-A, 78F0501AFC-AA3-A, 78F0502AFC-AA3-A, 78F0503AFC-AA3-A, 78F0503DAFC-AA3-A[Note]
78K0/KC2	38-pin plastic SSOP (7.62 mm (300))	Expanded-specification products	Standard products	μPD78F0511AMC-GAA-AX, 78F0512AMC-GAA-AX, 78F0513AMC-GAA-AX, 78F0513DAMC-GAA-AX[Note]
			(A) grade products	μPD78F0511AMCA-GAA-G, 78F0512AMCA-GAA-G, 78F0513AMCA-GAA-G
			(A2) grade products	μPD78F0511AMCA2-GAA-G, 78F0512AMCA2-GAA-G, 78F0513AMCA2-GAA-G
	44-pin plastic LQFP (10x10)	Conventional-specification products	Standard products	μPD78F0511GB-UES-A, 78F0512GB-UES-A, 78F0513GB-UES-A, 78F0513DGB-UES-A[Note]
			(A) grade products	μPD78F0511GB(A)-GAF-AX, 78F0512GB(A)-GAF-AX, 78F0513GB(A)-GAF-AX
			(A2) grade products	μPD78F0511GB(A2)-GAF-AX, 78F0512GB(A2)-GAF-AX, 78F0513GB(A2)-GAF-AX
		Expanded-specification products	Standard products	μPD78F0511AGB-GAF-AX, 78F0512AGB-GAF-AX, 78F0513AGB-GAF-AX, 78F0513DAGB-GAF-AX[Note]
			(A) grade products	μPD78F0511AGBA-GAF-G, 78F0512AGBA-GAF-G, 78F0513AGBA-GAF-G
			(A2) grade products	μPD78F0511AGBA2-GAF-G, 78F0512AGBA2-GAF-G, 78F0513AGBA2-GAF-G

Note The μPD78F0503D, 78F0503DA, 78F0513D, and 78F0513DA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Table 3-2. Set Values of Internal Memory Size Switching Register (IMS) and Internal Expansion RAM Size Switching Register (IXS) (48-pin products of the 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)

48-pin products of the 78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2	IMS	IXS	ROM Capacity	Internal High-Speed RAM Capacity	Internal Expansion RAM Capacity
μPD78F0511, 78F0511A	μPD78F0521, 78F0521A	μPD78F0531, 78F0531A	–	04H	0CH	16 KB	768 bytes	–
μPD78F0512, 78F0512A	μPD78F0522, 78F0522A	μPD78F0532, 78F0532A	–	C6H	0CH	24 KB	1 KB	–
μPD78F0513, 78F0513A	μPD78F0523, 78F0523A	μPD78F0533, 78F0533A	–	C8H	0CH	32 KB	1 KB	–
μPD78F0514, 78F0514A	μPD78F0524, 78F0524A	μPD78F0534, 78F0534A	μPD78F0544, 78F0544A	CCH	0AH	48 KB	1 KB	1 KB
μPD78F0515, 78F0515A, 78F0515D[Note 1], 78F0515DA[Note 1]	μPD78F0525, 78F0525A	μPD78F0535, 78F0535A	μPD78F0545, 78F0545A	CFH	08H	60 KB		2 KB
–	μPD78F0526, 78F0526A	μPD78F0536, 78F0536A	μPD78F0546, 78F0546A	CCH[Note 2]	04H	96 KB[Note 2]		4 KB
–	μPD78F0527, 78F0527A, 78F0527D[Note 1], 78F0527DA[Note 1]	μPD78F0537, 78F0537A, 78F0537D[Note 1], 78F0537DA[Note 1]	μPD78F0547, 78F0547A, 78F0547D[Note 1], 78F0547DA[Note 1]	CCH[Note 2]	00H	128 KB[Note 2]		6 KB

Notes 1. The ROM and RAM capacities of the products with the on-chip debug function can be debugged according to the debug target products. Set IMS and IXS according to the debug target products.

2. The μPD78F05x6 and 78F05x6A (x = 2 to 4) have internal ROMs of 96 KB, and the μPD78F05x7, 78F05x7A, 78F05x7D and 78F05x7DA (x = 2 to 4) have those of 128 KB. However, the set value of IMS of these devices is the same as those of the 48 KB product because memory banks are used. For how to set the memory banks, see **4.3 Memory Bank Select Register (BANK)**.

Table 3-8. Special Function Register List (1/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset	KB2	KC2	KD2	KE2	KF2
				1 Bit	8 Bits	16 Bits						
FF00H	Port register 0	P0	R/W	√	√	–	00H	√	√	√	√	√
FF01H	Port register 1	P1	R/W	√	√	–	00H	√	√	√	√	√
FF02H	Port register 2	P2	R/W	√	√	–	00H	√	√	√	√	√
FF03H	Port register 3	P3	R/W	√	√	–	00H	√	√	√	√	√
FF04H	Port register 4	P4	R/W	√	√	–	00H	–	√	√	√	√
FF05H	Port register 5	P5	R/W	√	√	–	00H	–	–	–	√	√
FF06H	Port register 6	P6	R/W	√	√	–	00H	√	√	√	√	√
FF07H	Port register 7	P7	R/W	√	√	–	00H	–	√	√	√	√
FF08H	10-bit A/D conversion result register	ADCR	R	–	–	√	0000H	√	√	√	√	√
FF09H	8-bit A/D conversion result register	ADCRH	R	–	√	–	00H	√	√	√	√	√
FF0AH	Receive buffer register 6	RXB6	R	–	√	–	FFH	√	√	√	√	√
FF0BH	Transmit buffer register 6	TXB6	R/W	–	√	–	FFH	√	√	√	√	√
FF0CH	Port register 12	P12	R/W	√	√	–	00H	√	√	√	√	√
FF0DH	Port register 13	P13	R/W	√	√	–	00H	–	**Note**	√	√	√
FF0EH	Port register 14	P14	R/W	√	√	–	00H	–	**Note**	√	√	√
FF0FH	Serial I/O shift register 10	SIO10	R	–	√	–	00H	√	√	√	√	√
FF10H FF11H	16-bit timer counter 00	TM00	R	–	–	√	0000H	√	√	√	√	√
FF12H FF13H	16-bit timer capture/compare register 000	CR000	R/W	–	–	√	0000H	√	√	√	√	√
FF14H FF15H	16-bit timer capture/compare register 010	CR010	R/W	–	–	√	0000H	√	√	√	√	√
FF16H	8-bit timer counter 50	TM50	R	–	√	–	00H	√	√	√	√	√
FF17H	8-bit timer compare register 50	CR50	R/W	–	√	–	00H	√	√	√	√	√
FF18H	8-bit timer H compare register 00	CMP00	R/W	–	√	–	00H	√	√	√	√	√
FF19H	8-bit timer H compare register 10	CMP10	R/W	–	√	–	00H	√	√	√	√	√
FF1AH	8-bit timer H compare register 01	CMP01	R/W	–	√	–	00H	√	√	√	√	√
FF1BH	8-bit timer H compare register 11	CMP11	R/W	–	√	–	00H	√	√	√	√	√
FF1FH	8-bit timer counter 51	TM51	R	–	√	–	00H	√	√	√	√	√
FF20H	Port mode register 0	PM0	R/W	√	√	–	FFH	√	√	√	√	√
FF21H	Port mode register 1	PM1	R/W	√	√	–	FFH	√	√	√	√	√
FF22H	Port mode register 2	PM2	R/W	√	√	–	FFH	√	√	√	√	√
FF23H	Port mode register 3	PM3	R/W	√	√	–	FFH	√	√	√	√	√
FF24H	Port mode register 4	PM4	R/W	√	√	–	FFH	–	√	√	√	√
FF25H	Port mode register 5	PM5	R/W	√	√	–	FFH	–	–	–	√	√
FF26H	Port mode register 6	PM6	R/W	√	√	–	FFH	√	√	√	√	√
FF27H	Port mode register 7	PM7	R/W	√	√	–	FFH	–	√	√	√	√
FF28H	A/D converter mode register	ADM	R/W	√	√	–	00H	√	√	√	√	√
FF29H	Analog input channel specification register	ADS	R/W	√	√	–	00H	√	√	√	√	√
FF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH	√	√	√	√	√
FF2EH	Port mode register 14	PM14	R/W	√	√	–	FFH	–	**Note**	√	√	√
FF2FH	A/D port configuration register	ADPC	R/W	√	√	–	00H	√	√	√	√	√

Note This register is incorporated only in 48-pin products.

3.3 Instruction Address Addressing

An instruction address is determined by contents of the program counter (PC) and memory bank select register (BANK), and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to PC and branched by the following addressing (for details of instructions, refer to the **78K/0 Series Instructions User's Manual (U12326E)**).

3.3.1 Relative addressing

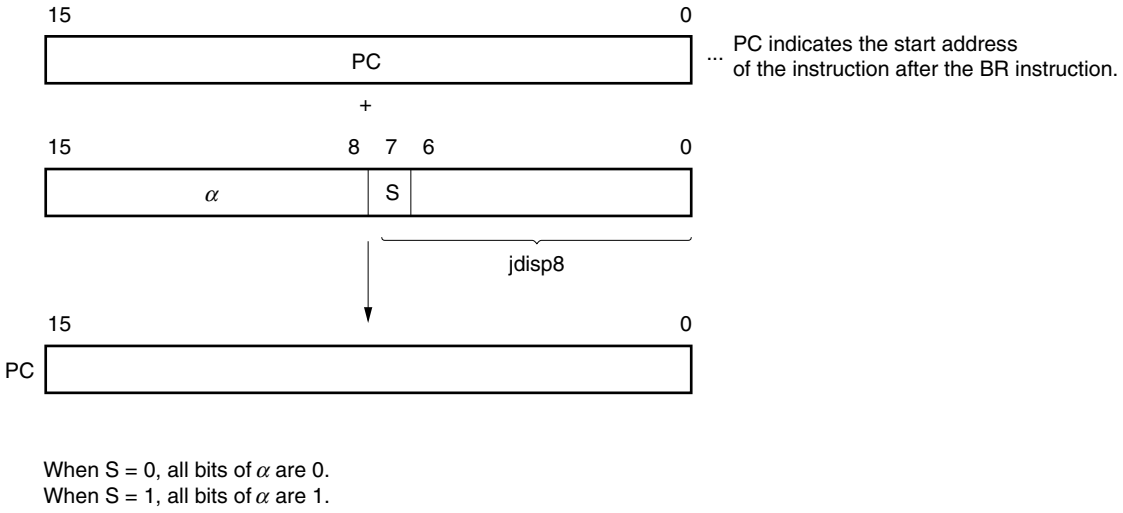
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit.

In other words, relative addressing consists of relative branching from the start address of the following instruction to the −128 to +127 range.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

Table 4-1. Memory Bank Address Representation

Memory Bank Number	CPU Address	Flash Memory Real Address	Address Representation in Simulator and Debugger[Note 1]
Memory bank 0	08000H-0BFFFH[Note 2]	08000H-0BFFFH	08000H-0BFFFH
Memory bank 1		0C000H-0FFFFH	18000H-1BFFFH
Memory bank 2		10000H-13FFFH	28000H-2BFFFH
Memory bank 3		14000H-17FFFH	38000H-3BFFFH
Memory bank 4		18000H-1BFFFH	48000H-4BFFFH
Memory bank 5		1C000H-1FFFFH	58000H-5BFFFH

Notes 1. SM+ for 78K0, SM+ for 78K0/Kx2, and ID78K0-QB

2. Set the memory bank to be used by the memory bank select register (BANK) (see **Figure 4-3**).

For details, see the **RA78K0 Ver. 3.80 Assembler Package Operation User's Manual (U17199E)** and the **78K0 Microcontrollers Self Programming Library Type01 User's Manual (U18274E)**.

4.3 Memory Bank Select Register (BANK)

The memory bank select register (BANK) is used to select a memory bank to be used.

BANK can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears BANK to 00H.

Figure 4-3. Format of Memory Bank Select Register (BANK)

Address: FFF3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BANK	0	0	0	0	0	BANK2	BANK1	BANK0

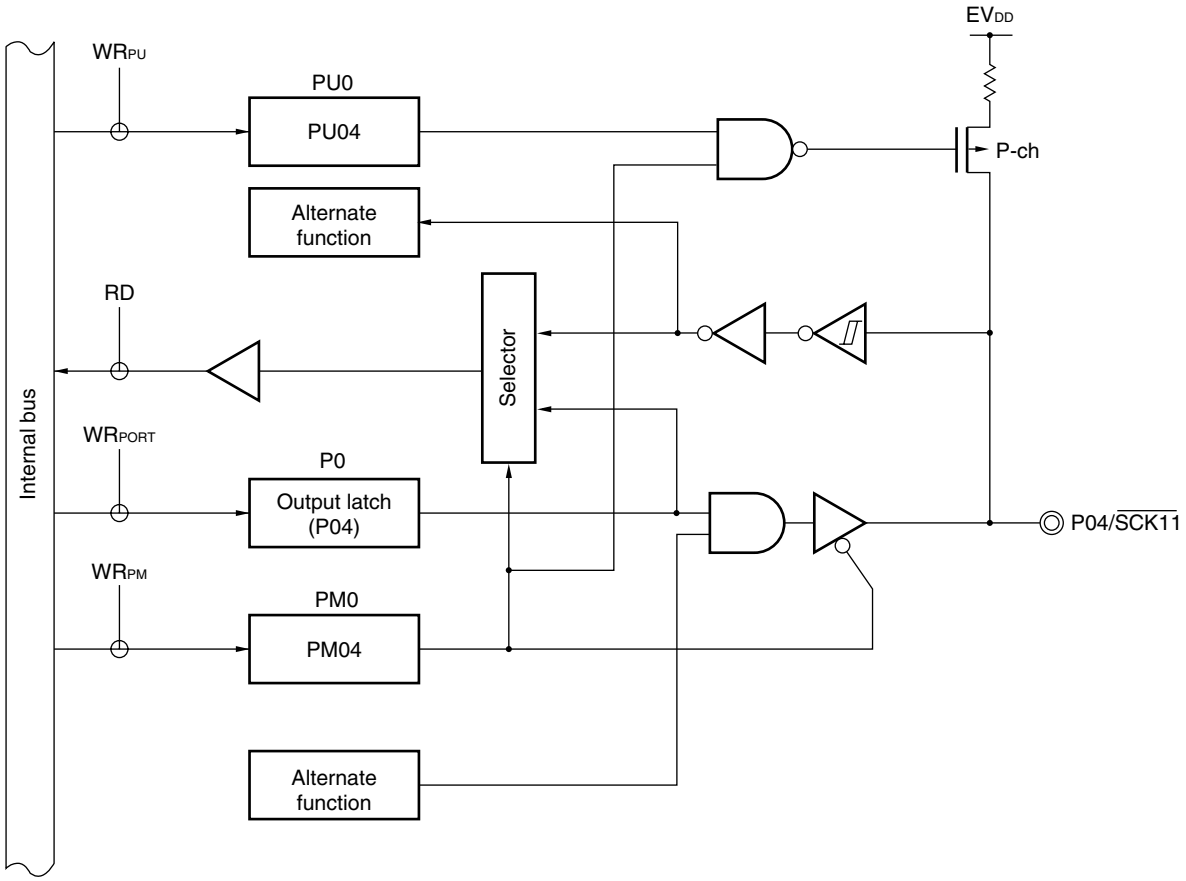
BANK2	BANK1	BANK0	Bank setting	
			μPD78F05x6 and 78F05x6A	μPD78F05x7, 78F05x7A, 78F05x7D, and 78F05x7DA
0	0	0	Common area (32 KB) + memory bank 0 (16 KB)	
0	0	1	Common area (32 KB) + memory bank 1 (16 KB)	
0	1	0	Common area (32 KB) + memory bank 2 (16 KB)	
0	1	1	Common area (32 KB) + memory bank 3 (16 KB)	
1	0	0	Setting prohibited	Common area (32 KB) + memory bank 4 (16 KB)
1	0	1		Common area (32 KB) + memory bank 5 (16 KB)
Other than above			Setting prohibited	

Caution Be sure to change the value of the BANK register in the common area (0000H to 7FFFH). If the value of the BANK register is changed in the bank area (8000H to BFFFH), an inadvertent program loop occurs in the CPU. Therefore, never change the value of the BANK register in the bank area.

Remark x = 2 to 4

Figure 5-5. Block Diagram of P04 (2/2)

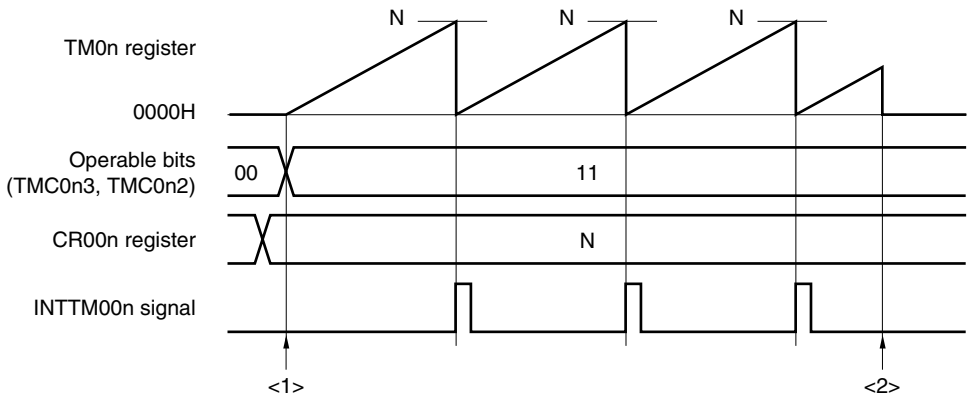
(2) 78K0/KE2 products whose flash memory is at least 48 KB and 78K0/KF2



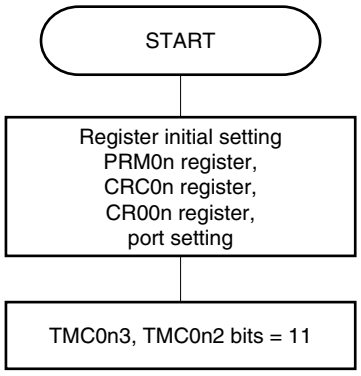
P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 7-19. Example of Software Processing for Interval Timer Function



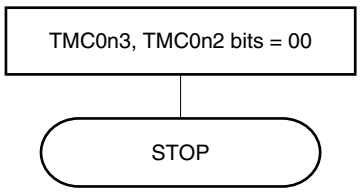
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC0n3 and TMC0n2 bits to 11.

Starts count operation

<2> Count operation stop flow

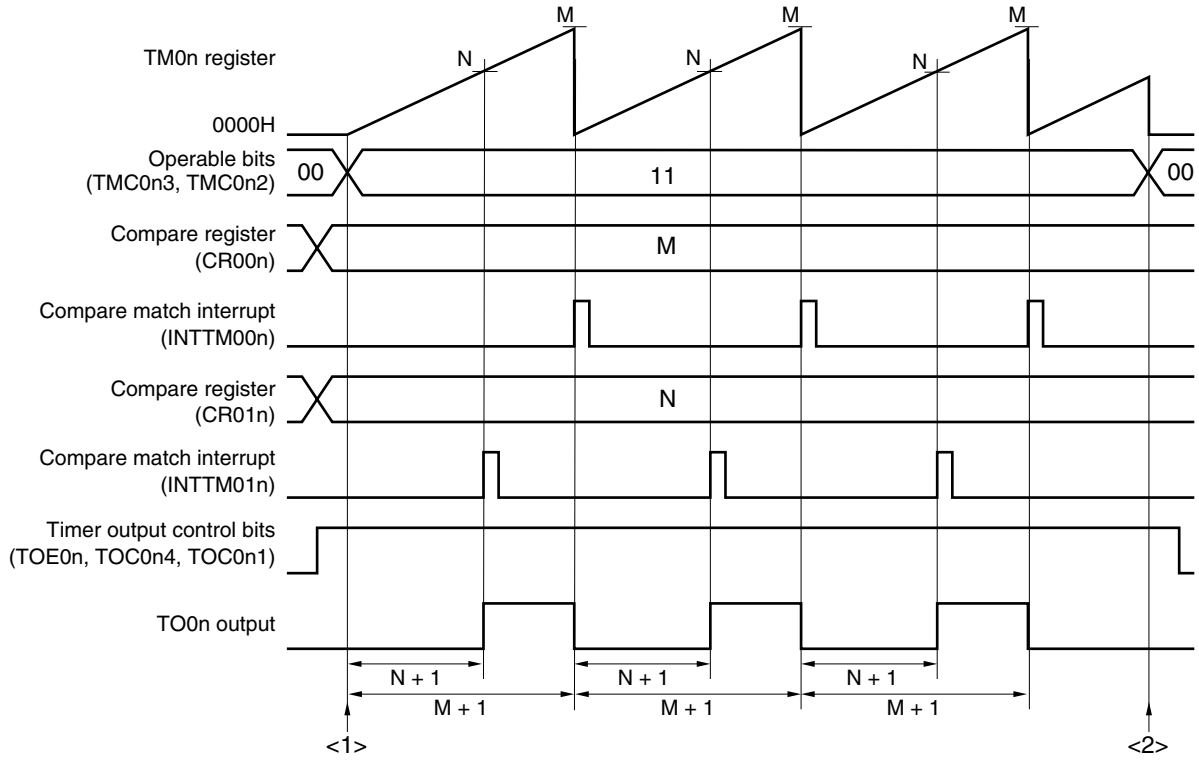


The counter is initialized and counting is stopped by clearing the TMC0n3 and TMC0n2 bits to 00.

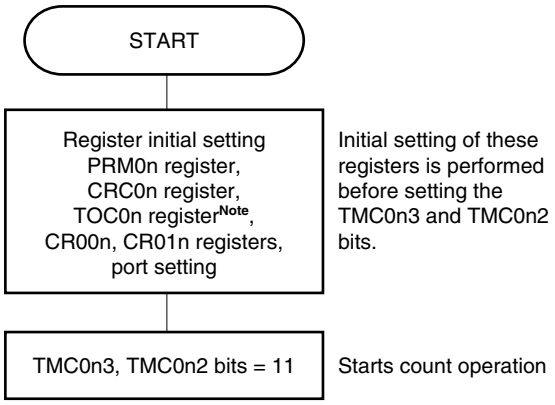
Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

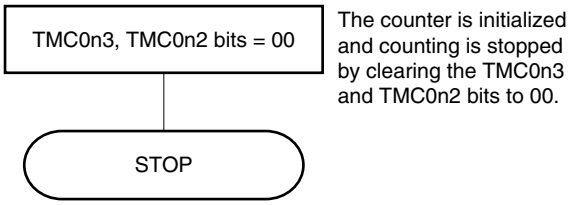
Figure 7-47. Example of Software Processing for PPG Output Operation



<1> Count operation start flow



<2> Count operation stop flow



Note Care must be exercised when setting TOC0n. For details, see **7.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remarks 1. PPG pulse cycle = (M + 1) × Count clock cycle
PPG duty = (N + 1)/(M + 1)

2. n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Notes 2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V ≤ V_{DD} < 2.7 V, the setting of CKS12 = CKS11 = CKS10 = 0 (count clock: f_{PRS}) is prohibited.

3. This is settable only if 4.0 V ≤ V_{DD} ≤ 5.5 V.

Cautions 1. When TMHE1 = 1, setting the other bits of TMHMD1 is prohibited. However, TMHMD1 can be refreshed (the same value is written).

2. In the PWM output mode and carrier generator mode, be sure to set the 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

3. When the carrier generator mode is used, set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

4. The actual TOH1/INTP5/P16 pin output is determined depending on PM16 and P16, besides TOH1 output.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. f_{RL}: Internal low-speed oscillation clock frequency

(2) 8-bit timer H carrier control register 1 (TMCYC1)

This register controls the remote control output and carrier pulse output status of 8-bit timer H1.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-7. Format of 8-Bit Timer H Carrier Control Register 1 (TMCYC1)

Address: FF6DH After reset: 00H R/W[Note]

	7	6	5	4	3	2	1	<0>
TMCYC1	0	0	0	0	0	RMC1	NRZB1	NRZ1

RMC1	NRZB1	Remote control output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

NRZ1	Carrier pulse output status flag
0	Carrier output disabled status (low-level status)
1	Carrier output enabled status (RMC1 = 1: Carrier pulse output, RMC1 = 0: High-level status)

Note Bit 0 is read-only.

Caution Do not rewrite RMC1 when TMHE = 1. However, TMCYC1 can be refreshed (the same value is written).

Caution Do not change the count clock and interval time (by setting bits 4 to 7 (WTM4 to WTM7) of WTM) during watch timer operation.

Remarks 1. f_W: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

15.2 Configuration of Serial Interface UART6

Serial interface UART6 includes the following hardware.

Table 15-1. Configuration of Serial Interface UART6

Item	Configuration
Registers	Receive buffer register 6 (RXB6) Receive shift register 6 (RXS6) Transmit buffer register 6 (TXB6) Transmit shift register 6 (TXS6)
Control registers	Asynchronous serial interface operation mode register 6 (ASIM6) Asynchronous serial interface reception error status register 6 (ASIS6) Asynchronous serial interface transmission status register 6 (ASIF6) Clock selection register 6 (CKSR6) Baud rate generator control register 6 (BRGC6) Asynchronous serial interface control register 6 (ASICL6) Input switch control register (ISC) Port mode register 1 (PM1) Port register 1 (P1)

16.2 Configuration of Serial Interfaces CSI10 and CSI11

Serial interfaces CSI10 and CSI11 include the following hardware.

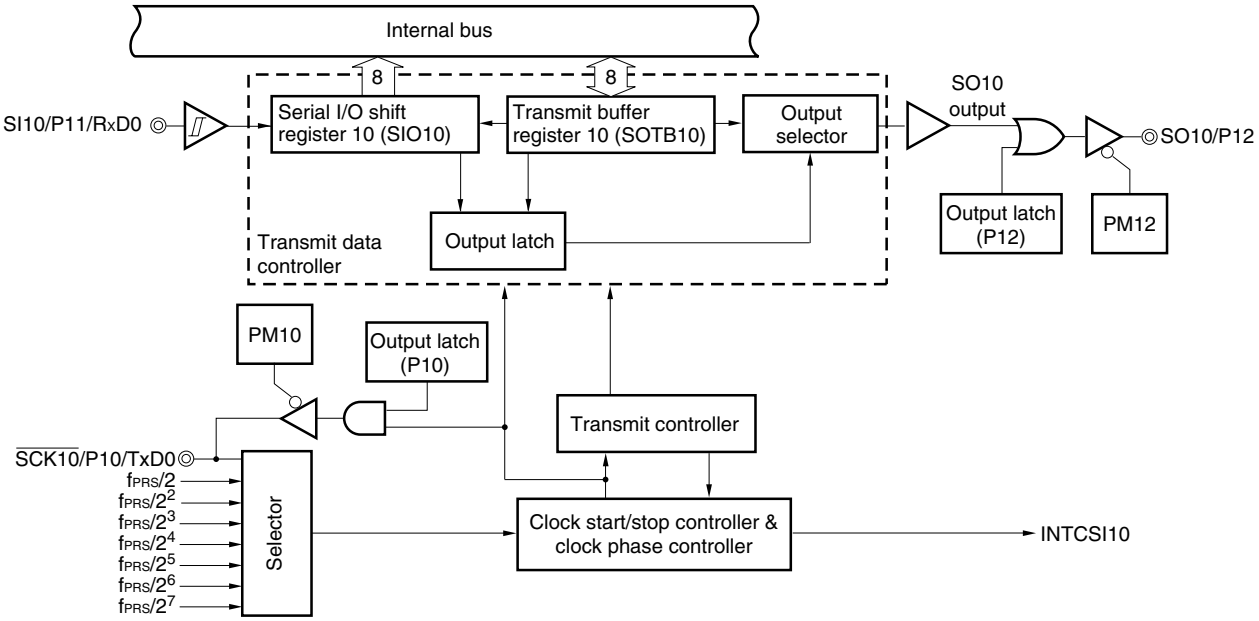
Table 16-1. Configuration of Serial Interfaces CSI10 and CSI11

Item	Configuration
Controller	Transmit controller Clock start/stop controller & clock phase controller
Registers	Transmit buffer register 1n (SOTB1n) Serial I/O shift register 1n (SIO1n)
Control registers	Serial operation mode register 1n (CSIM1n) Serial clock selection register 1n (CSIC1n) Port mode register 0 (PM0) or port mode register 1 (PM1) Port register 0 (P0) or port register 1 (P1)

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

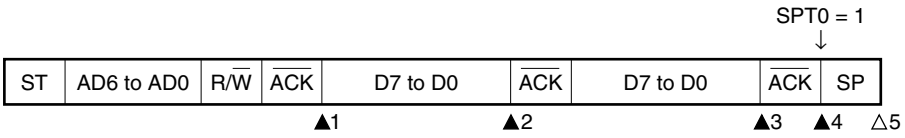
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 16-1. Block Diagram of Serial Interface CSI10



(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIM0 = 0

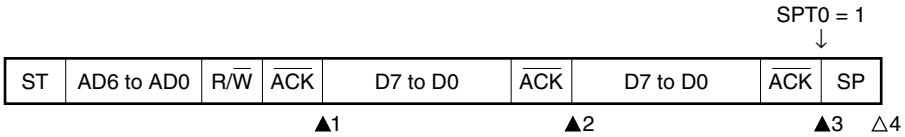


▲1: IICS0 = 1010×110B
▲2: IICS0 = 1010×000B
▲3: IICS0 = 1010×000B (Sets WTIM0 to 1[Note])
▲4: IICS0 = 1010××00B (Sets SPT0 to 1)
△5: IICS0 = 00000001B

Note To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIIC0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 1010×110B
▲2: IICS0 = 1010×100B
▲3: IICS0 = 1010××00B (Sets SPT0 to 1)
△4: IICS0 = 00001001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 22-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				fx = 10 MHz	fx = 20 MHz
0	0	1	2^{11}/fx	204.8 μs	102.4 μs
0	1	0	2^{13}/fx	819.2 μs	409.6 μs
0	1	1	2^{14}/fx	1.64 ms	819.2 μs
1	0	0	2^{15}/fx	3.27 ms	1.64 ms
1	0	1	2^{16}/fx	6.55 ms	3.27 ms
Other than above			Setting prohibited		

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

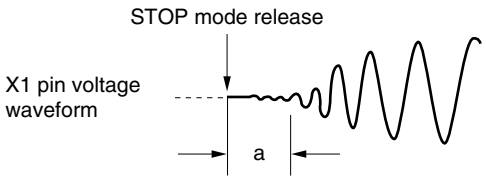
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

22.2 Standby Function Operation

22.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, internal high-speed oscillation clock, or subsystem clock[Note]. The operating statuses in the HALT mode are shown below.

Note The 78K0/KB2 is not provided with a subsystem clock.

Cautions 1. To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.

2. Even if "internal low-speed oscillator can be stopped by software" is selected by the option byte, the internal low-speed oscillation clock continues in the STOP mode in the status before the STOP mode is set. To stop the internal low-speed oscillator's oscillation in the STOP mode, stop it by software and then execute the STOP instruction.

3. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), switch the CPU clock to the internal high-speed oscillation clock before the execution of the STOP instruction using the following procedure.

<1> Set RSTOP to 0 (starting oscillation of the internal high-speed oscillator) → <2> Set MCM0 to 0 (switching the CPU from X1 oscillation to internal high-speed oscillation) → <3> Check that MCS is 0 (checking the CPU clock) → <4> Check that RSTS is 1 (checking internal high-speed oscillation operation) → <5> Execute the STOP instruction

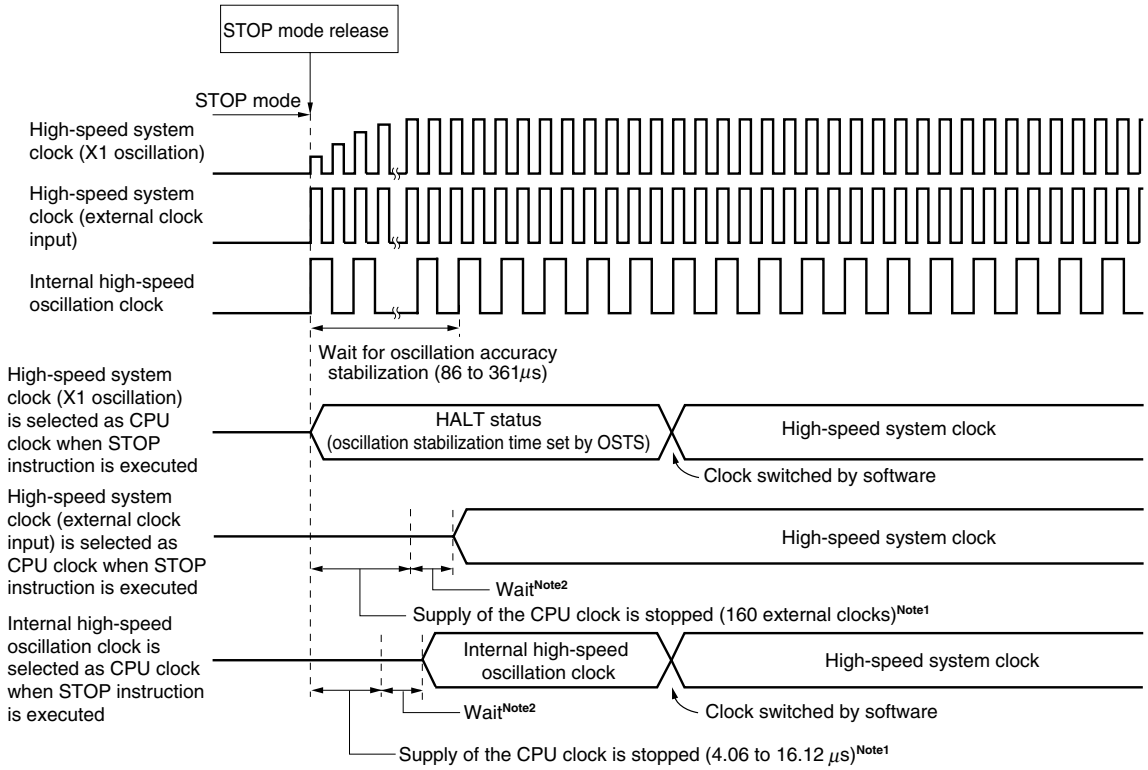
Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

4. If the STOP instruction is executed when AMPH = 1, supply of the CPU clock is stopped for 4.06 to 16.12 μs after the STOP mode is released when the internal high-speed oscillation clock is selected as the CPU clock, or for the duration of 160 external clocks when the high-speed system clock (external clock input) is selected as the CPU clock.

5. Execute the STOP instruction after having confirmed that the internal high-speed oscillator is operating stably (RSTS = 1).

(2) STOP mode release

Figure 22-5. Operation Timing When STOP Mode Is Released (When Unmasked Interrupt Request Is Generated)



Notes 1. When AMPH = 1

2. The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks

The STOP mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

- **Basic characteristics**

Parameter		Symbol	Conditions				MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}	f_{XP} = 10 MHz (TYP.), 20 MHz (MAX.)					4.5	11.0	mA
Erase time Notes 1, 2	All block	T_{eraca}						20	200	ms
	Block unit	T_{erasa}						20	200	ms
Write time (in 8-bit units) Note 1		T_{wrwa}						10	100	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite Note 3	Expanded-specification Products (μPD78F05xxA (A))	• When a flash memory programmer is used, and the libraries Note 4 provided by Renesas Electronics are used • For program update	Retention: 15 years	1000			Times
					• When the EEPROM emulation libraries Note 5 provided by Renesas Electronics are used • The rewritable ROM size: 4 KB • For data update	Retention: 5 years	10000			Times
				Expanded-specification Products (μPD78F05xxA (A))	Conditions other than the above Note 6	Retention: 10 years	100			Times
				Conventional-specification Products (μPD78F05xx (A))						

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP4 or PG-FP5, is used and the rewrite time during self programming, see **Tables 27-12** to **27-14**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

4. The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) is excluded.

5. The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) is excluded.

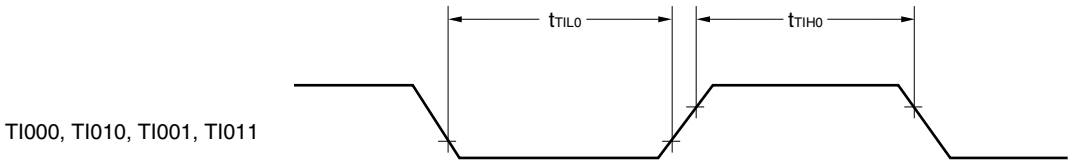
6. These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) and the sample program specified by **the 78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) are used.

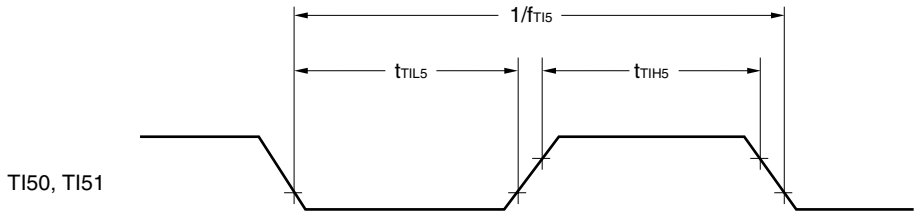
Remarks 1. f_{XP}: Main system clock oscillation frequency

2. For serial write operation characteristics, refer to **78K0/Kx2 Flash Memory Programming (Programmer) Application Note (**Document No.: **U17739E)**.

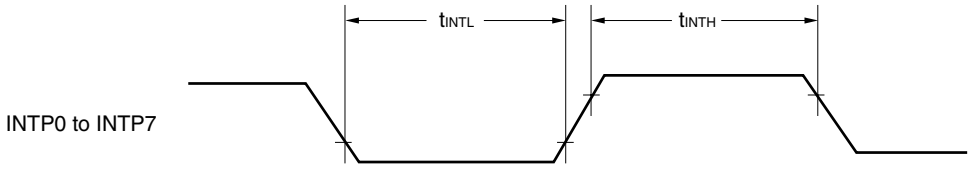
Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

TI Timing

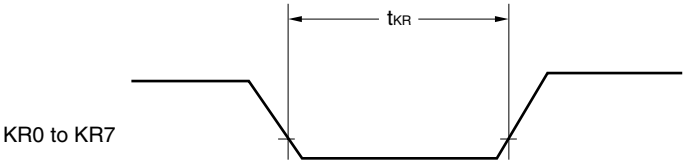




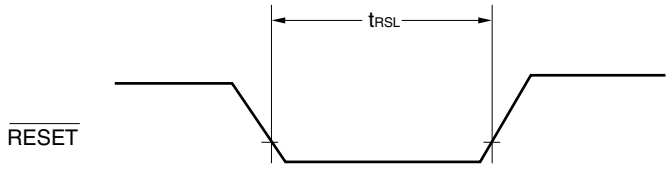
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

(f) CSIA0 (master mode, $\overline{SCKA0}$…internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKA0}$ cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V		600			ns
		2.7 V ≤ V_{DD} < 4.0 V		1200			ns
$\overline{SCKA0}$ high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3}/2$ – 50			ns
		2.7 V ≤ V_{DD} < 4.0 V		$t_{KCY3}/2$ – 100			ns
SIA0 setup time (to $\overline{SCKA0}$↑)	t_{SIK3}			100			ns
SIA0 hold time (from $\overline{SCKA0}$↑)	t_{KSI3}			300			ns
Delay time from $\overline{SCKA0}$↓ to SOA0 output	t_{KSO3}	C = 100 pF[Note]	4.0 V ≤ V_{DD} ≤ 5.5 V			200	ns
			2.7 V ≤ V_{DD} < 4.0 V			300	ns
Time from $\overline{SCKA0}$↑ to STB0↑	t_{SBD}			$t_{KCY3}/2$ – 100			ns
Strobe signal high-level width	t_{SBW}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY3} – 30			ns
		2.7 V ≤ V_{DD} < 4.0 V		t_{KCY3} – 60			ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}			100			ns
Time from busy inactive to $\overline{SCKA0}$↓	t_{SPS}	4.0 V ≤ V_{DD} ≤ 5.5 V				$2t_{KCY3}$ + 100	ns
		2.7 V ≤ V_{DD} < 4.0 V				$2t_{KCY3}$ – 150	ns

Note C is the load capacitance of the $\overline{SCKA0}$ and SOA0 output lines.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

2.7 V POC Circuit Characteristics (T_A = –40 to +110°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option bye) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until V_{POC} = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC}, similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until V_{DDPOC} = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at V_{POC} = 1.59 V (TYP.) and not at V_{DDPOC}. The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH}.