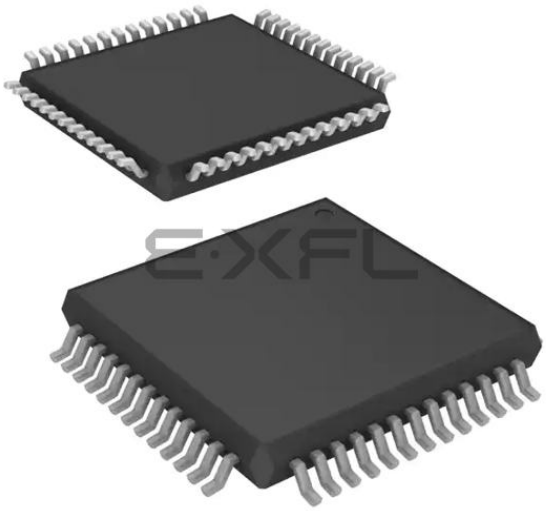
Renesas Electronics America Inc - UPD78F0523AGB-GAG-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0523agb-gag-ax

1.1.6 Interrupt response time for self programming library

(1) Conventional-specification products (μPD78F05xx and 78F05xxD) (1/2)

<1> When internal high-speed oscillation clock is used

Library Name	Interrupt Response Time (μs (Max.))			
	Normal Model of C Compiler		Static Model of C Compiler/Assembler	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	933.6	668.6	927.9	662.9
Block erase library	1026.6	763.6	1020.9	757.9
Word write library	2505.8	1942.8	2497.8	1934.8
Block verify library	958.6	693.6	952.9	687.9
Set information library	476.5	211.5	475.5	210.5
EEPROM write library	2760.8	2168.8	2759.5	2167.5

Remarks 1. The above interrupt response times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

<2> When high-speed system clock is used (normal model of C compiler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	179/f_{CPU} + 507	179/f_{CPU} + 407	179/f_{CPU} + 1650	179/f_{CPU} + 714
Block erase library	179/f_{CPU} + 559	179/f_{CPU} + 460	179/f_{CPU} + 1702	179/f_{CPU} + 767
Word write library	333/f_{CPU} + 1589	333/f_{CPU} + 1298	333/f_{CPU} + 2732	333/f_{CPU} + 1605
Block verify library	179/f_{CPU} + 518	179/f_{CPU} + 418	179/f_{CPU} + 1661	179/f_{CPU} + 725
Set information library	80/f_{CPU} + 370	80/f_{CPU} + 165	80/f_{CPU} + 1513	80/f_{CPU} + 472
EEPROM write library[Note]	29/f_{CPU} + 1759 333/f_{CPU} + 834	29/f_{CPU} + 1468 333/f_{CPU} + 512	29/f_{CPU} + 1759 333/f_{CPU} + 2061	29/f_{CPU} + 1468 333/f_{CPU} + 873

Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

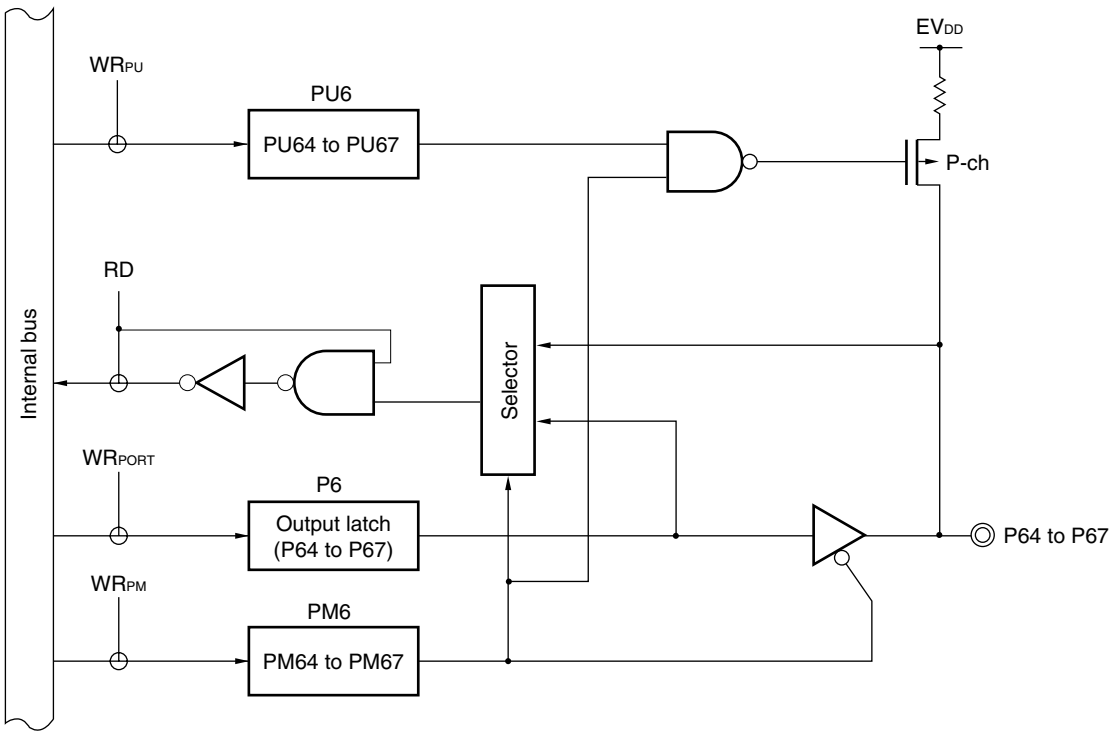
3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

(5/6)

78K0/Kx2 Microcontrollers	Package	Product type	Quality grace	Part Number
78K0/KE2	64-pin plastic LQFP (12x12)	Conventional-specification products	Standard products	μPD78F0531GK-UET-A, 78F0532GK-UET-A, 78F0533GK-UET-A, 78F0534GK-UET-A, 78F0535GK-UET-A, 78F0536GK-UET-A, 78F0537GK-UET-A, 78F0537DGK-UET-A[Note]
			(A) grade products	μPD78F0531GK(A)-GAJ-AX, 78F0532GK(A)-GAJ-AX, 78F0533GK(A)-GAJ-AX, 78F0534GK(A)-GAJ-AX, 78F0535GK(A)-GAJ-AX, 78F0536GK(A)-GAJ-AX, 78F0537GK(A)-GAJ-AX
			(A2) grade products	μPD78F0531GK(A2)-GAJ-AX, 78F0532GK(A2)-GAJ-AX, 78F0533GK(A2)-GAJ-AX, 78F0534GK(A2)-GAJ-AX, 78F0535GK(A2)-GAJ-AX, 78F0536GK(A2)-GAJ-AX, 78F0537GK(A2)-GAJ-AX
		Expanded-specification products	Standard products	μPD78F0531AGK-GAJ-AX, 78F0532AGK-GAJ-AX, 78F0533AGK-GAJ-AX, 78F0534AGK-GAJ-AX, 78F0535AGK-GAJ-AX, 78F0536AGK-GAJ-AX, 78F0537AGK-GAJ-AX, 78F0537DAGK-GAJ-AX[Note]
			(A) grade products	μPD78F0531AGKA-GAJ-G, 78F0532AGKA-GAJ-G, 78F0533AGKA-GAJ-G, 78F0534AGKA-GAJ-G, 78F0535AGKA-GAJ-G, 78F0536AGKA-GAJ-G, 78F0537AGKA-GAJ-G
			(A2) grade products	μPD78F0531AGKA2-GAJ-G, 78F0532AGKA2-GAJ-G, 78F0533AGKA2-GAJ-G, 78F0534AGKA2-GAJ-G, 78F0535AGKA2-GAJ-G, 78F0536AGKA2-GAJ-G, 78F0537AGKA2-GAJ-G
	64-pin plastic TQFP (fine pitch) (7x7)	Conventional-specification products	Standard products	μPD78F0531GA-9EV-A, 78F0532GA-9EV-A, 78F0533GA-9EV-A, 78F0534GA-9EV-A, 78F0535GA-9EV-A, 78F0536GA-9EV-A, 78F0537GA-9EV-A, 78F0537DGA-9EV-A[Note]
		Expanded-specification products	Standard products	μPD78F0531AGA-HAB-AX, 78F0532AGA-HAB-AX, 78F0533AGA-HAB-AX, 78F0534AGA-HAB-AX, 78F0535AGA-HAB-AX, 78F0536AGA-HAB-AX, 78F0537AGA-HAB-AX, 78F0537DAGA-HAB-AX[Note]

Note The μPD78F0537D and 78F0537DA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

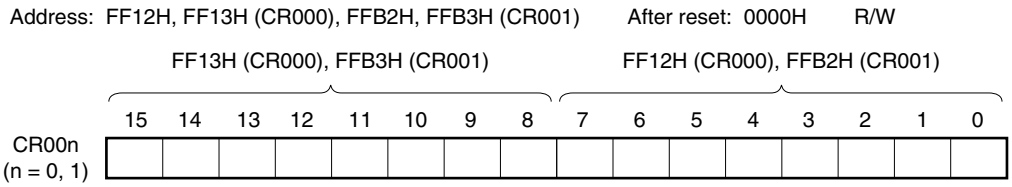
Figure 5-20. Block Diagram of P64 to P67



P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

Figure 7-4. Format of 16-Bit Timer Capture/Compare Register 00n (CR00n)



(i) When CR00n is used as a compare register

The value set in CR00n is constantly compared with the TM0n count value, and an interrupt request signal (INTTM00n) is generated if they match. The value is held until CR00n is rewritten.

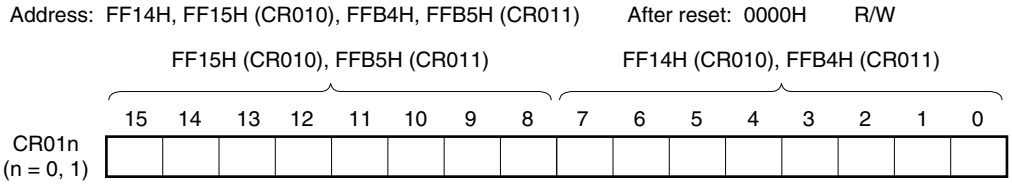
Caution CR00n does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR00n is used as a capture register

The count value of TM0n is captured to CR00n when a capture trigger is input.

As the capture trigger, an edge of a phase reverse to that of the TI00n pin or the valid edge of the TI01n pin can be selected by using CRC0n or PRM0n.

Figure 7-5. Format of 16-Bit Timer Capture/Compare Register 01n (CR01n)



(i) When CR01n is used as a compare register

The value set in CR01n is constantly compared with the TM0n count value, and an interrupt request signal (INTTM01n) is generated if they match.

Caution CR01n does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR01n is used as a capture register

The count value of TM0n is captured to CR01n when a capture trigger is input.

It is possible to select the valid edge of the TI00n pin as the capture trigger. The TI00n pin valid edge is set by PRM0n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-18. Example of Register Settings for Interval Timer Operation

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	1	1	0	0

Clears and starts on match between TM0n and CR00n.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0	0	0

CR00n used as compare register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0	0	0	0

(d) Prescaler mode register 0n (PRM0n)

ES1n1	ES1n0	ES0n1	ES0n0	3	2	PRM0n1	PRM0n0
0	0	0	0	0	0	0/1	0/1

Selects count clock

(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

If M is set to CR00n, the interval time is as follows.

- Interval time = (M + 1) × Count clock cycle

Setting CR00n to 0000H is prohibited.

(g) 16-bit capture/compare register 01n (CR01n)

Usually, CR01n is not used for the interval timer function. However, a compare match interrupt (INTTM01n) is generated when the set value of CR01n matches the value of TM0n.

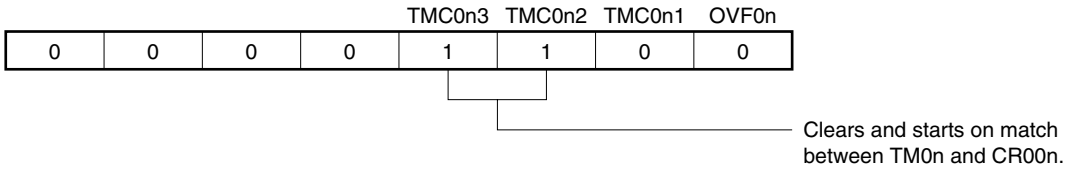
Therefore, mask the interrupt request by using the interrupt mask flag (TMMK01n).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

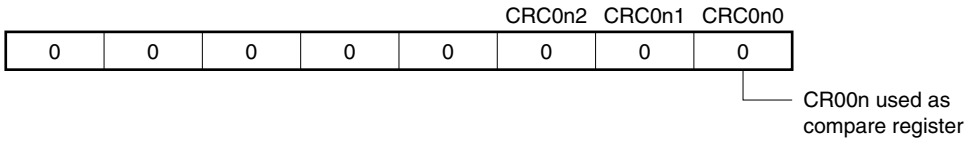
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-22. Example of Register Settings for Square-Wave Output Operation

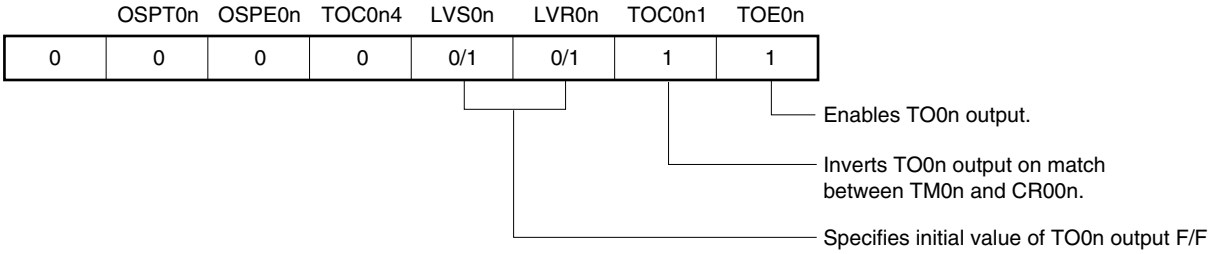
(a) 16-bit timer mode control register 0n (TMC0n)



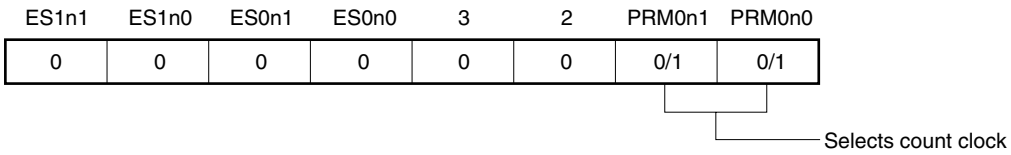
(b) Capture/compare control register 0n (CRC0n)



(c) 16-bit timer output control register 0n (TOC0n)



(d) Prescaler mode register 0n (PRM0n)



(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

If M is set to CR00n, the interval time is as follows.

- Square wave frequency = 1 / [2 × (M + 1) × Count clock cycle]

Setting CR00n to 0000H is prohibited.

(g) 16-bit capture/compare register 01n (CR01n)

Usually, CR01n is not used for the square-wave output function. However, a compare match interrupt (INTTM01n) is generated when the set value of CR01n matches the value of TM0n.

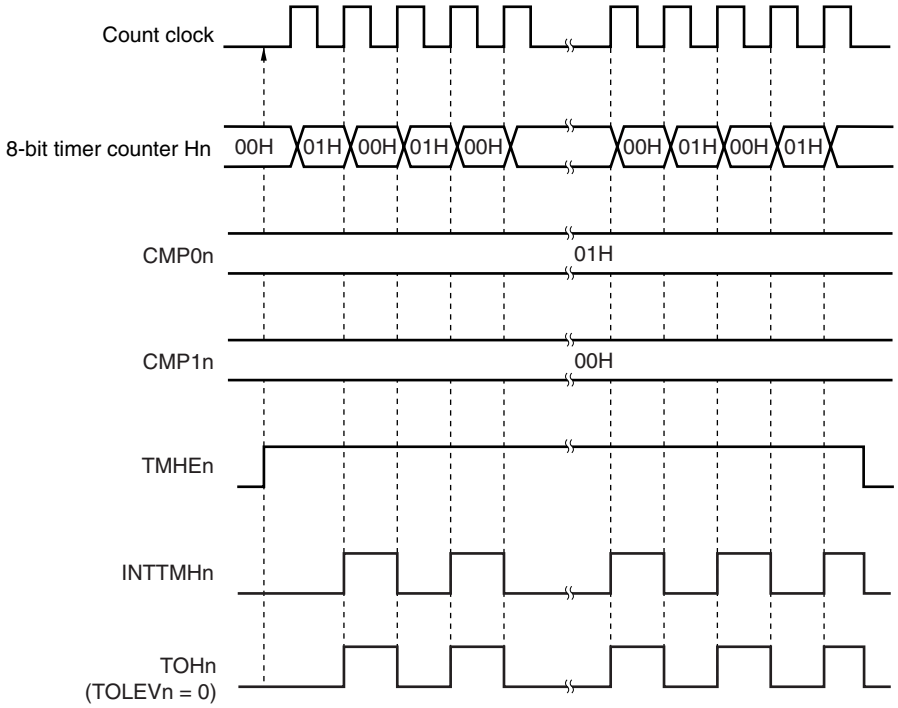
Therefore, mask the interrupt request by using the interrupt mask flag (TMMK01n).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 9-12. Operation Timing in PWM Output Mode (3/4)

(d) Operation when CMP0n = 01H, CMP1n = 00H



Remark n = 0, 1

Caution Do not change the count clock and interval time (by setting bits 4 to 7 (WTM4 to WTM7) of WTM) during watch timer operation.

Remarks 1. f_W: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

The setting methods are described below.

<1> Set bit 0 (ADCE) of the A/D converter mode register (ADM) to 1.
<2> Set the channel to be used in the analog input mode by using bits 3 to 0 (ADPC3 to ADPC0) of the A/D port configuration register (ADPC) and bits 7 to 0 (PM27 to PM20) of port mode register 2 (PM2).
<3> Select conversion time by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of ADM.
<4> Select a channel to be used by using bits 2 to 0 (ADS2 to ADS0) of the analog input channel specification register (ADS).
<5> Set bit 7 (ADCS) of ADM to 1 to start A/D conversion.
<6> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<7> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Change the channel>

<8> Change the channel using bits 2 to 0 (ADS2 to ADS0) of ADS to start A/D conversion.
<9> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<10> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

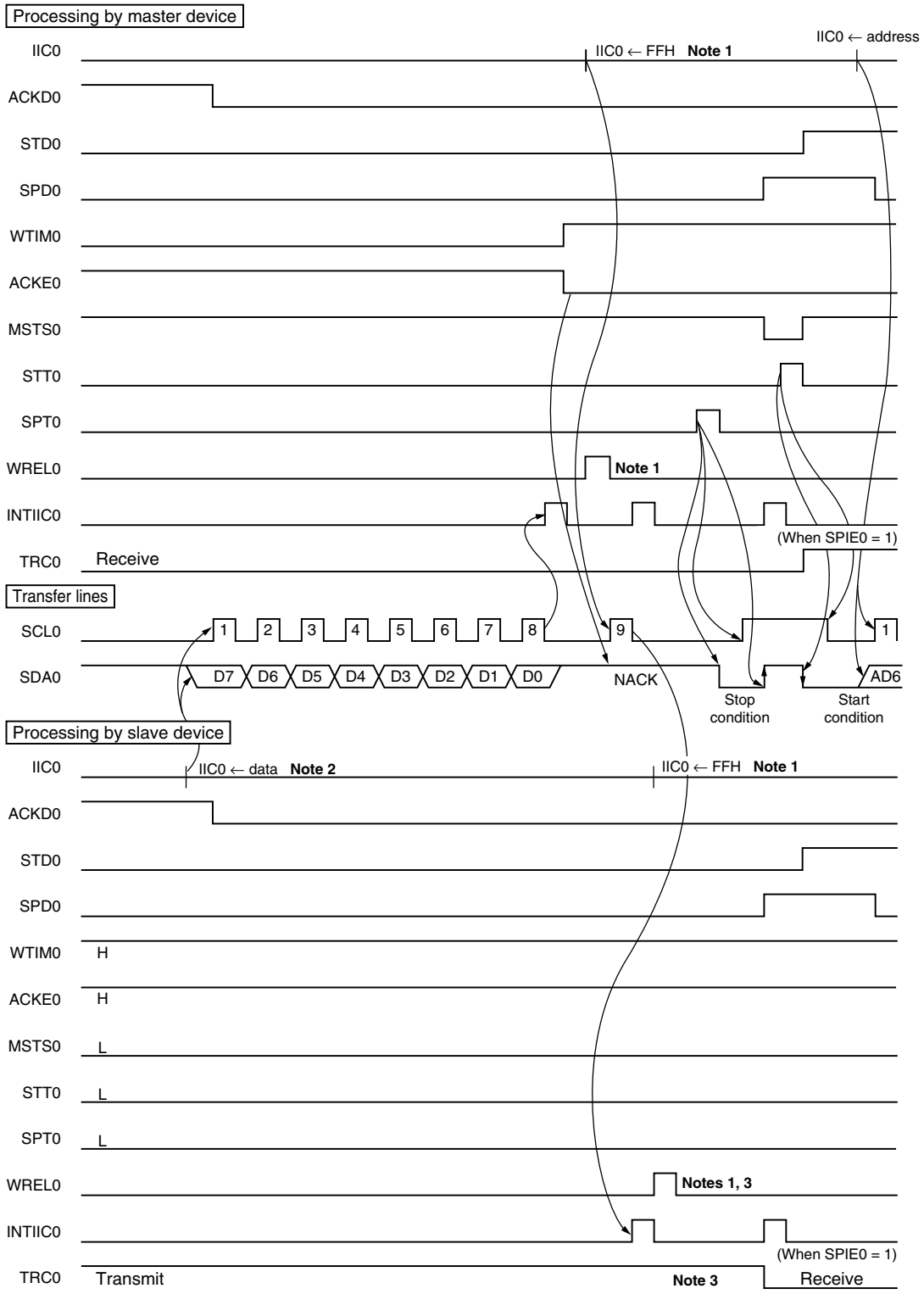
<Complete A/D conversion>

<11> Clear ADCS to 0.
<12> Clear ADCE to 0.

Cautions 1. Make sure the period of <1> to <5> is 1 μs or more.
2. <1> may be done between <2> and <4>.
3. <1> can be omitted. However, ignore data of the first conversion after <5> in this case.
4. The period from <6> to <9> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM. The period from <8> to <9> is the conversion time set using FR2 to FR0, LV1, and LV0.

Figure 18-28. Example of Slave to Master Communication
(When 8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Stop condition



Notes 1. To cancel wait, write “FFH” to IIC0 or set WREL0.

2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

3. If a wait state during slave transmission is canceled by setting WREL0, TRC0 will be cleared.

Figure 20-10. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KE2)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	SREMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK010	TMMK000	TMMK50	TMMKH0	TMMKH1	DUALMK0 CSIMK10 STMK0	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	PMK7	PMK6	WTMK	KRMK	TMMK51	WTIMK	SRMK0	ADMK

Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
MK1H	1	1	1	1	TMMK011[Note]	TMMK001[Note]	CSIMK11[Note]	IICMK0 DMUMK[Note]

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note Products whose flash memory is at least 48 KB only.

Caution Be sure to set bits 1 to 7 of MK1H to 1 for the products whose flash memory is less than 32 KB. Be sure to set bits 4 to 7 of MK1H to 1 for the products whose flash memory is at least 48 KB.

Table 22-3. Operating Statuses in STOP Mode

Item \ STOP Mode Setting			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{RH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EXCLK})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{RH}	Stopped		
		f_X			
		f_{EXCLK}	Input invalid		
	Subsystem clock	f_{XT}	Status before STOP mode was set is retained		
		f_{EXCLKS}	Operates or stops by external clock input		
	f_{RL}		Status before STOP mode was set is retained		
CPU			Operation stopped		
Flash memory					
RAM			Status before STOP mode was set is retained		
Port (latch)					
16-bit timer/event counter		00[Note 1]	Operation stopped		
		01[Note 1]			
8-bit timer/event counter		50[Note 1]	Operable only when TI50 is selected as the count clock		
		51[Note 1]	Operable only when TI51 is selected as the count clock		
8-bit timer		H0	Operable only when TM50 output is selected as the count clock during 8-bit timer/event counter 50 operation		
		H1	Operable only when f_{RL}, $f_{RL}/2^7$, $f_{RL}/2^9$ is selected as the count clock		
Watch timer			Operable only when subsystem clock is selected as the count clock		
Watchdog timer			Operable. Clock supply to watchdog timer stops when “internal low-speed oscillator can be stopped by software” is set by option byte.		
Clock output			Operable only when subsystem clock is selected as the count clock		
Buzzer output			Operation stopped		
A/D converter					
Serial interface	UART0		Operable only when TM50 output is selected as the serial clock during 8-bit timer/event counter 50 operation		
	UART6				
	CSI10[Note 1]		Operable only when external clock is selected as the serial clock		
	CSI11[Note 1]				
	CSIA0[Note 1]		Operation stopped		
	IIC0[Note 1]		Operable only when the external clock from EXSCL0/P62 pin is selected as the serial clock[Note 2]		
Multiplier/divider			Operation stopped		
Power-on-clear function			Operable		
Low-voltage detection function					
External interrupt					

Notes 1. Do not start operation of these functions on the external clock input from peripheral hardware pins in the stop mode.

2. The operation of 78K0/KB2 products is stopped (The external clock from the EXSCL0/P62 pin cannot be selected, because the EXSCL0/P62 pin is not mounted.).

Remarks 1. f_{RH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{XT}: XT1 clock
f_{EXCLKS}: External subsystem clock, f_{RL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. See **1.7 Block Diagram** and **1.8 Outline of Functions**.

27.9 Processing Time for Each Command When PG-FP4 or PG-FP5 Is Used (Reference)

The following table shows the processing time for each command (reference) when the PG-FP4 or PG-FP5 is used as a dedicated flash memory programmer.

Table 27-12. Processing Time for Each Command When PG-FP4 or PG-FP5 Is Used (Reference) (1/2)

(1) Products with internal ROMs of the 32 KB

Command of PG-FP4	Port: CSI-Internal-OSC (Internal high-speed oscillation clock (f_{RH})), Speed: 2.5 MHz	Port: UART-Ext-FP4CK (External main system clock (f_{EXCLK})), Speed: 115,200 bps	
		Frequency: 2.0 MHz	Frequency: 20 MHz
Signature	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)
Blankcheck	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)
Erase	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)
Program	2.5 s (TYP.)	5 s (TYP.)	5 s (TYP.)
Verify	1.5 s (TYP.)	4 s (TYP.)	3.5 s (TYP.)
E.P.V	3.5 s (TYP.)	6 s (TYP.)	6 s (TYP.)
Checksum	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)
Security	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)

(2) Products with internal ROMs of the 60 KB

Command of PG-FP4	Port: CSI-Internal-OSC (Internal high-speed oscillation clock (f_{RH})), Speed: 2.5 MHz	Port: UART-Ext-FP4CK (External main system clock (f_{EXCLK})), Speed: 115,200 bps	
		Frequency: 2.0 MHz	Frequency: 20 MHz
Signature	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)
Blankcheck	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Erase	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Program	5 s (TYP.)	9 s (TYP.)	9 s (TYP.)
Verify	2 s (TYP.)	6.5 s (TYP.)	6.5 s (TYP.)
E.P.V	6 s (TYP.)	10.5 s (TYP.)	10.5 s (TYP.)
Checksum	0.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Security	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)

Caution When executing boot swapping, do not use the E.P.V. command with the dedicated flash memory programmer.

Table 27-16. Interrupt Response Time for Self Programming Library (Expanded-specification Products (μPD78F05xxA and 78F05xxDA)) (1/2)

(1) When internal high-speed oscillation clock is used

Library Name	Interrupt Response Time (μs (Max.))			
	Normal Model of C Compiler		Static Model of C Compiler/Assembler	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	1100.9	431.9	1095.3	426.3
Block erase library	1452.9	783.9	1447.3	778.3
Word write library	1247.2	579.2	1239.2	571.2
Block verify library	1125.9	455.9	1120.3	450.3
Set information library	906.9	312.0	905.8	311.0
EEPROM write library	1215.2	547.2	1213.9	545.9

Remarks 1. The above interrupt response times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

(2) When high-speed system clock is used (normal model of C compiler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	179/f_{CPU} + 567	179/f_{CPU} + 246	179/f_{CPU} + 1708	179/f_{CPU} + 569
Block erase library	179/f_{CPU} + 780	179/f_{CPU} + 459	179/f_{CPU} + 1921	179/f_{CPU} + 782
Word write library	333/f_{CPU} + 763	333/f_{CPU} + 443	333/f_{CPU} + 1871	333/f_{CPU} + 767
Block verify library	179/f_{CPU} + 580	179/f_{CPU} + 259	179/f_{CPU} + 1721	179/f_{CPU} + 582
Set information library	80/f_{CPU} + 456	80/f_{CPU} + 200	80/f_{CPU} + 1598	80/f_{CPU} + 459
EEPROM write library[Note]	29/f_{CPU} + 767 333/f_{CPU} + 696	29/f_{CPU} + 447 333/f_{CPU} + 376	29/f_{CPU} + 767 333/f_{CPU} + 1838	29/f_{CPU} + 447 333/f_{CPU} + 700

Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Flash Memory Programming Characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

• Basic characteristics

Parameter		Symbol	Conditions				MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}	f_{XP} = 10 MHz (TYP.), 20 MHz (MAX.)					4.5	16.0	mA
Erase time Notes 1, 2	All block	T_{eraca}						20	200	ms
	Block unit	T_{erasa}						20	200	ms
Write time (in 8-bit units) Note 1		T_{wrwa}						10	100	μs
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite Note 3	Expanded-specification Products (μPD78F05xxA (A2))	• When a flash memory programmer is used, and the libraries Note 4 provided by Renesas Electronics are used • For program update	Retention: 15 years	1000			Times
					• When the EEPROM emulation libraries Note 5 provided by Renesas Electronics are used • The rewritable ROM size: 4 KB • For data update	Retention: 5 years	10000			Times
				Expanded-specification Products (μPD78F05xxA (A2))	Conditions other than the above Note 6	Retention: 10 years	100			Times
				Conventional-specification Products (μPD78F05xx (A2))						

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP4 or PG-FP5, is used and the rewrite time during self programming, see **Tables 27-12** to **27-14**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

4. The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) is excluded.

5. The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) is excluded.

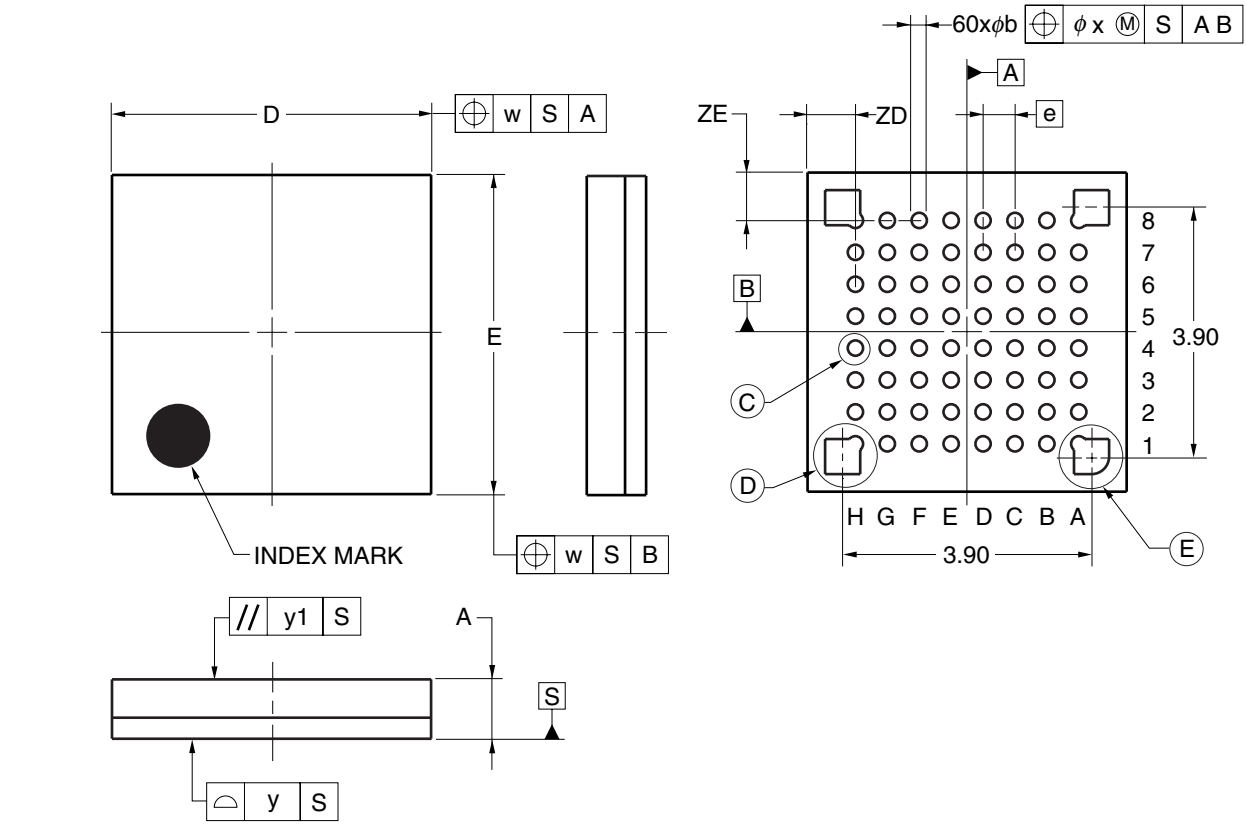
6. These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User’s Manual** (Document No.: **U17516E**) and the sample program specified by **the 78K0/Kx2 EEPROM Emulation Application Note** (Document No.: **U17517E**) are used.

Remarks 1. f_{XP}: Main system clock oscillation frequency

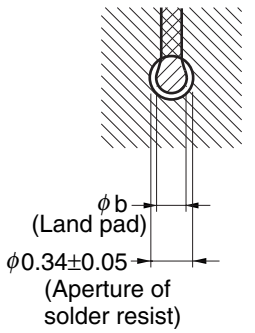
2. For serial write operation characteristics, refer to **78K0/Kx2 Flash Memory Programming (Programmer) Application Note (**Document No.: **U17739E)**.

- μPD78F0531FC-AA1-A, 78F0532FC-AA1-A, 78F0533FC-AA1-A, 78F0534FC-AA1-A, 78F0535FC-AA1-A, 78F0536FC-AA1-A, 78F0537FC-AA1-A, 78F0537DFC-AA1-A
- μPD78F0531AFC-AA1-A, 78F0532AFC-AA1-A, 78F0533AFC-AA1-A, 78F0534AFC-AA1-A, 78F0535AFC-AA1-A, 78F0536AFC-AA1-A, 78F0537AFC-AA1-A, 78F0537DAFC-AA1-A

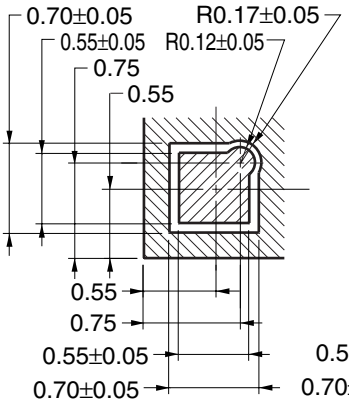
64-PIN PLASTIC FLGA(5x5)



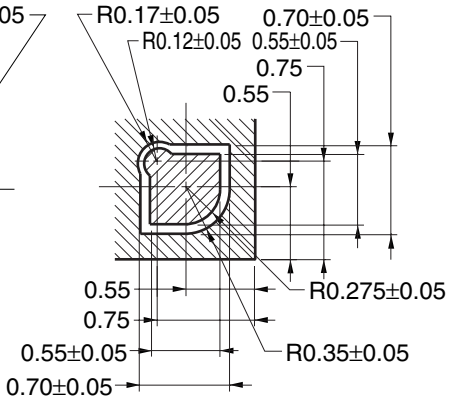
DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART



DETAIL OF Ⓔ PART



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.91±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AA1-1

[T]

[W]

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 14	Soft	Serial interface UART0	POWER0, TXE0, RXE0: Bits 7, 6, 5 of ASIM0	Clear POWER0 to 0 after clearing TXE0 and RXE0 to 0 to set the operation stop mode. To start the communication, set POWER0 to 1, and then set TXE0 or RXE0 to 1.	p. 441 ☐
			UART mode	Take relationship with the other party of communication when setting the port mode register and port register.	p. 442 ☐
			UART transmission	After transmit data is written to TXS0, do not write the next transmit data before the transmission completion interrupt signal (INTST0) is generated.	p. 445 ☐
			UART reception	If a reception error occurs, read asynchronous serial interface reception error status register 0 (ASIS0) and then read receive buffer register 0 (RXB0) to clear the error flag. Otherwise, an overrun error will occur when the next data is received, and the reception error status will persist.	p. 446 ☐
				Reception is always performed with the “number of stop bits = 1”. The second stop bit is ignored.	p. 446 ☐
			Error of baud rate	Keep the baud rate error during transmission to within the permissible error range at the reception destination.	p. 450 ☐
				Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.	p. 450 ☐
			Permissible baud rate range during reception	Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.	p. 451 ☐
Chapter 15	Soft	Serial interface UART6	UART mode	The TxD6 output inversion function inverts only the transmission side and not the reception side. To use this function, the reception side must be ready for reception of inverted data.	p. 453 ☐
				If clock supply to serial interface UART6 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART6 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD6 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER6 = 0, RXE6 = 0, and TXE6 = 0.	p. 453 ☐
				Set POWER6 = 1 and then set TXE6 = 1 (transmission) or RXE6 = 1 (reception) to start communication.	p. 453 ☐
				TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.	p. 453 ☐
				Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.	p. 453 ☐
				If data is continuously transmitted, the communication timing from the stop bit to the next start bit is extended two operating clocks of the macro. However, this does not affect the result of communication because the reception side initializes the timing when it has detected a start bit. Do not use the continuous transmission function if the interface is used in LIN communication operation.	p. 453 ☐
			TXB6: Transmit buffer register 6	Do not write data to TXB6 when bit 1 (TXBF6) of asynchronous serial interface transmission status register 6 (ASIF6) is 1.	p. 459 ☐
				Do not refresh (write the same value to) TXB6 by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) are 1 or when bits 7 and 5 (POWER6, RXE6) of ASIM6 are 1).	p. 459 ☐
				Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.	p. 459 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 15	Soft	Serial interface UART6	ASIM6: Asynchronous serial interface operation mode register 6	To start the transmission, set POWER6 to 1 and then set TXE6 to 1. To stop the transmission, clear TXE6 to 0, and then clear POWER6 to 0.	p. 461 ☐
				To start the reception, set POWER6 to 1 and then set RXE6 to 1. To stop the reception, clear RXE6 to 0, and then clear POWER6 to 0.	p. 461 ☐
				Set POWER6 to 1 and then set RXE6 to 1 while a high level is input to the RxD6 pin. If POWER6 is set to 1 and RXE6 is set to 1 while a low level is input, reception is started.	p. 461 ☐
				TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.	p. 461 ☐
				Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.	p. 461 ☐
				Clear the TXE6 and RXE6 bits to 0 before rewriting the PS61, PS60, and CL6 bits.	p. 461 ☐
				Fix the PS61 and PS60 bits to 0 when used in LIN communication operation.	p. 461 ☐
				Clear TXE6 to 0 before rewriting the SL6 bit. Reception is always performed with “the number of stop bits = 1”, and therefore, is not affected by the set value of the SL6 bit.	p. 461 ☐
				Make sure that RXE6 = 0 when rewriting the ISRM6 bit.	p. 461 ☐
			ASIS6: Asynchronous serial interface reception error status register 6	The operation of the PE6 bit differs depending on the set values of the PS61 and PS60 bits of asynchronous serial interface operation mode register 6 (ASIM6).	p. 462 ☐
				For the stop bit of the receive data, only the first bit is checked regardless of the number of stop bits.	p. 462 ☐
				If an overrun error occurs, the next receive data is not written to receive buffer register 6 (RXB6) but discarded.	p. 462 ☐
				If data is read from ASIS6, a wait cycle is generated. Do not read data from ASIS6 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.	p. 462 ☐
			ASIF6: Asynchronous serial interface transmission status register 6	To transmit data continuously, write the first transmit data (first byte) to the TXB6 register. Be sure to check that the TXBF6 flag is “0”. If so, write the next transmit data (second byte) to the TXB6 register. If data is written to the TXB6 register while the TXBF6 flag is “1”, the transmit data cannot be guaranteed.	p. 463 ☐
				To initialize the transmission unit upon completion of continuous transmission, be sure to check that the TXSF6 flag is “0” after generation of the transmission completion interrupt, and then execute initialization. If initialization is executed while the TXSF6 flag is “1”, the transmit data cannot be guaranteed.	p. 463 ☐
			CKSR6: Clock selection register 6	Make sure POWER6 = 0 when rewriting TPS63 to TPS60.	p. 465 ☐
			BRGC6: Baud rate generator control register 6	Make sure that bit 6 (TXE6) and bit 5 (RXE6) of the ASIM6 register = 0 when rewriting the MDL67 to MDL60 bits.	p. 465 ☐
	Hard			The baud rate is the output clock of the 8-bit counter divided by 2.	p. 465 ☐
	Soft		ASICL6: Asynchronous serial interface control register 6	ASICL6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1). However, do not set both SBRT6 and SBTT6 to 1 by a refresh operation during SBF reception (SBRT6 = 1) or SBF transmission (until INTST6 occurs since SBTT6 has been set (1)), because it may re-trigger SBF reception or SBF transmission.	p. 466 ☐
				In the case of an SBF reception error, the mode returns to the SBF reception mode. The status of the SBRF6 flag is held (1).	p. 467 ☐
				Before setting the SBRT6 bit, make sure that bit 7 (POWER6) and bit 5 (RXE6) of ASIM6 = 1. After setting the SBRT6 bit to 1, do not clear it to 0 before SBF reception is completed (before an interrupt request signal is generated).	p. 467 ☐