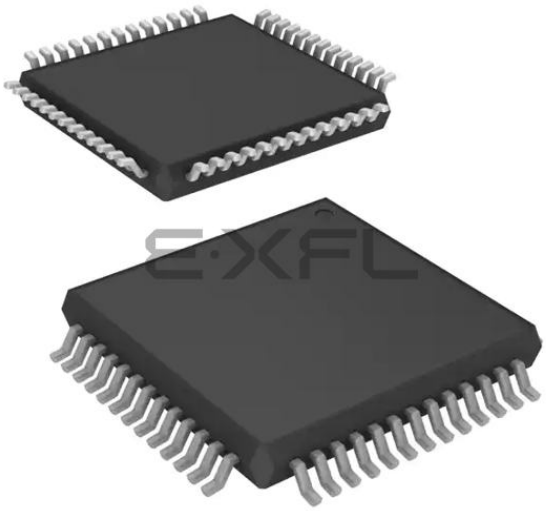
Renesas Electronics America Inc - UPD78F0524AGB-GAG-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0524agb-gag-ax

1.1.6 Interrupt response time for self programming library

(1) Conventional-specification products (μPD78F05xx and 78F05xxD) (1/2)

<1> When internal high-speed oscillation clock is used

Library Name	Interrupt Response Time (μs (Max.))			
	Normal Model of C Compiler		Static Model of C Compiler/Assembler	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	933.6	668.6	927.9	662.9
Block erase library	1026.6	763.6	1020.9	757.9
Word write library	2505.8	1942.8	2497.8	1934.8
Block verify library	958.6	693.6	952.9	687.9
Set information library	476.5	211.5	475.5	210.5
EEPROM write library	2760.8	2168.8	2759.5	2167.5

Remarks 1. The above interrupt response times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

<2> When high-speed system clock is used (normal model of C compiler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	179/f_{CPU} + 507	179/f_{CPU} + 407	179/f_{CPU} + 1650	179/f_{CPU} + 714
Block erase library	179/f_{CPU} + 559	179/f_{CPU} + 460	179/f_{CPU} + 1702	179/f_{CPU} + 767
Word write library	333/f_{CPU} + 1589	333/f_{CPU} + 1298	333/f_{CPU} + 2732	333/f_{CPU} + 1605
Block verify library	179/f_{CPU} + 518	179/f_{CPU} + 418	179/f_{CPU} + 1661	179/f_{CPU} + 725
Set information library	80/f_{CPU} + 370	80/f_{CPU} + 165	80/f_{CPU} + 1513	80/f_{CPU} + 472
EEPROM write library[Note]	29/f_{CPU} + 1759 333/f_{CPU} + 834	29/f_{CPU} + 1468 333/f_{CPU} + 512	29/f_{CPU} + 1759 333/f_{CPU} + 2061	29/f_{CPU} + 1468 333/f_{CPU} + 873

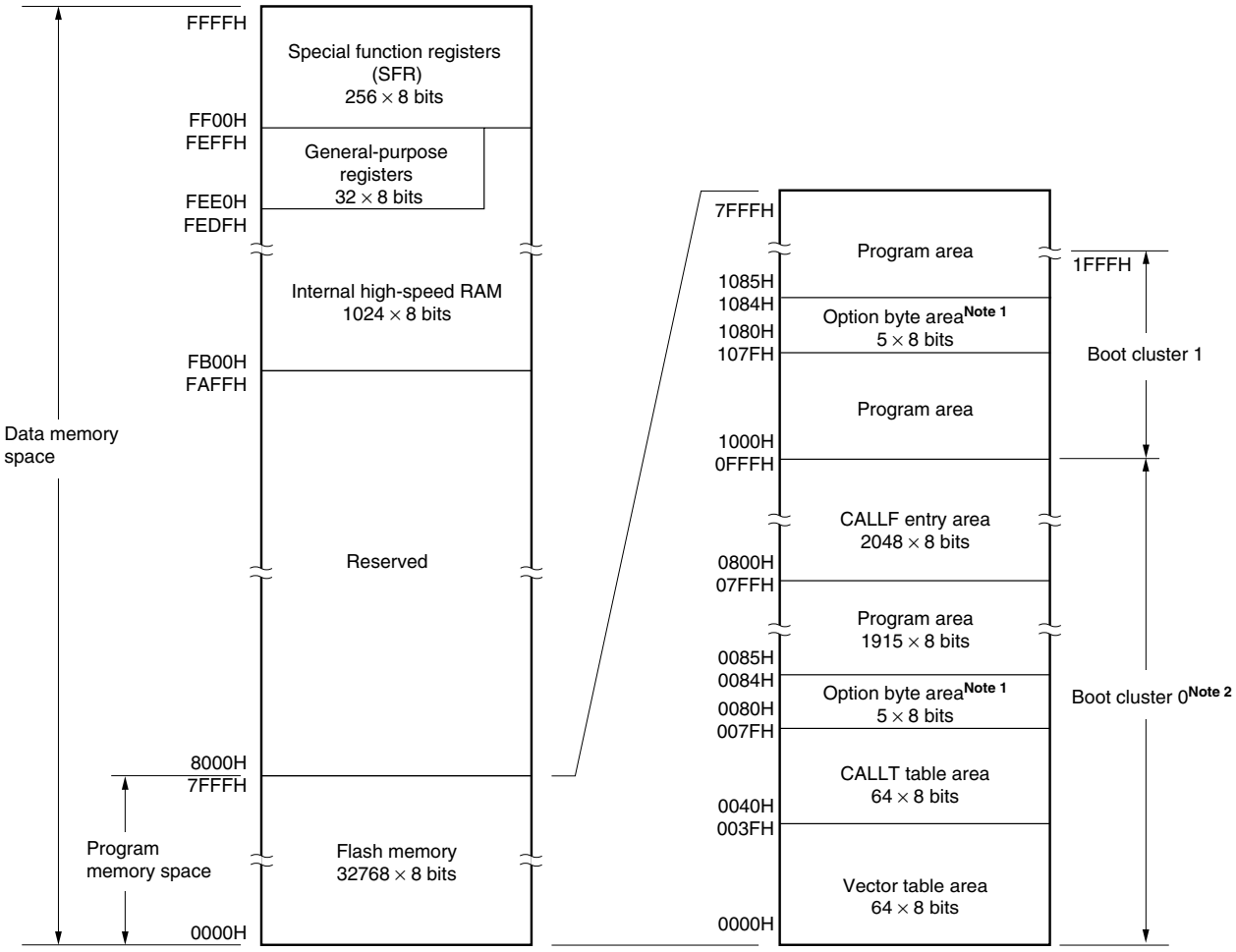
Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

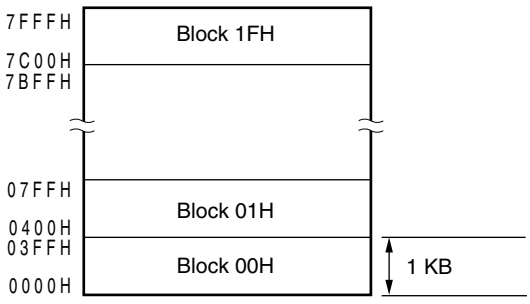
Figure 3-4. Memory Map (μPD78F0503, 78F0503A, 78F0513, 78F0513A, 78F0523, 78F0523A, 78F0533 and 78F0533A)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H.
When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.



5.2.4 Port 3

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P30/INTP1	√					
P31/INTP2/OCD1A[Note]	√					
P32/INTP3/OCD1B[Note]	√					
P33/INTP4/TI51/TO51	√					

Note OCD1A and OCD1B are provided to the products with an on-chip debug function (μPD78F05xxD and 78F05xxDA) only.

Remark √: Mounted

Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 to P33 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

This port can also be used for external interrupt request input and timer I/O.

Reset signal generation sets port 3 to input mode.

Figures 5-13 and 5-14 show block diagrams of port 3.

Cautions 1. In the product with an on-chip debug function (μP78F05xxD and D78F05xxDA), be sure to pull the P31/INTP2/OCD1A pin down before a reset release, to prevent malfunction.

2. Process the P31/INTP2/OCD1A pin of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P31/INTP2/OCD1A
Flash memory programmer connection		Connect to EV_{SS}[Note] via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset	
	During reset released	Input: Connect to EV_{DD}[Note] or EV_{SS}[Note] via a resistor. Output: Leave open.

Note With products without an EV_{SS} pin, connect them to V_{SS}. With products without an EV_{DD} pin, connect them to V_{DD}.

7.4.5 Free-running timer operation

When bits 3 and 2 (TMC0n3 and TMC0n2) of 16-bit timer mode control register 0n (TMC0n) are set to 01 (free-running timer mode), 16-bit timer/event counter 0n continues counting up in synchronization with the count clock. When it has counted up to FFFFH, the overflow flag (OVF0n) is set to 1 at the next clock, and TM0n is cleared (to 0000H) and continues counting. Clear OVF0n to 0 by executing the CLR instruction via software.

The following three types of free-running timer operations are available.

- Both CR00n and CR01n are used as compare registers.
- One of CR00n or CR01n is used as a compare register and the other is used as a capture register.
- Both CR00n and CR01n are used as capture registers.

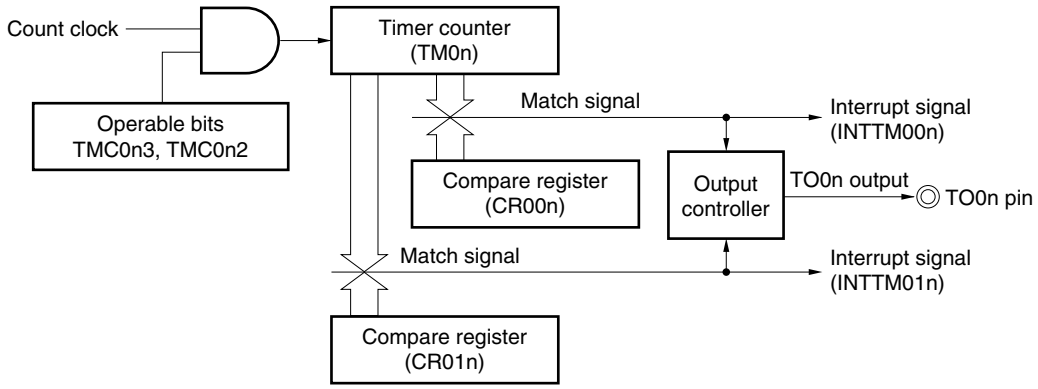
Remarks 1. For the setting of the I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

(1) Free-running timer mode operation

(CR00n: compare register, CR01n: compare register)

Figure 7-37. Block Diagram of Free-Running Timer Mode
(CR00n: Compare Register, CR01n: Compare Register)

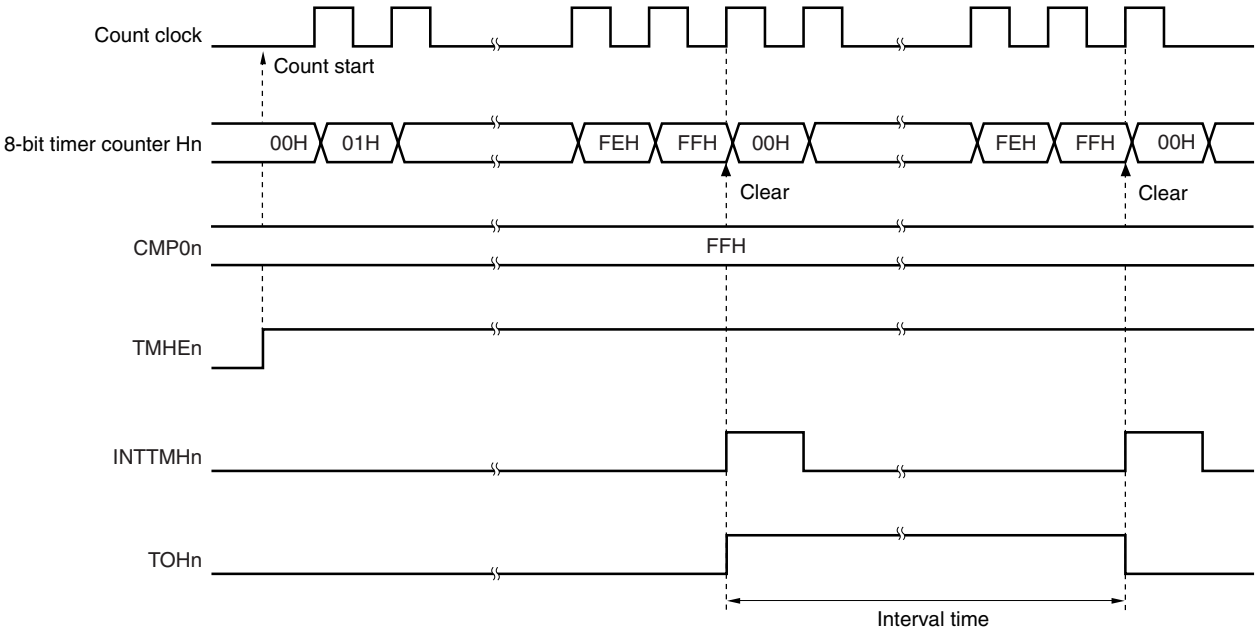


Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

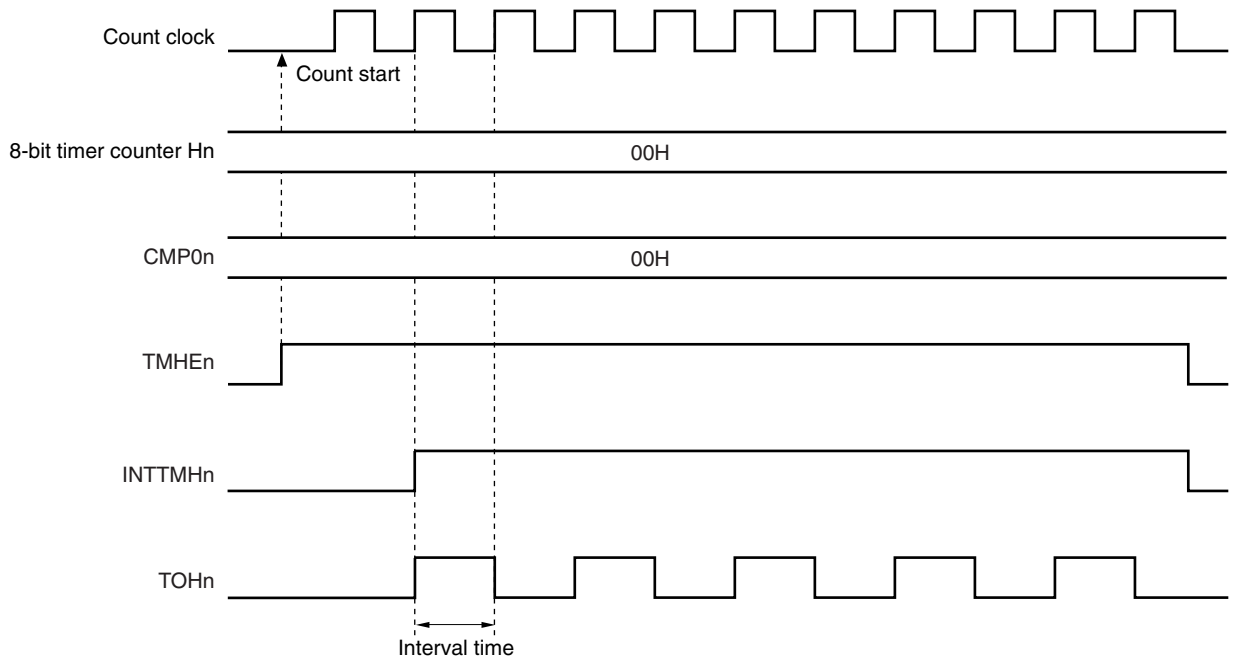
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 9-10. Timing of Interval Timer/Square-Wave Output Operation (2/2)

(b) Operation when CMP0n = FFH



(c) Operation when CMP0n = 00H



Remark n = 0, 1

11.4 Operation of Watchdog Timer

11.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (0080H).

   - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (0080H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 26**).

WDTON	Operation Control of Watchdog Timer Counter/Illegal Access Detection
0	Counter operation disabled (counting stopped after reset), illegal access detection operation disabled
1	Counter operation enabled (counting started after reset), illegal access detection operation enabled

   - Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (0080H) (for details, see **11.4.2** and **CHAPTER 26**).
   - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (0080H) (for details, see **11.4.3** and **CHAPTER 26**).

2. After a reset release, the watchdog timer starts counting.
3. By writing “ACH” to WDTE after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
4. After that, write WDTE the second time or later after a reset release during the window open period. If WDTE is written during a window close period, an internal reset signal is generated.
5. If the overflow time expires without “ACH” written to WDTE, an internal reset signal is generated.
   A internal reset signal is generated in the following cases.

   - If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
   - If data other than “ACH” is written to WDTE
   - If the instruction is fetched from an area not set by the IMS and IXS registers (detection of an invalid check during a CPU program loop)
   - If the CPU accesses an area not set by the IMS and IXS registers (excluding FB00H to FFCFH and FFE0H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

Cautions 1. The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.

2. If the watchdog timer is cleared by writing “ACH” to WDTE, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f_{RL} seconds.

3. The watchdog timer can be cleared immediately before the count value overflows (FFFFH).

Notes 2. Set the serial clock to satisfy the following conditions.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD) and Expanded-specification Products (μPD78F05xxA and 78F05xxDA)		
	Standard Products	(A) Grade Products	(A2) Grade Products
4.0 V ≤ V_{DD} ≤ 5.5 V	Serial clock ≤ 6.25 MHz	Serial clock ≤ 5 MHz	Serial clock ≤ 5 MHz
2.7 V ≤ V_{DD} < 4.0 V	Serial clock ≤ 4 MHz	Serial clock ≤ 2.5 MHz	Serial clock ≤ 2.5 MHz
1.8 V ≤ V_{DD} < 2.7 V	Serial clock ≤ 2 MHz	Serial clock ≤ 1.66 MHz	–

3. Do not start communication with the external clock from the $\overline{SCK11}$ pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. Do not write to CSIC11 while CSIE11 = 1 (operation enabled).

2. To use P02/SO11 and P04/$\overline{SCK11}$ as general-purpose ports, set CSIC11 in the default status (00H).

3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock frequency

(3) Port mode registers 0 and 1 (PM0, PM1)

These registers set port 0 and 1 input/output in 1-bit units.

When using P10/$\overline{SCK10}$ and P04/$\overline{SCK11}$ as the clock output pins of the serial interface, clear PM10 and PM04 to 0, and set the output latches of P10 and P04 to 1.

When using P12/SO10 and P02/SO11 as the data output pins of the serial interface, clear PM12, PM02, and the output latches of P12 and P02 to 0.

When using P10/$\overline{SCK10}$ and P04/$\overline{SCK11}$ as the clock input pins of the serial interface, P11/SI10/RxD0 and P03/SI11 as the data input pins, and P05/$\overline{SSI11}$/TI001 as the chip select input pin, set PM10, PM04, PM11, PM03, and PM05 to 1. At this time, the output latches of P10, P04, P11, P03, and P05 may be 0 or 1.

PM0 and PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 16-7. Format of Port Mode Register 0 (PM0)

Address: FF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

PM0n	P0n pin I/O mode selection (n = 0 to 6)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 0 of 78K0/KF2 products. For the format of port mode register 0 of other products, see **(1) Port mode registers (PMxx)** in **5.3 Registers Controlling Port Function**.

17.4.2 3-wire serial I/O mode

The one-byte data transmission/reception is executed in the mode in which bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) is cleared to 0.

The 3-wire serial I/O mode is useful for connecting peripheral ICs and display controllers with a clocked serial interface.

In this mode, communication is executed by using three lines: serial clock ($\overline{SCKA0}$), serial output (SOA0), and serial input (SIA0) lines.

(1) Registers used

- Serial operation mode specification register 0 (CSIMA0)[Note 1]
- Serial status register 0 (CSIS0)[Note 2]
- Divisor selection register 0 (BRGCA0)
- Port mode register 14 (PM14)
- Port register 14 (P14)

Notes 1. Bits 7, 6, and 4 to 1 (CSIAE0, ATE0, MASTER0, TXEA0, RXEA0, and DIR0) are used. Setting of bit 5 (ATM0) is invalid.

2. Only bit 0 (TSF0) and bit 6 (CKS00) are used.

The basic procedure of setting an operation in the 3-wire serial I/O mode is as follows.

<1> Set bit 6 (CKS00) of the CSIS0 register (see **Figure 17-3**)[Note 1].
<2> Set the BRGCA0 register (see **Figure 17-5**)[Note 1].
<3> Set bits 4 to 1 (MASTER0, TXEA0, RXEA0, and DIR0) of the CSIMA0 register (see **Figure 17-2**).
<4> Set bit 7 (CSIAE0) of the CSIMA0 register to 1 and clear bit 6 (ATE0) to 0.
<5> Write data to serial I/O shift register 0 (SIOA0). → Data transmission/reception is started[Note 2].

Notes 1. This register does not have to be set when the slave mode is specified (MASTER0 = 0).

2. Write dummy data to SIOA0 only for reception.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

17.4.3 3-wire serial I/O mode with automatic transmit/receive function

Up to 32 bytes of data can be transmitted/received without using software in the mode in which bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) is set to 1. After communication is started, only data of the set number of bytes stored in RAM in advance can be transmitted, and only data of the set number of bytes can be received and stored in RAM.

In addition, to transmit/receive data continuously when used as the master, handshake signals (STB0 and BUSY0) generated by hardware are supported. Therefore, connection to peripheral ICs such as OSD (On Screen Display) ICs and LCD controller/drivers can be easily realized.

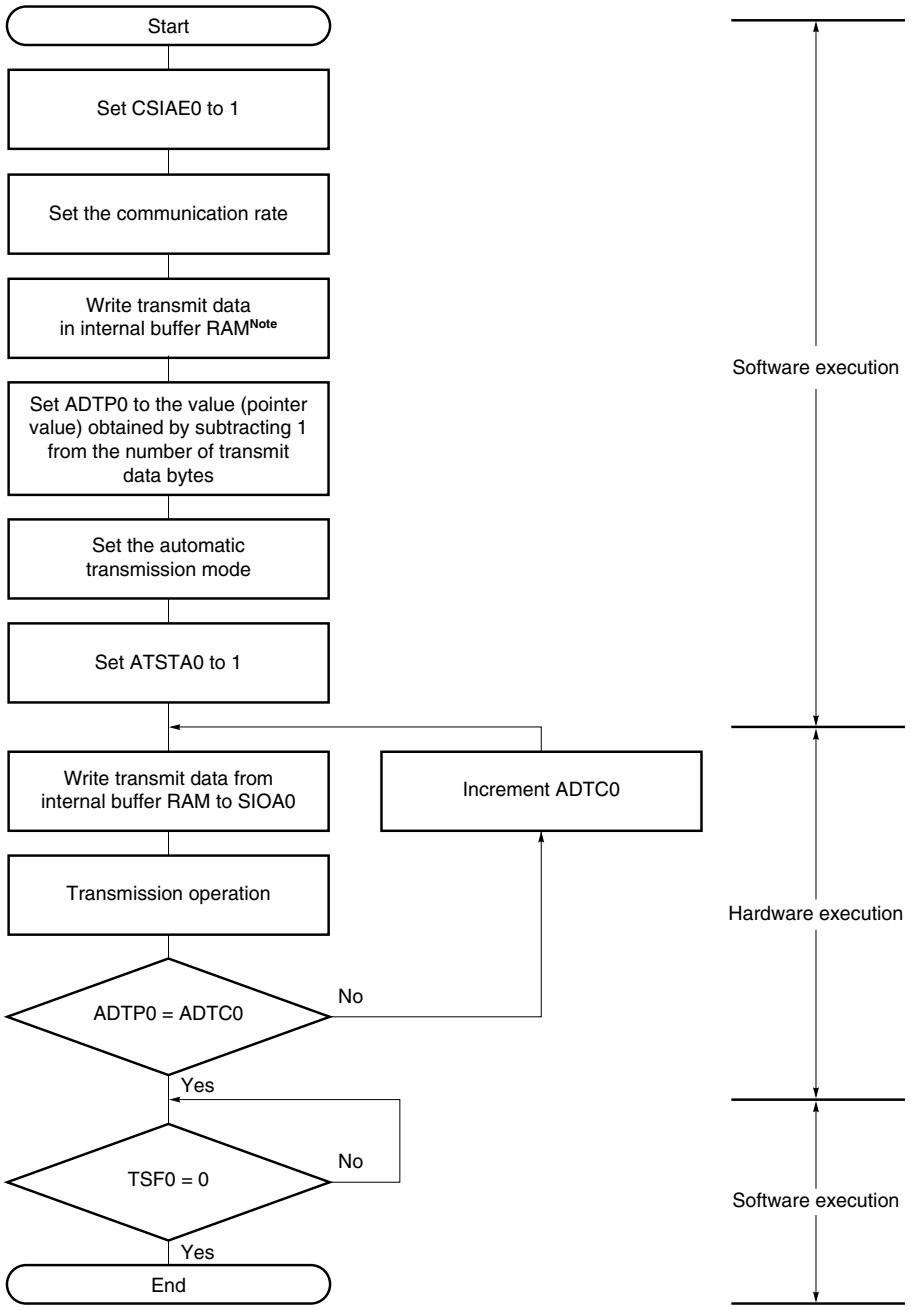
(1) Registers used

- Serial operation mode specification register 0 (CSIMA0)
- Serial status register 0 (CSIS0)
- Serial trigger register 0 (CSIT0)
- Divisor selection register 0 (BRGCA0)
- Automatic data transfer address point specification register 0 (ADTP0)
- Automatic data transfer interval specification register 0 (ADTI0)
- Port mode register 14 (PM14)
- Port register 14 (P14)

The relationship between the register settings and pins is shown below.

Caution A wait state may be generated when data is written to the buffer RAM. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

Figure 17-18. Automatic Transmission Mode Flowchart



CSIAE0: Bit 7 of serial operation mode specification register 0 (CSIMA0)
ADTP0: Automatic data transfer address point specification register 0
ADTI0: Automatic data transfer interval specification register 0
ATSTA0: Bit 0 of serial trigger register 0 (CSIT0)
SIOA0: Serial I/O shift register 0
ADTC0: Automatic data transfer address count register 0
TSF0: Bit 0 of serial status register 0 (CSIS0)

Note A wait state may be generated when data is written to the buffer RAM. For details, see **CHAPTER 36 CAUTIONS FOR WAIT**.

Table 18-7. Wait Periods

CL01	CL00	Wait Period
0	0	6 clocks
0	1	6 clocks
1	0	12 clocks
1	1	3 clocks

18.5.15 Cautions

(1) When STCEN (bit 1 of IIC flag register 0 (IICF0)) = 0

Immediately after I^2C operation is enabled (IICE0 = 1), the bus communication status (IICBSY flag (bit 6 of IICF0) = 1) is recognized regardless of the actual bus status. When changing from a mode in which no stop condition has been detected to a master device communication mode, first generate a stop condition to release the bus, then perform master device communication.

When using multiple masters, it is not possible to perform master device communication when the bus has not been released (when a stop condition has not been detected).

Use the following sequence for generating a stop condition.

<1> Set IIC clock selection register 0 (IICCL0).
<2> Set bit 7 (IICE0) of IIC control register 0 (IICC0) to 1.
<3> Set bit 0 (SPT0) of IICC0 to 1.

(2) When STCEN = 1

Immediately after I^2C operation is enabled (IICE0 = 1), the bus released status (IICBSY = 0) is recognized regardless of the actual bus status. To generate the first start condition (STT0 (bit 1 of IIC control register 0 (IICC0)) = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

(3) If other I^2C communications are already in progress

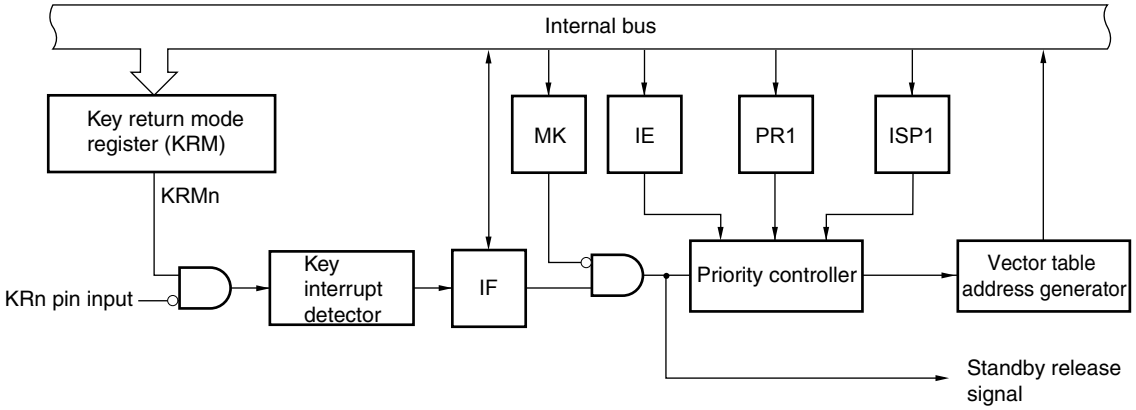
If I^2C operation is enabled and the device participates in communication already in progress when the SDA0 pin is low and the SCL0 pin is high, the macro of I^2C recognizes that the SDA0 pin has gone low (detects a start condition). If the value on the bus at this time can be recognized as an extension code, $\overline{ACK}$ is returned, but this interferes with other I^2C communications. To avoid this, start I^2C in the following sequence.

<1> Clear bit 4 (SPIE0) of IICC0 register to 0 to disable generation of an interrupt request signal (INTIIC0) when the stop condition is detected.
<2> Set bit 7 (IICE0) of IICC0 register to 1 to enable the operation of I^2C.
<3> Wait for detection of the start condition.
<4> Set bit 6 (LREL0) of IICC0 register to 1 before $\overline{ACK}$ is returned (4 to 80 clocks after setting IICE0 bit to 1), to forcibly disable detection.

(4) Determine the transfer clock frequency by using SMC0, CL01, CL00 bits (bits 3, 1, and 0 of IICL0 register), and CLX0 bit (bit 0 of IICX0 register) before enabling the operation (IICE0 = 1). To change the transfer clock frequency, clear IICE0 bit to 0 once.

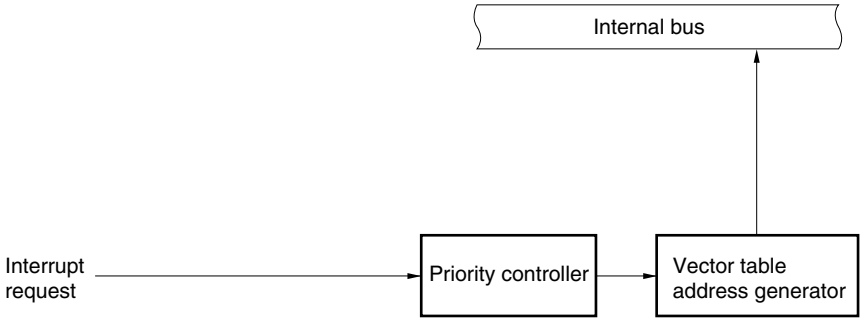
Figure 20-1. Basic Configuration of Interrupt Function (2/2)

<R> **(C) External maskable interrupt (INTKR)**



Remark n = 0, 1: 38-pin products of 78K0/KC2
n = 0 to 3: 44-pin and 48-pin products of 78K0/KC2
n = 0 to 7: 78K0/KD2, 78K0/KE2, 78K0/KF2

(D) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag
KRM: Key return mode register

Figure 20-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KB2)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	DUALIF0 CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	7	6	5	4	<3>	2	<1>	<0>
IF1L	0	0	0	0	TMIF51	0	SRIF0	ADIF

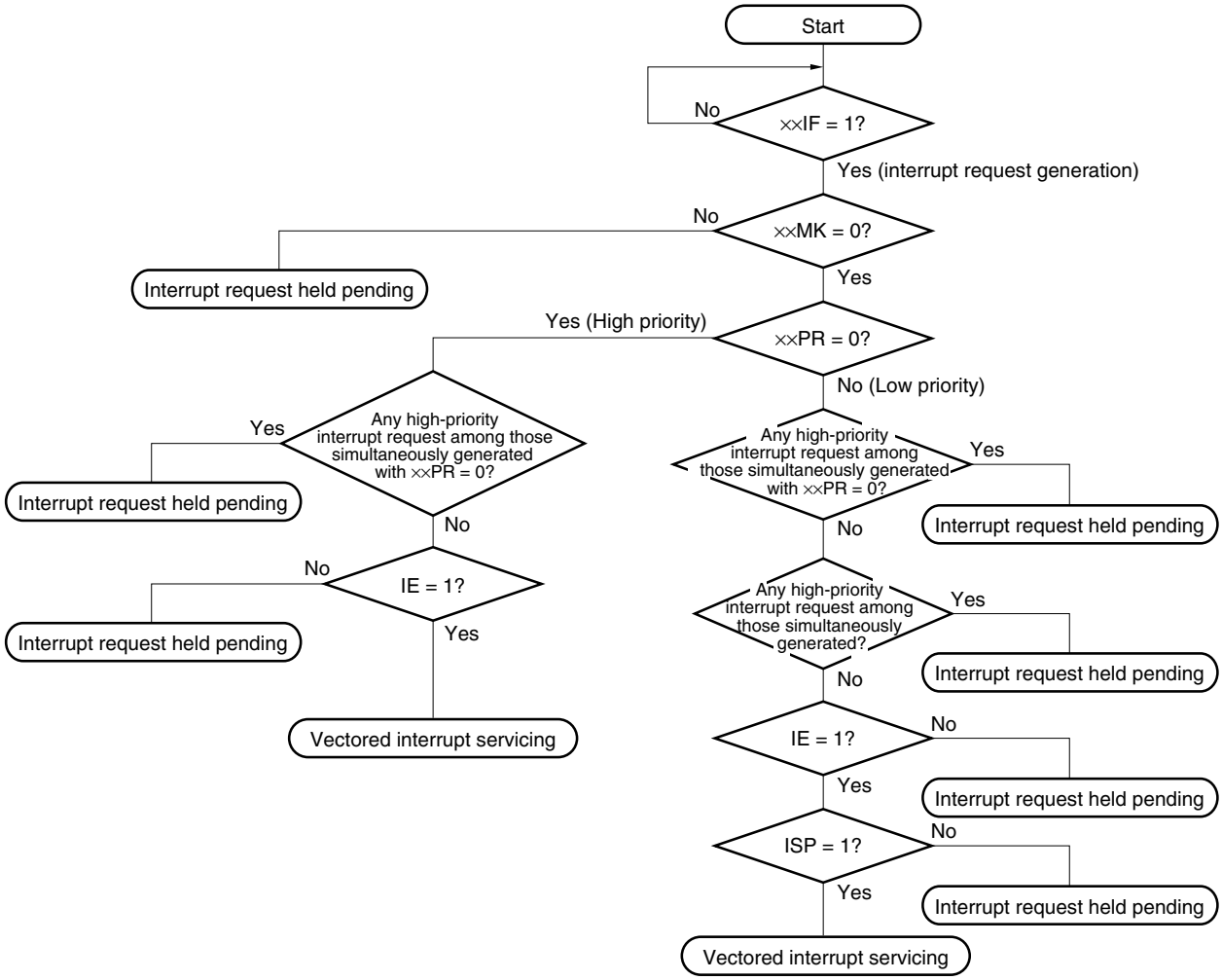
Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
IF1H	0	0	0	0	0	0	0	IICIF0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Caution Be sure to clear bits 2, 4 to 7 of IF1L and bits 1 to 7 of IF1H to 0.

Figure 20-19. Interrupt Request Acknowledgment Processing Algorithm



××IF: Interrupt request flag

××MK: Interrupt mask flag

××PR: Priority specification flag

IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)

ISP: Flag that indicates the priority level of the interrupt currently being serviced (0 = high-priority interrupt servicing, 1 = No interrupt request acknowledged, or low-priority interrupt servicing)

Cautions 3. When using LVI as an interrupt, if LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

4. With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.

(2) Low-voltage detection level selection register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 25-3. Format of Low-Voltage Detection Level Selection Register (LVIS)

Address: FFBFH After reset: 00H[Note 1] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.24 V ±0.1 V)
0	0	0	1	V_{LVI1} (4.09 V ±0.1 V)
0	0	1	0	V_{LVI2} (3.93 V ±0.1 V)
0	0	1	1	V_{LVI3} (3.78 V ±0.1 V)
0	1	0	0	V_{LVI4} (3.62 V ±0.1 V)
0	1	0	1	V_{LVI5} (3.47 V ±0.1 V)
0	1	1	0	V_{LVI6} (3.32 V ±0.1 V)
0	1	1	1	V_{LVI7} (3.16 V ±0.1 V)
1	0	0	0	V_{LVI8} (3.01 V ±0.1 V)
1	0	0	1	V_{LVI9} (2.85 V ±0.1 V)
1	0	1	0	V_{LVI10} (2.70 V ±0.1 V) [Note 2]
1	0	1	1	V_{LVI11} (2.55 V ±0.1 V) [Note 2]
1	1	0	0	V_{LVI12} (2.39 V ±0.1 V) [Note 2]
1	1	0	1	V_{LVI13} (2.24 V ±0.1 V) [Note 2]
1	1	1	0	V_{LVI14} (2.08 V ±0.1 V) [Note 2]
1	1	1	1	V_{LVI15} (1.93 V ±0.1 V) [Note 2]

Notes 1. The value of LVIS is not reset but retained as is, upon a reset by LVI. It is cleared to 00H upon other resets.

2. Do not set V_{LVI10} to V_{LVI15} for (A2) grade products.

Cautions 1. Be sure to clear bits 4 to 7 to "0".

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.

4. With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.

(3) Port mode register 12 (PM12)

When using the P120/EXLVI/INTP0 pin for external low-voltage detection potential input, set PM120 to 1. At this time, the output latch of P120 may be 0 or 1.

PM12 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM12 to FFH.

Figure 25-4. Format of Port Mode Register 12 (PM12)

Address: FF2CH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	PM124	PM123	PM122	PM121	PM120

PM12n	P12n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The format of port mode register 12 of 78K0/KB2 products is different from the above format. See **5.3 Registers Controlling Port Function (1) Port mode registers (PMxx)**.

25.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

(1) Used as reset (LVIMD = 1)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), generates an internal reset signal when $V_{DD} < V_{LVI}$, and releases internal reset when $V_{DD} \geq V_{LVI}$.
- If LVISEL = 1, compares the input voltage from external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V (TYP.)), generates an internal reset signal when EXLVI < V_{EXLVI}, and releases internal reset when EXLVI ≥ V_{EXLVI}.

(2) Used as interrupt (LVIMD = 0)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}). When V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$), generates an interrupt signal (INTLVI).
- If LVISEL = 1, compares the input voltage from external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V (TYP.)). When EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}), generates an interrupt signal (INTLVI).

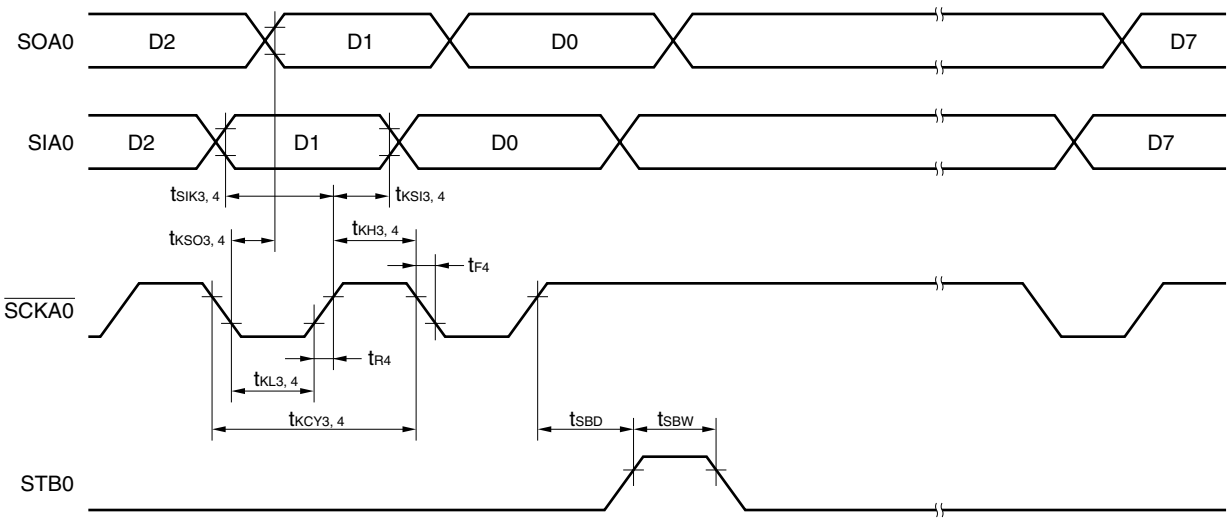
While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

Remark LVIMD: Bit 1 of low-voltage detection register (LVIM)
LVISEL: Bit 2 of LVIM

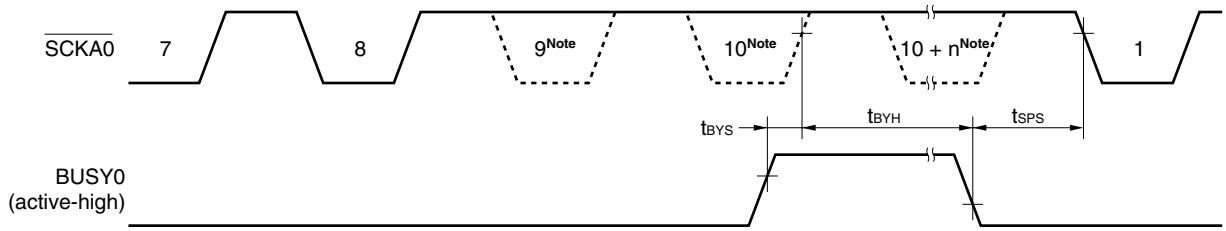
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Serial Transfer Timing (2/2)

CSIA0:



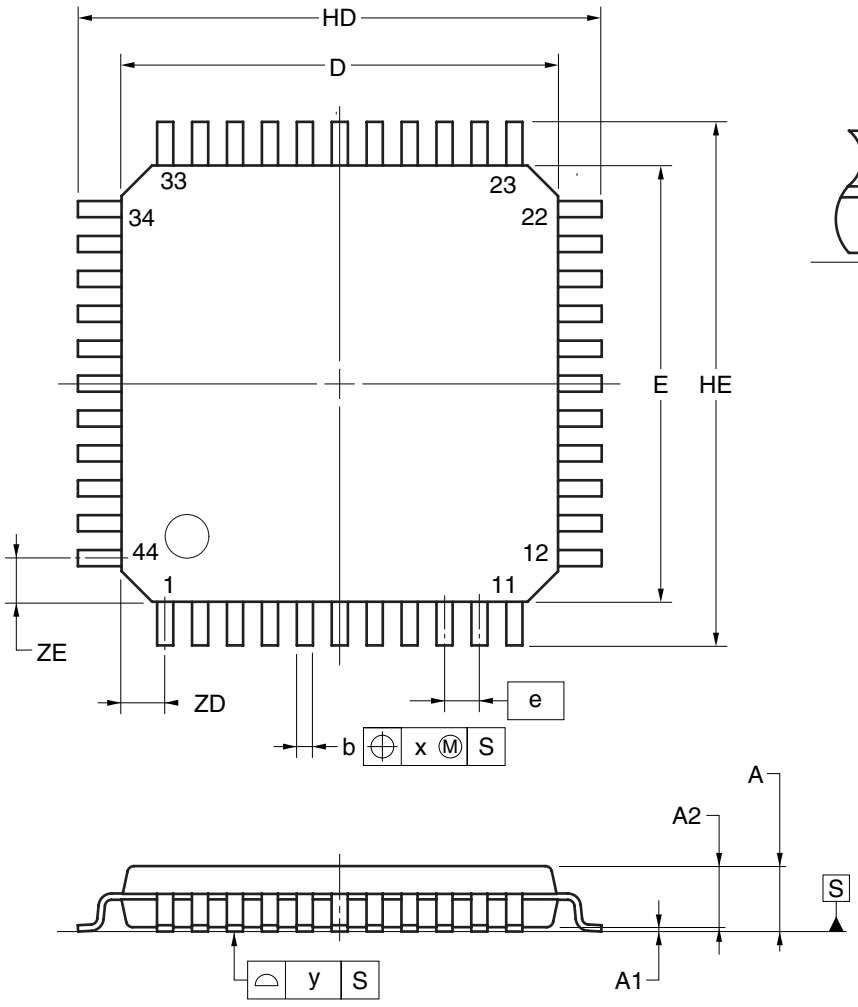
CSIA0 (busy processing):



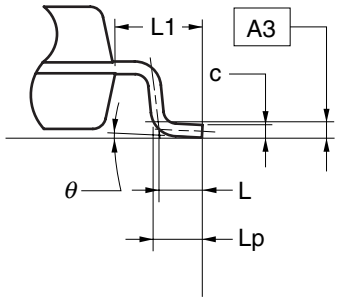
Note SCKA0 does not become low level here, but the timing is illustrated so that the timing specifications can be shown.

- μPD78F0511GB(A)-GAF-AX, 78F0512GB(A)-GAF-AX, 78F0513GB(A)-GAF-AX
- μPD78F0511GB(A2)-GAF-AX, 78F0512GB(A2)-GAF-AX, 78F0513GB(A2)-GAF-AX
- μPD78F0511AGB-GAF-AX, 78F0512AGB-GAF-AX, 78F0513AGB-GAF-AX, 78F0513DAGB-GAF-AX
- μPD78F0511AGBA-GAF-G, 78F0512AGBA-GAF-G, 78F0513AGBA-GAF-G
- μPD78F0511AGBA2-GAF-G, 78F0512AGBA2-GAF-G, 78F0513AGBA2-GAF-G

44-PIN PLASTIC LQFP (10x10)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.35^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

P44GB-80-GAF

NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

[MEMO]