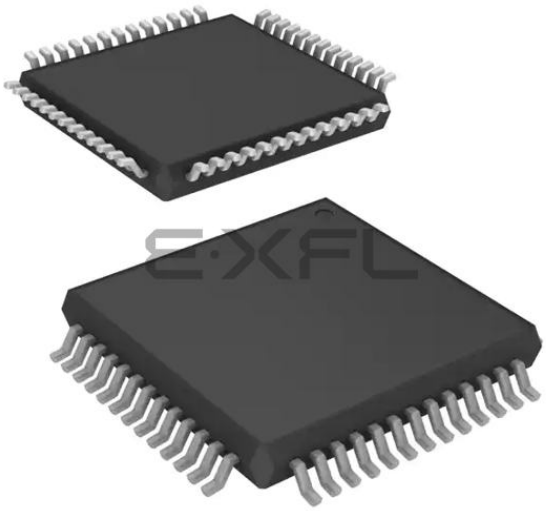
Renesas Electronics America Inc - UPD78F0526AGB-GAG-AX Datasheet



Welcome to E-XFL.COM

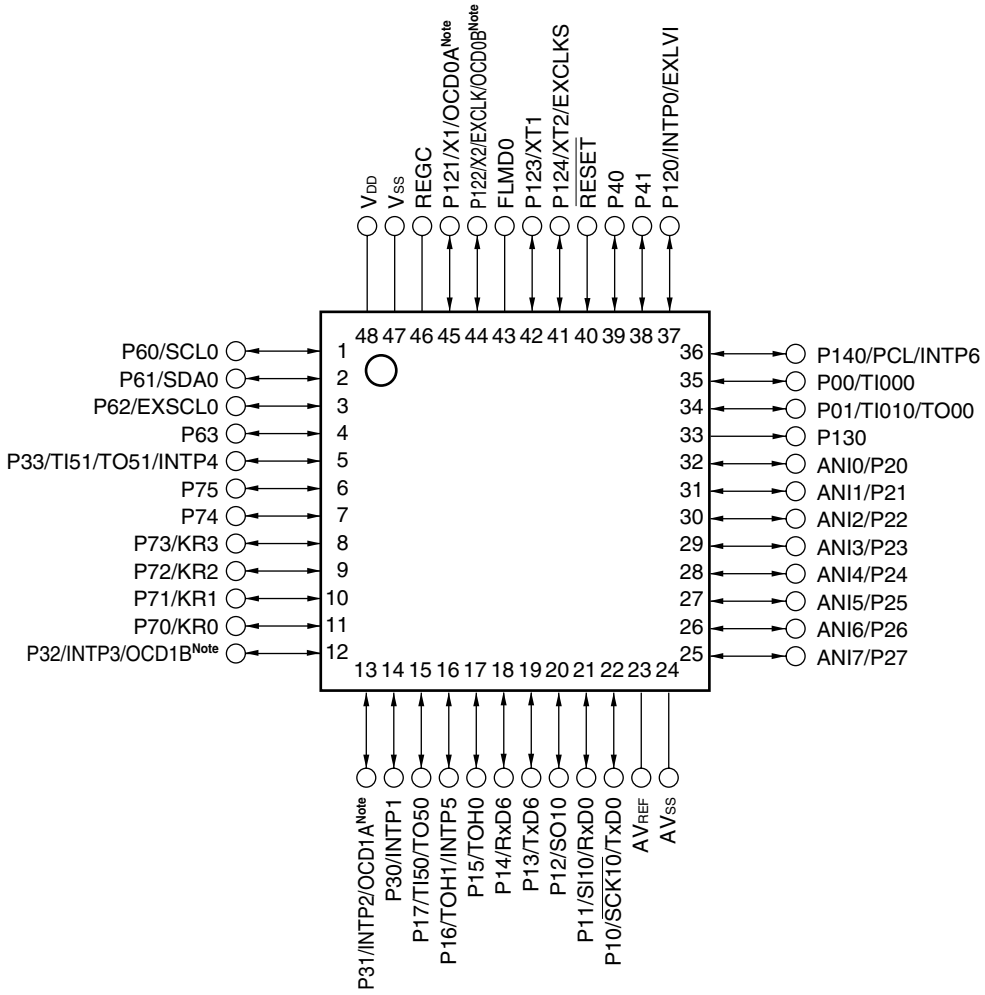
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0526agb-gag-ax

- 48-pin plastic LQFP (fine pitch) (7 × 7)



Note Products with on-chip debug function only

Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

3. ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

Remark For pin identification, see **1.6 Pin Identification**.

3.4.7 Based addressing

[Function]

8-bit immediate data is added as offset data to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored.

This addressing can be carried out for all of the memory spaces. However, before addressing a memory bank that is not set by the memory bank select register (BANK), change the setting of the memory bank by using BANK.

[Operand format]

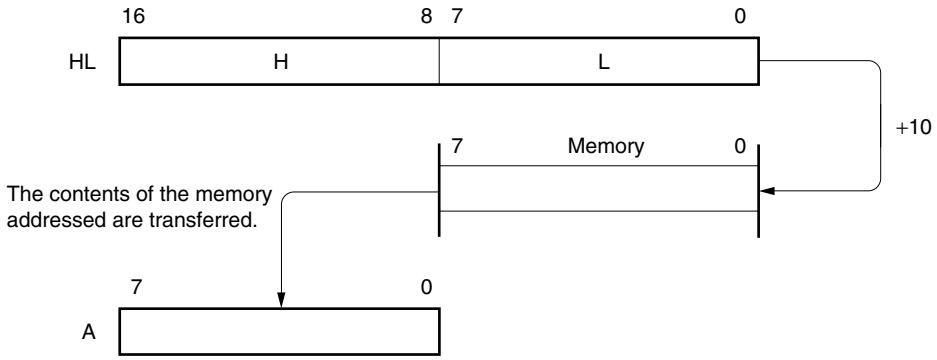
Identifier	Description
–	[HL + byte]

[Description example]

MOV A, [HL + 10H]; when setting byte to 10H

Operation code	1	0	1	0	1	1	1	0
	0	0	0	1	0	0	0	0

[Illustration]



(3) Example of setting procedure when stopping the internal high-speed oscillation clock

The internal high-speed oscillation clock can be stopped in the following two ways.

- Executing the STOP instruction to set the STOP mode
- Setting RSTOP to 1 and stopping the internal high-speed oscillation clock

(a) To execute a STOP instruction

<1> Setting of peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, see **CHAPTER 22 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed. To operate the CPU immediately after the STOP mode has been released, set MCM0 to 0, switch the CPU clock to the internal high-speed oscillation clock, and check that RSTS is 1.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and internal high-speed oscillation clock is stopped.

(b) To stop internal high-speed oscillation clock by setting RSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the internal high-speed oscillation clock.

When CLS = 0 and MCS = 0, the internal high-speed oscillation clock is supplied to the CPU, so change the CPU clock to a clock other than the internal high-speed oscillation clock.

- 78K0/KB2

MCS	CPU Clock Status
0	Internal high-speed oscillation clock
1	High-speed system clock

- 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the internal high-speed oscillation clock (RCM register)

When RSTOP is set to 1, internal high-speed oscillation clock is stopped.

Caution Be sure to confirm that MCS = 1 or CLS = 1 when setting RSTOP to 1. In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock.

Figure 7-18. Example of Register Settings for Interval Timer Operation

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	1	1	0	0

Clears and starts on match between TM0n and CR00n.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0	0	0

CR00n used as compare register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0	0	0	0

(d) Prescaler mode register 0n (PRM0n)

ES1n1	ES1n0	ES0n1	ES0n0	3	2	PRM0n1	PRM0n0
0	0	0	0	0	0	0/1	0/1

Selects count clock

(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

If M is set to CR00n, the interval time is as follows.

- Interval time = (M + 1) × Count clock cycle

Setting CR00n to 0000H is prohibited.

(g) 16-bit capture/compare register 01n (CR01n)

Usually, CR01n is not used for the interval timer function. However, a compare match interrupt (INTTM01n) is generated when the set value of CR01n matches the value of TM0n.

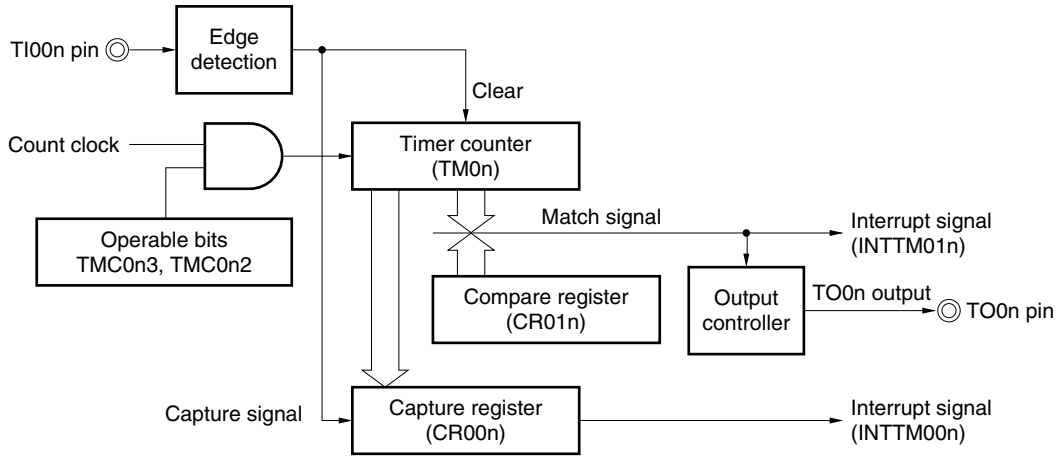
Therefore, mask the interrupt request by using the interrupt mask flag (TMMK01n).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(3) Operation in clear & start mode by entered TI00n pin valid edge input (CR00n: capture register, CR01n: compare register)

Figure 7-31. Block Diagram of Clear & Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register, CR01n: Compare Register)



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(2) Measuring the pulse width by using one input signal of the TI00n pin (free-running timer mode)

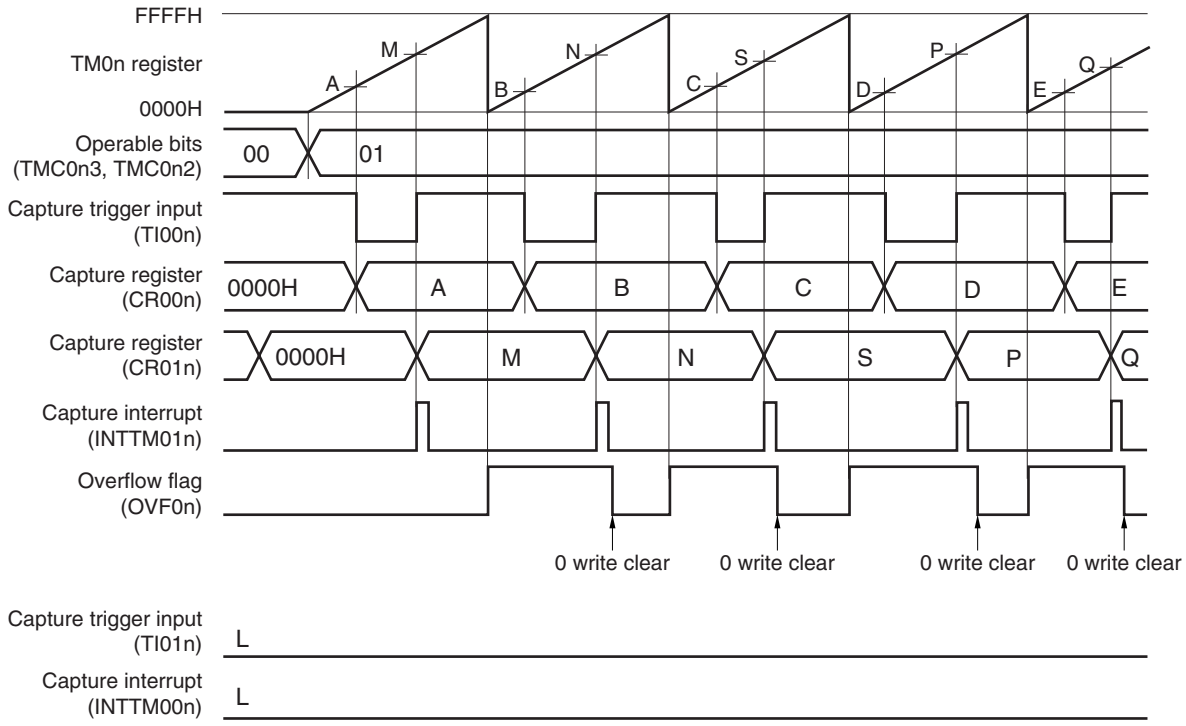
Set the free-running timer mode (TMC0n3 and TMC0n2 = 01). The count value of TM0n is captured to CR00n in the phase reverse to the valid edge detected on the TI00n pin. When the valid edge of the TI00n pin is detected, the count value of TM0n is captured to CR01n.

By this measurement method, values are stored in separate capture registers when a width from one edge to another is measured. Therefore, the capture values do not have to be saved. By subtracting the value of one capture register from that of another, a high-level width, low-level width, and cycle are calculated.

If an overflow occurs, the value becomes negative if one captured value is simply subtracted from another and, therefore, a borrow occurs (bit 0 (CY) of the program status word (PSW) is set to 1). If this happens, ignore CY and take the calculated value as the pulse width. In addition, clear bit 0 (OVF0n) of 16-bit timer mode control register 0n (TMC0n) to 0.

Figure 7-54. Timing Example of Pulse Width Measurement (2)

• TMC0n = 04H, PRM0n = 10H, CRC0n = 07H



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 10-2. Format of Watch Timer Operation Mode Register (WTM)

Address: FF6FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
WTM	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM7	Watch timer count clock selection (f_W)[Note]					
		f_{SUB} = 32.768 kHz	f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	$f_{PRS}/2^7$	–	15.625 kHz	39.062 kHz	78.125 kHz	156.25 kHz
1	f_{SUB}	32.768 kHz	–			

WTM6	WTM5	WTM4	Prescaler interval time selection
0	0	0	$2^4/f_W$
0	0	1	$2^5/f_W$
0	1	0	$2^6/f_W$
0	1	1	$2^7/f_W$
1	0	0	$2^8/f_W$
1	0	1	$2^9/f_W$
1	1	0	$2^{10}/f_W$
1	1	1	$2^{11}/f_W$

WTM3	WTM2	Selection of watch timer interrupt time
0	0	$2^{14}/f_W$
0	1	$2^{13}/f_W$
1	0	$2^5/f_W$
1	1	$2^4/f_W$

WTM1	5-bit counter operation control
0	Clear after operation stop
1	Start

WTM0	Watch timer operation enable
0	Operation stop (clear both prescaler and 5-bit counter)
1	Operation enable

Note The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when f_{PRS} = f_{XH} (XSEL = 1).)

Figure 14-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (2/2)

PS01	PS00	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL0	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL0	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE0) of asynchronous serial interface reception error status register 0 (ASIS0) is not set and the error interrupt does not occur.

Cautions 1. To start the transmission, set POWER0 to 1 and then set TXE0 to 1. To stop the transmission, clear TXE0 to 0, and then clear POWER0 to 0.

2. To start the reception, set POWER0 to 1 and then set RXE0 to 1. To stop the reception, clear RXE0 to 0, and then clear POWER0 to 0.

3. Set POWER0 to 1 and then set RXE0 to 1 while a high level is input to the RxD0 pin. If POWER0 is set to 1 and RXE0 is set to 1 while a low level is input, reception is started.

4. TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.

5. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

6. Clear the TXE0 and RXE0 bits to 0 before rewriting the PS01, PS00, and CL0 bits.

7. Make sure that TXE0 = 0 when rewriting the SL0 bit. Reception is always performed with “number of stop bits = 1”, and therefore, is not affected by the set value of the SL0 bit.

8. Be sure to set bit 0 to 1.

(1) Receive buffer register 6 (RXB6)

This 8-bit register stores parallel data converted by receive shift register 6 (RXS6).

Each time 1 byte of data has been received, new receive data is transferred to this register from RXS6. If the data length is set to 7 bits, data is transferred as follows.

- In LSB-first reception, the receive data is transferred to bits 0 to 6 of RXB6 and the MSB of RXB6 is always 0.
- In MSB-first reception, the receive data is transferred to bits 1 to 7 of RXB6 and the LSB of RXB6 is always 0.

If an overrun error (OVE6) occurs, the receive data is not transferred to RXB6.

RXB6 can be read by an 8-bit memory manipulation instruction. No data can be written to this register.

Reset signal generation sets this register to FFH.

(2) Receive shift register 6 (RXS6)

This register converts the serial data input to the RxD6 pin into parallel data.

RXS6 cannot be directly manipulated by a program.

(3) Transmit buffer register 6 (TXB6)

This buffer register is used to set transmit data. Transmission is started when data is written to TXB6.

This register can be read or written by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Cautions 1. Do not write data to TXB6 when bit 1 (TXBF6) of asynchronous serial interface transmission status register 6 (ASIF6) is 1.

2. Do not refresh (write the same value to) TXB6 by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) are 1 or when bits 7 and 5 (POWER6, RXE6) of ASIM6 are 1).

3. Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.

(4) Transmit shift register 6 (TXS6)

This register transmits the data transferred from TXB6 from the TxD6 pin as serial data. Data is transferred from TXB6 immediately after TXB6 is written for the first transmission, or immediately before INTST6 occurs after one frame was transmitted for continuous transmission. Data is transferred from TXB6 and transmitted from the TxD6 pin at the falling edge of the base clock.

TXS6 cannot be directly manipulated by a program.

Figure 22-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				fx = 10 MHz	fx = 20 MHz
0	0	1	2^{11}/fx	204.8 μs	102.4 μs
0	1	0	2^{13}/fx	819.2 μs	409.6 μs
0	1	1	2^{14}/fx	1.64 ms	819.2 μs
1	0	0	2^{15}/fx	3.27 ms	1.64 ms
1	0	1	2^{16}/fx	6.55 ms	3.27 ms
Other than above			Setting prohibited		

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

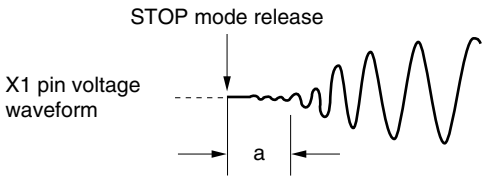
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

22.2 Standby Function Operation

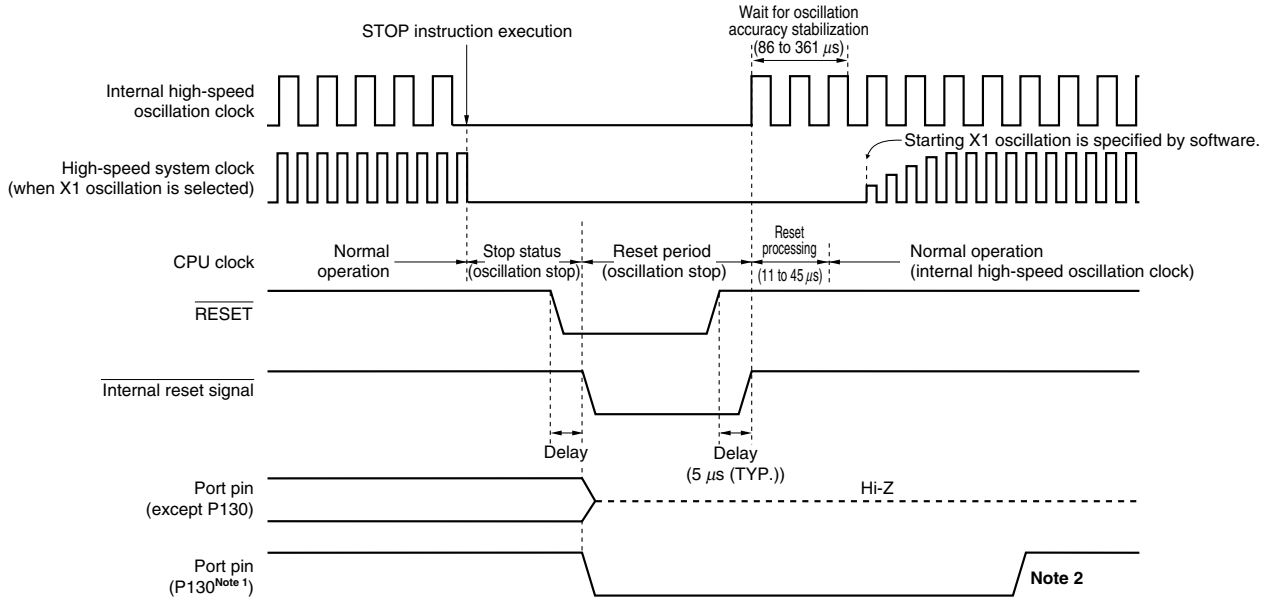
22.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, internal high-speed oscillation clock, or subsystem clock[Note]. The operating statuses in the HALT mode are shown below.

Note The 78K0/KB2 is not provided with a subsystem clock.

Figure 23-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input



Notes 1. P130 pin is not mounted onto 78K0/KB2, and 38-pin and 44-pin products of the 78K0/KC2.

2. Set P130 to high-level output by software.

Remarks 1. When reset is effected, P130 outputs a low level. If P130 is set to output a high level before reset is effected, the output signal of P130 can be dummy-output as the CPU reset signal.

2. For the reset timing of the power-on-clear circuit and low-voltage detector, see **CHAPTER 24 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 25 LOW-VOLTAGE DETECTOR**.

Table 27-14. Processing Time for Self Programming Library
(Expanded-specification Products (μPD78F05xxA and 78F05xxDA)) (1/3)

(1) When internal high-speed oscillation clock is used and entry RAM is located outside short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		4.0	4.5	4.0	4.5
Initialize library		1105.9	1106.6	1105.9	1106.6
Mode check library		905.7	906.1	904.9	905.3
Block blank check library		12776.1	12778.3	12770.9	12772.6
Block erase library		26050.4	349971.3	26045.3	349965.6
Word write library		1180.1 + 203 × w	1184.3 + 2241 × w	1172.9 + 203 × w	1176.3 + 2241 × w
Block verify library		25337.9	25340.2	25332.8	25334.5
Self programming end library		4.0	4.5	4.0	4.5
Get information library	Option value: 03H	1072.9	1075.2	1067.5	1069.1
	Option value: 04H	1060.2	1062.6	1054.8	1056.6
	Option value: 05H	1023.8	1028.2	1018.3	1022.1
Set information library		70265.9	759995.0	70264.9	759994.0
EEPROM write library		1316.8 + 347 × w	1320.9 + 2385 × w	1309.0 + 347 × w	1312.4 + 2385 × w

(2) When internal high-speed oscillation clock is used and entry RAM is located in short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		4.0	4.5	4.0	4.5
Initialize library		449.5	450.2	449.5	450.2
Mode check library		249.3	249.7	248.6	248.9
Block blank check library		12119.7	12121.9	12114.6	12116.3
Block erase library		25344.7	349266.4	25339.6	349260.8
Word write library		445.8 + 203 × w	449.9 + 2241 × w	438.5 + 203 × w	441.9 + 2241 × w
Block verify library		24682.7	24684.9	24677.6	24679.3
Self programming end library		4.0	4.5	4.0	4.5
Get information library	Option value: 03H	417.6	419.8	412.1	413.8
	Option value: 04H	405.0	407.4	399.5	401.3
	Option value: 05H	367.4	371.8	361.9	365.8
Set information library		69569.3	759297.3	69568.3	759296.2
EEPROM write library		795.1 + 347 × w	799.3 + 2385 × w	787.4 + 347 × w	790.8 + 2385 × w

Remarks 1. The above processing times are those when a write start address structure is located in the internal high-speed RAM and during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

3. w: Number of words in write data (1 word = 4 bytes)

(2) Non-port functions

Port		78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
		30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Power supply, ground		V_{DD}, EV_{DD}[Note 1], V_{SS}, EV_{SS}[Note 1], AV_{REF}, AV_{SS}	V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, V_{SS}, EV_{SS}, AV_{REF}, AV_{SS}	
Regulator		REGC						
Reset		$\overline{\text{RESET}}$						
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK, EXCLKS					
Writing to flash memory		FLMD0						
Interrupt		INTP0 to INTP5			INTP0 to INTP6		INTP0 to INTP7	
Key interrupt		–	KR0, KR1	KR0 to KR3		KR0 to KR7		
Timer	TM00	TI000, TI010, TO00						
	TM01	–					TI001[Note 2], TI011[Note 2], TO01[Note 2]	
	TM50	TI50, TO50						
	TM51	TI51, TO51						
	TMH0	TOH0						
	TMH1	TOH1						
Serial interface	UART0	RxD0, TxD0						
	UART6	RxD6, TxD6						
	IIC0	SCL0, SDA0	SCL0, SDA0, EXSCL0					
	CSI10	$\overline{\text{SCK10}}$, SI10, SO10						
	CSI11	–					$\overline{\text{SCK11}}$[Note 2], SI11[Note 2], SO11[Note 2], $\overline{\text{SSI11}}$[Note 2]	
	CSIA0	–						$\overline{\text{SCKA0}}$, SIA0, SOA0, BUSY0, STB0
A/D converter		ANI0 to ANI3	ANI0 to ANI5	ANI0 to ANI7				
Clock output		–			PCL			
Buzzer output		–					BUZ	
Low-voltage detector (LVI)		EXLVI						

Notes 1. This is not mounted onto 30-pin products.

2. This is not mounted onto the 78K0/KE2 products whose flash memory is less than 32 KB.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(1) Basic operation (2/2)

(T_A = –40 to +110°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
External subsystem clock frequency[Note 1]	f_{EXCLKS}		32	32.768	35	kHz
External subsystem clock input high-level width, low-level width[Note 1]	$t_{EXCLKSH}$, $t_{EXCLKSL}$		12			μs
TI000, TI010, TI001, TI011 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$ + 0.1[Note 2]			μs
		2.7 V ≤ V_{DD} < 4.0 V	$2/f_{sam}$ + 0.2[Note 2]			μs
TI50, TI51 input frequency	f_{TI5}				10	MHz
TI50, TI51 input high-level width, low-level width	t_{TIH5}, t_{TIL5}		50			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}		1			μs
Key interrupt input low-level width	t_{KR}		250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

Notes 1. The 78K0/KB2 is not provided with a subsystem clock.

2. Selection of f_{sam} = f_{PRS}, $f_{PRS}/4$, $f_{PRS}/256$, or f_{PRS}, $f_{PRS}/16$, $f_{PRS}/64$ is possible using bits 0 and 1 (PRM000, PRM001 or PRM010, PRM011) of prescaler mode registers 00 and 01 (PRM00, PRM01). Note that when selecting the TI000 or TI001 valid edge as the count clock, f_{sam} = f_{PRS}.

CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: T_A = –40 to +125°C)

Target Products	Conventional-specification Products	Expanded-specification Products
78K0/KB2	μPD78F0500(A2), 78F0501(A2), 78F0502(A2), 78F0503(A2)	μPD78F0500A(A2), 78F0501A(A2), 78F0502A(A2), 78F0503A(A2)
78K0/KC2	μPD78F0511(A2), 78F0512(A2), 78F0513(A2), 78F0514(A2), 78F0515(A2)	μPD78F0511A(A2), 78F0512A(A2), 78F0513A(A2), 78F0514A(A2), 78F0515A(A2)
78K0/KD2	μPD78F0521(A2), 78F0522(A2), 78F0523(A2), 78F0524(A2), 78F0525(A2), 78F0526(A2), 78F0527(A2)	μPD78F0521A(A2), 78F0522A(A2), 78F0523A(A2), 78F0524A(A2), 78F0525A(A2), 78F0526A(A2), 78F0527A(A2)
78K0/KE2	μPD78F0531(A2), 78F0532(A2), 78F0533(A2), 78F0534(A2), 78F0535(A2), 78F0536(A2), 78F0537(A2)	μPD78F0531A(A2), 78F0532A(A2), 78F0533A(A2), 78F0534A(A2), 78F0535A(A2), 78F0536A(A2), 78F0537A(A2)
78K0/KF2	μPD78F0544(A2), 78F0545(A2), 78F0546(A2), 78F0547(A2)	μPD78F0544A(A2), 78F0545A(A2), 78F0546A(A2), 78F0547A(A2)

The following items are described separately for conventional-specification products (μPD78F05xx(A2)) and expanded-specification products (μPD78F05xxA(A2)).

- X1 clock oscillation frequency (**X1 oscillator characteristics**)
- Instruction cycle, peripheral hardware clock frequency, external main system clock frequency, external main system clock input high-level width, and external main system clock input low-level width (**(1) Basic operation** in **AC characteristics**)
- A/D conversion time (**A/D Converter Characteristics**)
- Number of rewrites per chip (**Flash Memory Programming Characteristics**)

Caution The pins mounted depend on the product as follows.

(1) Port functions

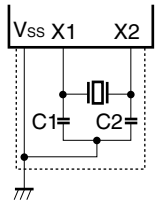
Port	78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
	30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Port 0	P00, P01				P00 to P03	P00 to P06	
Port 1	P10 to P17						
Port 2	P20 to P23	P20 to P25	P20 to P27				
Port 3	P30 to P33						
Port 4	–		P40, P41			P40 to P43	P40 to P47
Port 5	–					P50 to P53	P50 to P57
Port 6	P60, P61	P60 to P63					P60 to P67
Port 7	–	P70, P71	P70 to P73	P70 to P75	P70 to P77		
Port 12	P120 to P122	P120 to P124					
Port 13	–			P130			
Port 14	–			P140		P140, P141	P140 to P145

(The remaining table is on the next page.)

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

X1 Oscillator Characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
Ceramic resonator, Crystal resonator		X1 clock oscillation frequency (f_X)Note 1	Conventional-specification Products (μPD78F05xx (A2))	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0Note 2		20.0	MHz
				2.7 V ≤ V_{DD} < 4.0 V	1.0Note 2		10.0	
			Expanded-specification Products (μPD78F05xxA(A2))		1.0Note 2		20.0	MHz

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

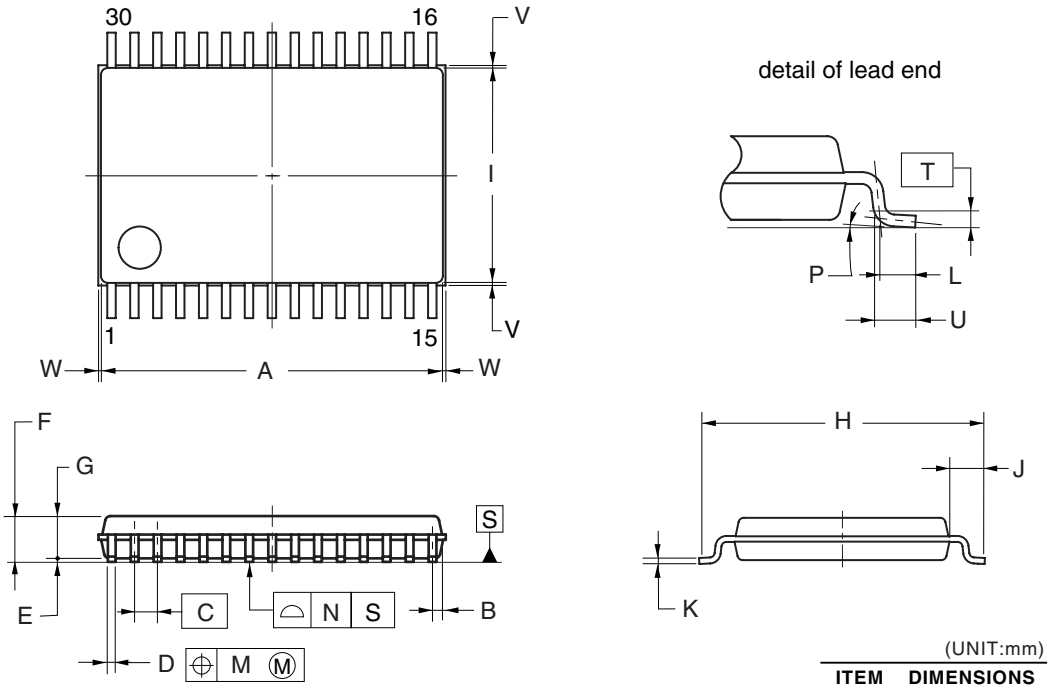
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

- μPD78F0500MC(A)-CAB-AX, 78F0501MC(A)-CAB-AX, 78F0502MC(A)-CAB-AX, 78F0503MC(A)-CAB-AX
- μPD78F0500MC(A2)-CAB-AX, 78F0501MC(A2)-CAB-AX, 78F0502MC(A2)-CAB-AX, 78F0503MC(A2)-CAB-AX
- μPD78F0500AMC-CAB-AX, 78F0501AMC-CAB-AX, 78F0502AMC-CAB-AX, 78F0503AMC-CAB-AX, 78F0503DAMC-CAB-AX
- μPD78F0500AMCA-CAB-G, 78F0501AMCA-CAB-G, 78F0502AMCA-CAB-G, 78F0503AMCA-CAB-G
- μPD78F0500AMCA2-CAB-G, 78F0501AMCA2-CAB-G, 78F0502AMCA2-CAB-G, 78F0503AMCA2-CAB-G

30-PIN PLASTIC SSOP (7.62mm (300))



(UNIT:mm)

ITEM	DIMENSIONS
A	9.70±0.10
B	0.30
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P30MC-65-CAB

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

(3/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 5	Soft	Port function	P121/X1/OCD0A, P122/X2/EXCLK/OCD0B, P123/XT1, P124/XT2/EXCLKS	When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK) or subsystem clock (EXCLKS), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see 6.3 (1) Clock operation mode select register (OSCCTL) and (3) Setting of operation mode for subsystem clock pin). The reset value of OSCCTL is 00H (all of the P121 to P124 pins are I/O port pins). At this time, setting of the PM121 to PM124 and P121 to P124 pins is not necessary.	p. 196 ☐
				Process the P121/X1/OCD0A pin of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator (see the table on p.197).	p. 197 ☐
			Port mode registers	Be sure to set bits 2 to 7 of PM0, bits 4 to 7 of PM2, bits 4 to 7 of PM3, bits 2 to 7 of PM6, bits 3 to 7 of PM12 to 1. (78K0/KB2)	p. 205 ☐
				For the 38-pin products, be sure to set bits 2 to 7 of PM0, bits 6 and 7 of PM2, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 4 to 7 of PM7, and bits 5 to 7 of PM12 to “1”. Also, be sure to set bits 0 and 1 of PM4, and bits 2 and 3 of PM7 to “0”. For the 44-pin products, be sure to set bits 2 to 7 of PM0, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 4 to 7 of PM7, and bits 5 to 7 of PM12 to “1”. For the 48-pin products, be sure to set bits 2 to 7 of PM0, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 6 and 7 of PM7, bits 5 to 7 of PM12, and bits 1 to 7 of PM14 to “1”. (78K0/KC2)	p. 206 ☐
				Be sure to set bits 4 to 7 of PM0, bits 4 to 7 of PM3, bits 2 to 7 of PM4, bits 4 to 7 of PM6, bits 5 to 7 of PM12, and bits 1 to 7 of PM14 to 1. (78K0/KD2)	p. 207 ☐
				Be sure to set bit 7 of PM0, bits 4 to 7 of PM3, bits 4 to 7 of PM4, bits 4 to 7 of PM5, bits 4 to 7 of PM6, bits 5 to 7 of PM12, and bits 2 to 7 of PM14 to “1”. (78K0/KE2)	p. 208 ☐
				Be sure to set bit 7 of PM0, bits 4 to 7 of PM3, bits 5 to 7 of PM12, and bits 6 and 7 of PM14 to “1”. (78K0/KF2)	p. 209 ☐
			Port register (78K0/KC2)	For the 38-pin products, be sure to set bits 6 and 7 of P2, bits 0 and 1 of P4, and bits 2 and 3 of P7 to “0”.	p. 211 ☐
			ADPC: A/D port configuration register	Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).	p. 220 ☐
				If data is written to ADPC, a wait cycle is generated. Do not write data to ADPC when the peripheral hardware clock is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.	p. 220 ☐
			1-bit manipulation instruction for port register n (Pn)	When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit. Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.	p. 224 ☐
Chapter 6	Soft	Clock generator	OSCCTL: Clock operation mode select register	Be sure to set AMPH to 1 if the high-speed system clock oscillation frequency exceeds 10 MHz.	pp. 230, 231 ☐
				Set AMPH before setting the main clock mode register (MCM).	pp. 230, 231 ☐

(8/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 7	Soft	16-bit timer/event counters 00, 01	PRM0n: Prescaler mode register 0n	Do not apply the following setting when setting the PRM0n1 and PRM0n0 bits to 11 (to specify the valid edge of the TI00n pin as a count clock). • Clear & start mode entered by the TI00n pin valid edge • Setting the TI00n pin as a capture trigger	p. 285 ☐
				If the operation of the 16-bit timer/event counter 0n is enabled when the TI00n or TI01n pin is at high level and when the valid edge of the TI00n or TI01n pin is specified to be the rising edge or both edges, the high level of the TI00n or TI01n pin is detected as a rising edge. Note this when the TI00n or TI01n pin is pulled up. However, the rising edge is not detected when the timer operation has been once stopped and then is enabled again.	p. 285 ☐
	Hard			The valid edge of TI010 and timer output (TO00) cannot be used for the P01 pin at the same time, and the valid edge of TI011 and timer output (TO01) cannot be used for the P06 pin at the same time. Select either of the functions.	p. 285 ☐
	Soft		Clear & start mode entered by TI00n pin valid edge input	Do not set the count clock as the valid edge of the TI00n pin (PRM0n1 and PRM0n0 = 11). When PRM0n1 and PRM0n0 = 11, TM0n may be cleared.	p. 299 ☐
			PPG output	To change the duty factor (value of CR01n) during operation, see 7.5.1 Rewriting CR01n during TM0n operation.	p. 321 ☐
				Set values to CR00n and CR01n such that the condition 0000H ≤ CR01n < CR00n ≤ FFFFH is satisfied.	p. 323 ☐
			One-shot pulse output	Do not input the trigger again (setting OSPT0n to 1 or detecting the valid edge of the TI00n pin) while the one-shot pulse is output. To output the one-shot pulse again, generate the trigger after the current one-shot pulse output has completed.	p. 325 ☐
				To use only the setting of OSPT0n to 1 as the trigger of one-shot pulse output, do not change the level of the TI00n pin or its alternate function port pin. Otherwise, the pulse will be unexpectedly output.	p. 325 ☐
				Do not set the same value to CR00n and CR01n.	p. 327 ☐
			LVS0n, LVRn0	Be sure to set LVS0n and LVR0n following steps <1>, <2>, and <3> above. Step <2> can be performed after <1> and before <3>.	p. 339 ☐
			–	Table 7-3 shows the restrictions for each channel.	p. 340 ☐
	Hard		Timer start errors	An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM0n is started asynchronously to the count pulse.	p. 340 ☐
	Soft		CR00n, CR01n: 16-bit timer capture/compare registers 00n, 01n	Set a value other than 0000H to CR00n and CR01n in clear & start mode entered upon a match between TM0n and CR00n (TM0n cannot count one pulse when it is used as an external event counter).	p. 340 ☐
				When the valid edge is input to the TI00n/TI01n pin and the reverse phase of the TI00n pin is detected while CR00n/CR01n is read, CR01n performs a capture operation but the read value of CR00n/CR01n is not guaranteed. At this time, an interrupt signal (INTTM00n/INTTM01n) is generated when the valid edge of the TI00n/TI01n pin is detected (the interrupt signal is not generated when the reverse-phase edge of the TI00n pin is detected). When the count value is captured because the valid edge of the TI00n/TI01n pin was detected, read the value of CR00n/CR01n after INTTM00n/INTTM01n is generated.	p. 341 ☐
				The values of CR00n and CR01n are not guaranteed after 16-bit timer/event counter 0n stops.	p. 341 ☐

(2/4)

Edition	Description	Chapter
3nd Edition	Modification of **Note 1** in and addition of **Note 4** to **Figure 8-5 Format of Timer Clock Selection Register 50 (TCL50)** and **Figure 8-6 Format of Timer Clock Selection Register 51 (TCL51)**	**CHAPTER 8 8-BIT TIMER/EVENT COUNTERS 50 AND 51**
	Modification of **Note 1** in and addition of **Note 3** to **Figure 9-5 Format of 8-Bit Timer H Mode Register 0 (TMHMD0)** and **Figure 9-6 Format of 8-Bit Timer H Mode Register 1 (TMHMD1)**	**CHAPTER 9 8-BIT TIMERS H0 AND H1**
	Addition of **Note** to **Figure 10-2 Format of Watch Timer Operation Mode Register (WTM)**	**CHAPTER 10 WATCH TIMER**
	Modification of **Note** and description in **11.1 Functions of Watchdog Timer**	**CHAPTER 11 WATCHDOG TIMER**
	Modification of **Note** and description in **11.4.1 Controlling operation of watchdog timer**	
	Modification of **Remark** in 11.4.3 Setting window open period of watchdog timer	
	Modification of **Note 1** in **Figure 12-3 Format of Clock Output Selection Register (CKS) (78K0/KD2, 48-pin Products of 78K0/KC2)** and **Figure 12-4 Format of Clock Output Selection Register (CKS) (78K0/KE2, 78K0/KF2)**	**CHAPTER 12 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER**
	Addition of **Table 13-2 A/D Conversion Time Selection (Conventional-specification Products (μPD78F05xx and 78F05xxD))**	**CHAPTER 13 A/D CONVERTER**
	Modification of **Table 13-3 A/D Conversion Time Selection (Expanded-specification Products (μPD78F05xxA and 78F05xxDA))**	
	Modification of **Figure 13-6 Format of 10-Bit A/D Conversion Result Register (ADCR)**	
	Modification of **Note 1** in **Figure 14-4 Format of Baud Rate Generator Control Register 0 (BRGC0)**	**CHAPTER 14 SERIAL INTERFACE UART0**
	Modification of **Note 1** in **Table 14-4 Set Value of TPS01 and TPS00**	
	Modification of **Table 14-5 Set Data of Baud Rate Generator**	
	Modification of **Note 1** in **Figure 15-5 Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (1/2)**	**CHAPTER 15 SERIAL INTERFACE UART6**
	Modification of **Note 1** in and addition of **Note 3** to **Figure 15-8 Format of Clock Selection Register 6 (CKSR6)**	
	Addition of **Caution 8** to **Figure 15-10 Format of Asynchronous Serial Interface Control Register 6 (ASICL6) (2/2)**	
	Modification of **Note 1** in **15.4.1 (1) Register used**	
	Modification of **Note 1** in and addition of **Note 3** to **Table 15-4 Set Value of TPS63 to TPS60**	
	Modification of **Notes 1** and **2** in **Figure 16-5 Format of Serial Clock Selection Register 10 (CSIC10)** and **Figure 16-6 Format of Serial Clock Selection Register 11 (CSIC11)**	**CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11**
	Addition of **Note 2** in and modification of **Table 16-2 Relationship Between Register Settings and Pins**	
	Modification of **16.4.2 (5) SO1n output**	