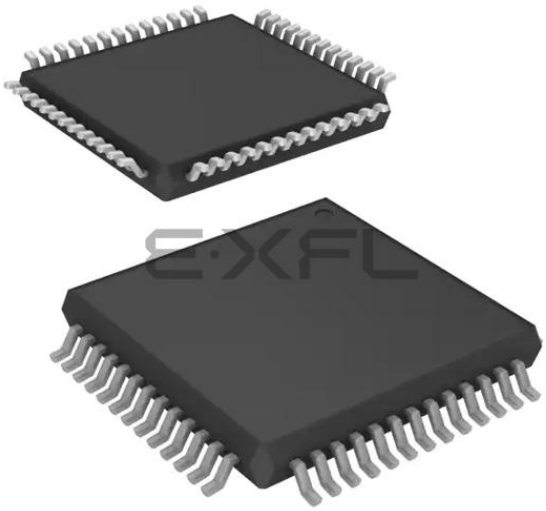
Renesas Electronics America Inc - UPD78F0527AGB-GAG-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0527agb-gag-ax

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
78K0/Kx2 User's Manual	This manual
78K/0 Series Instructions User's Manual	U12326E
78K0/Kx2 Flash Memory Programming (Programmer) Application Note	U17739E
78K0/Kx2 Flash Memory Self Programming User's Manual	U17516E
78K0/Kx2 EEPROM™ Emulation Application Note	U17517E
78K0 Microcontrollers Self Programming Library Type01 User's Manual	U18274E
78K0 Microcontrollers EEPROM Emulation Library Type01 User's Manual	U18275E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	U18865E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Documents Related to Development Tools (Hardware)

Document Name	Document No.
QB-78K0KX2 In-Circuit Emulator User's Manual	U17341E
QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual	U18371E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

(2) Expanded-specification products (μPD78F05xxA and 78F05xxDA) (1/2)

<1> When internal high-speed oscillation clock is used

Library Name	Interrupt Response Time (μs (Max.))			
	Normal Model of C Compiler		Static Model of C Compiler/Assembler	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	1100.9	431.9	1095.3	426.3
Block erase library	1452.9	783.9	1447.3	778.3
Word write library	1247.2	579.2	1239.2	571.2
Block verify library	1125.9	455.9	1120.3	450.3
Set information library	906.9	312.0	905.8	311.0
EEPROM write library	1215.2	547.2	1213.9	545.9

Remarks 1. The above interrupt response times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

<2> When high-speed system clock is used (normal model of C compiler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	179/f_{CPU} + 567	179/f_{CPU} + 246	179/f_{CPU} + 1708	179/f_{CPU} + 569
Block erase library	179/f_{CPU} + 780	179/f_{CPU} + 459	179/f_{CPU} + 1921	179/f_{CPU} + 782
Word write library	333/f_{CPU} + 763	333/f_{CPU} + 443	333/f_{CPU} + 1871	333/f_{CPU} + 767
Block verify library	179/f_{CPU} + 580	179/f_{CPU} + 259	179/f_{CPU} + 1721	179/f_{CPU} + 582
Set information library	80/f_{CPU} + 456	80/f_{CPU} + 200	80/f_{CPU} + 1598	80/f_{CPU} + 459
EEPROM write library[Note]	29/f_{CPU} + 767 333/f_{CPU} + 696	29/f_{CPU} + 447 333/f_{CPU} + 376	29/f_{CPU} + 767 333/f_{CPU} + 1838	29/f_{CPU} + 447 333/f_{CPU} + 700

Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

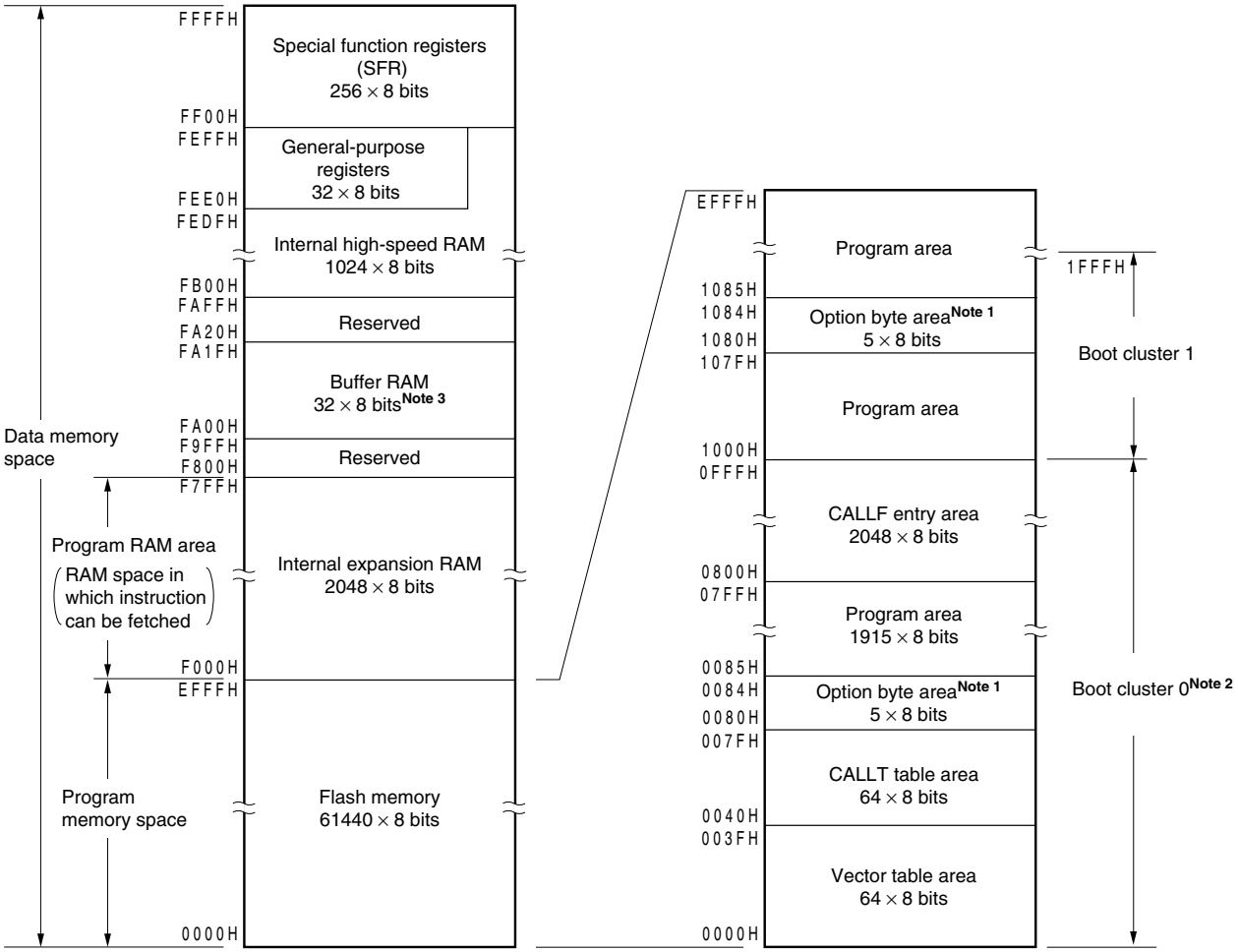
3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

(2) Non-port functions (1/2): 78K0/KB2

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI3	Input	A/D converter analog input	Analog input	P20 to P23
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
FLMD0	–	Flash memory programming mode setting	–	–
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P30
INTP2				P31/OCD1A[Note]
INTP3				P32/OCD1B[Note]
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
REGC	–	Connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI10
RxD6	Input	Serial data input to UART6	Input port	P14
TxD0	Output	Serial data output from UART0	Input port	P10/$\overline{\text{SCK10}}$
TxD6	Output	Serial data output from UART6	Input port	P13
$\overline{\text{SCK10}}$	I/O	Clock input/output for CSI10	Input port	P10/TxD0
SI10	Input	Serial data input to CSI10		P11/RxD0
SO10	Output	Serial data output from CSI10		P12
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SDA0		Serial data I/O for I^2C		P61
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00
TI010	Input	Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00	Input port	P01/TO00
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TI010
TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50
TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
TOH0	Output	8-bit timer H0 output	Input port	P15
TOH1		8-bit timer H1 output		P16/INTP5
X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A[Note]
X2	–		Input port	P122/EXCLK/OCD0B[Note]
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B[Note]

Note μPD78F0503D and 78F0503DA (product with on-chip debug function) only

Figure 3-7. Memory Map (μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, 78F0535A, 78F0545, and 78F0545A)

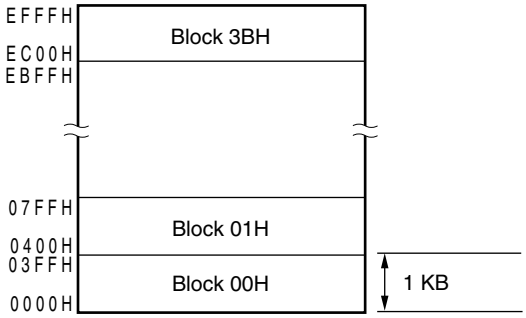


Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H.
When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

3. The buffer RAM is incorporated only in the μPD78F0545 and 78F0545A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, and 78F0535A.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.



3.2.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FEE0H to FEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

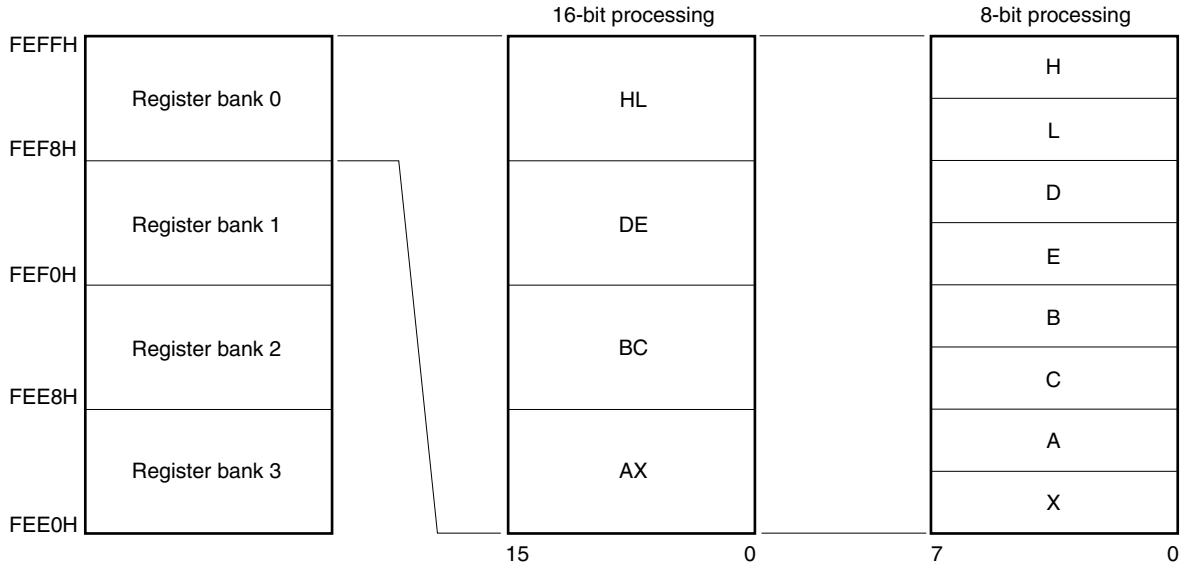
Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

These registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupts for each bank.

Figure 3-25. Configuration of General-Purpose Registers

(a) Function name



(b) Absolute name

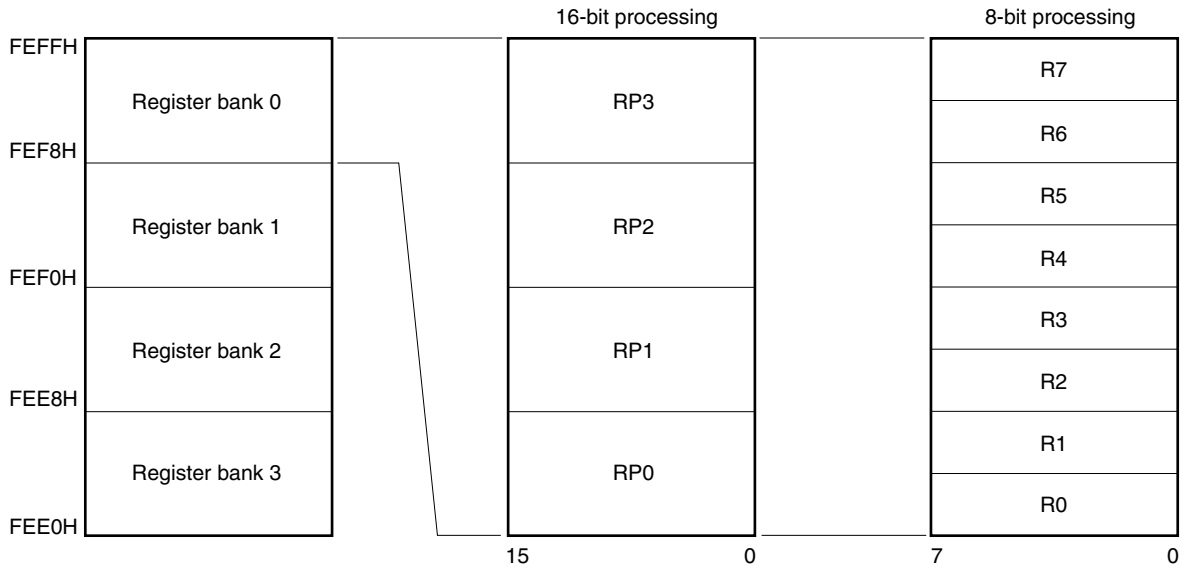
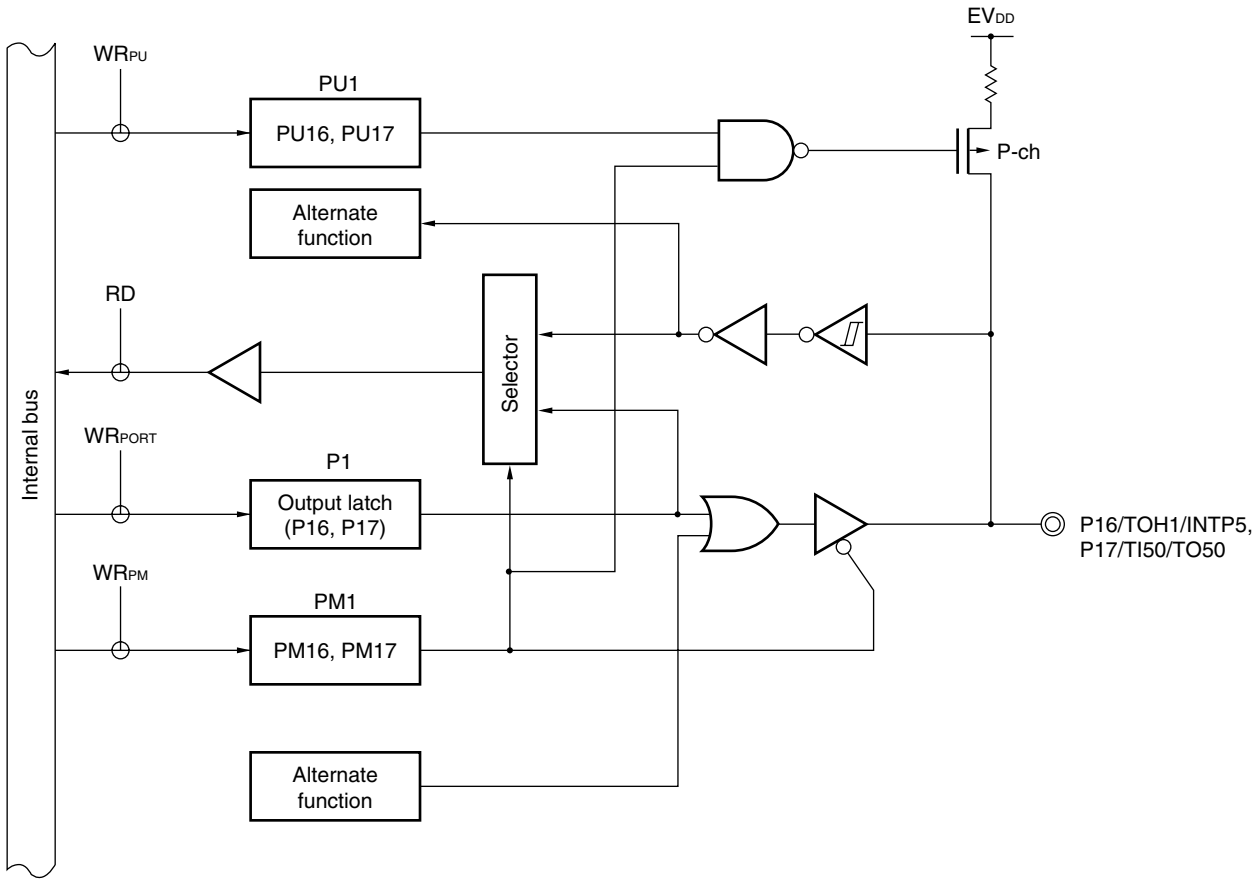


Figure 5-11. Block Diagram of P16 and P17



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

6.6.10 Peripheral hardware and source clocks

The following lists peripheral hardware and source clocks incorporated in the 78K0/Kx2 microcontrollers.

Remark The peripheral hardware depends on the product. See **1.7 Block Diagram** and **1.8 Outline of Functions**.

Table 6-13. Peripheral Hardware and Source Clocks

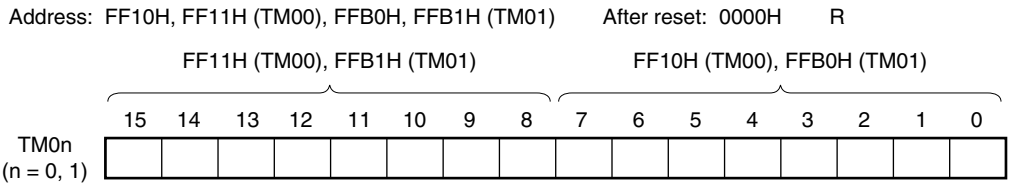
Peripheral Hardware \ Source Clock		Peripheral Hardware Clock (f_{PRS})	Subsystem Clock (f_{SUB})[Note 1]	Internal Low-Speed Oscillation Clock (f_{RL})	TM50 Output	External Clock from Peripheral Hardware Pins
16-bit timer/ event counter	00	Y	N	N	N	Y (TI000 pin)[Note 2]
	01	Y	N	N	N	Y (TI001 pin)[Note 2]
8-bit timer/ event counter	50	Y	N	N	N	Y (TI50 pin)[Note 2]
	51	Y	N	N	N	Y (TI51 pin)[Note 2]
8-Bit timer	H0	Y	N	N	Y	N
	H1	Y	N	Y	N	N
Watch timer		Y	Y	N	N	N
Watchdog timer		N	N	Y	N	N
Buzzer output		Y	N	N	N	N
Clock output		Y	Y	N	N	N
A/D converter		Y	N	N	N	N
Serial interface	UART0	Y	N	N	Y	N
	UART6	Y	N	N	Y	N
	CSI10	Y	N	N	N	Y ($\overline{SCK10}$ pin)[Note 2]
	CSI11	Y	N	N	N	Y ($\overline{SCK11}$ pin)[Note 2]
	CSIA0	Y	N	N	N	Y ($\overline{SCKA0}$ pin)[Note 2]
	IIC0	Y	N	N	N	Y (EXSCL0, SCL0 pin)[Note 2]

Notes 1. The 78K0/KB2 is not provided with a subsystem clock.

2. Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Remark Y: Can be selected, N: Cannot be selected

Figure 7-3. Format of 16-Bit Timer Counter 0n (TM0n)



The count value of TM0n can be read by reading TM0n when the value of bits 3 and 2 (TMC0n3 and TMC0n2) of 16-bit timer mode control register 0n (TMC0n) is other than 00. The value of TM0n is 0000H if it is read when TMC0n3 and TMC0n2 = 00.

The count value is reset to 0000H in the following cases.

- At reset signal generation
- If TMC0n3 and TMC0n2 are cleared to 00
- If the valid edge of the TI00n pin is input in the mode in which the clear & start occurs when inputting the valid edge to the TI00n pin
- If TM0n and CR00n match in the mode in which the clear & start occurs when TM0n and CR00n match
- OSPT0n is set to 1 in one-shot pulse output mode or the valid edge is input to the TI00n pin

Caution Even if TM0n is read, the value is not captured by CR01n.

(2) 16-bit timer capture/compare register 00n (CR00n), 16-bit timer capture/compare register 01n (CR01n)

CR00n and CR01n are 16-bit registers that are used with a capture function or comparison function selected by using CRC0n.

Change the value of CR00n while the timer is stopped (TMC0n3 and TMC0n2 = 00).

The value of CR01n can be changed during operation if the value has been set in a specific way. For details, see **7.5.1 Rewriting CR01n during TM0n operation**.

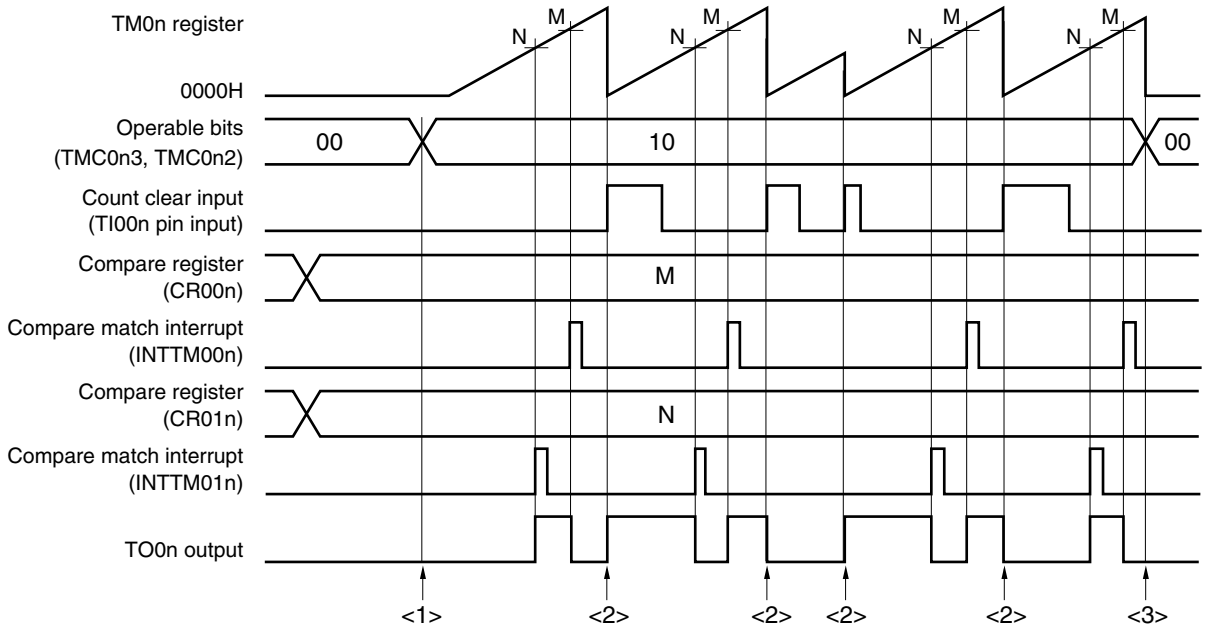
These registers can be read or written in 16-bit units.

Reset signal generation clears these registers to 0000H.

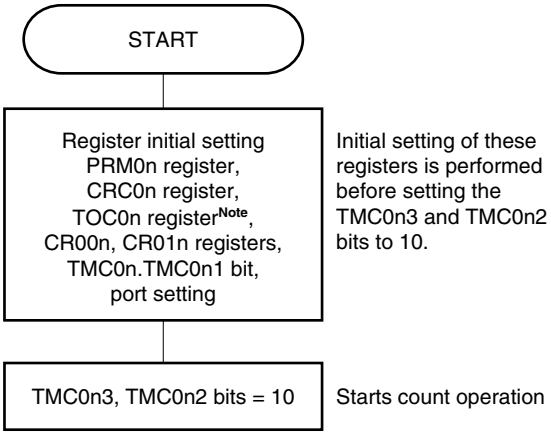
Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

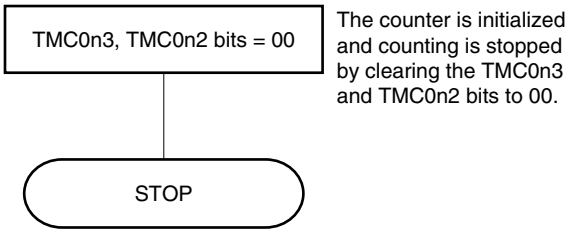
Figure 7-36. Example of Software Processing in Clear & Start Mode Entered by TI00n Pin Valid Edge Input



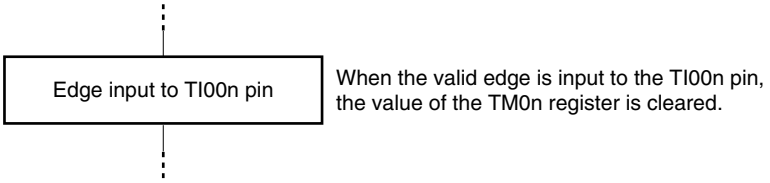
<1> Count operation start flow



<3> Count operation stop flow



<2> TM0n register clear & start flow

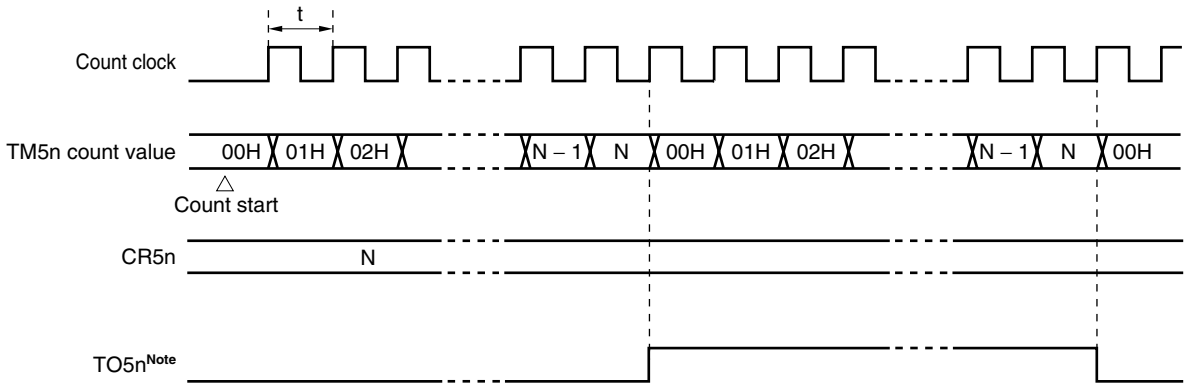


Note Care must be exercised when setting TOC0n. For details, see **7.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 8-13. Square-Wave Output Operation Timing



Note The initial value of TO5n output can be set by bits 2 and 3 (LVR5n, LVS5n) of 8-bit timer mode control register 5n (TMC5n).

8.4.4 PWM output operation

8-bit timer/event counter 5n operates as a PWM output when bit 6 (TMC5n6) of 8-bit timer mode control register 5n (TMC5n) is set to 1.

The duty pulse determined by the value set to 8-bit timer compare register 5n (CR5n) is output from TO5n.

Set the active level width of the PWM pulse to CR5n; the active level can be selected with bit 1 (TMC5n1) of TMC5n.

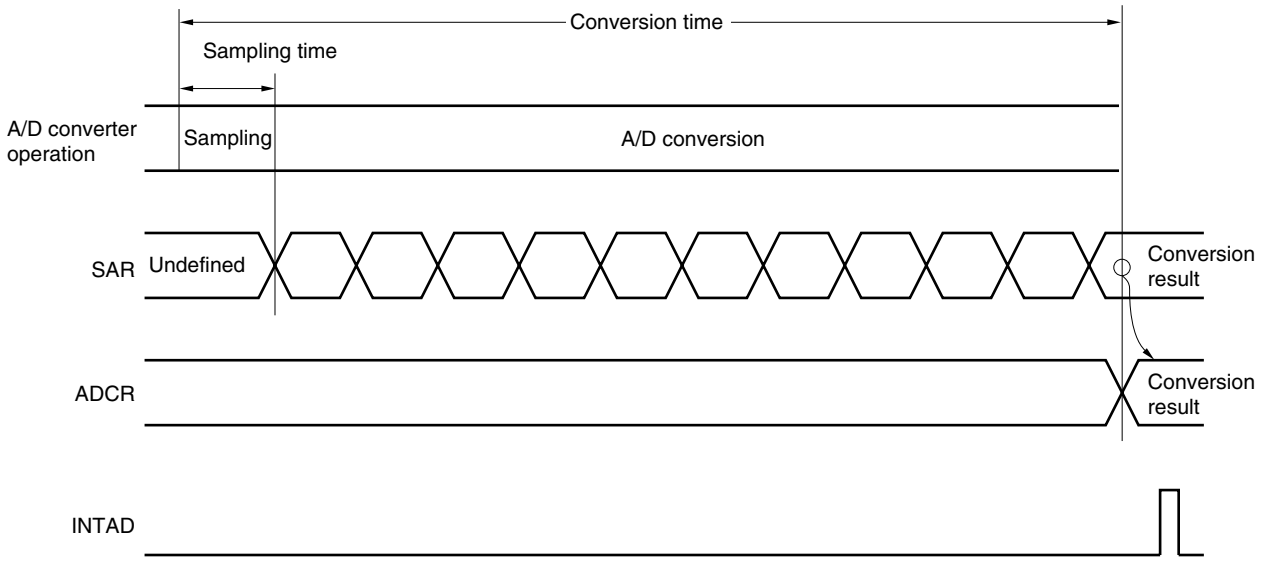
The count clock can be selected with bits 0 to 2 (TCL5n0 to TCL5n2) of timer clock selection register 5n (TCL5n).

PWM output can be enabled/disabled with bit 0 (TOE5n) of TMC5n.

Caution In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.

Remark n = 0, 1

Figure 13-11. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.

13.4.2 Input voltage and conversion results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI7) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$SAR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

or

$$\left(\frac{ADCR}{64} - 0.5\right) \times \frac{AV_{REF}}{1024} \leq V_{AIN} < \left(\frac{ADCR}{64} + 0.5\right) \times \frac{AV_{REF}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses

V_{AIN}: Analog input voltage

AV_{REF}: AV_{REF} pin voltage

ADCR: A/D conversion result register (ADCR) value

SAR: Successive approximation register

Remark ANI0 to ANI3: 78K0/KB2

ANI0 to ANI5: 38-pin products of the 78K0/KC2

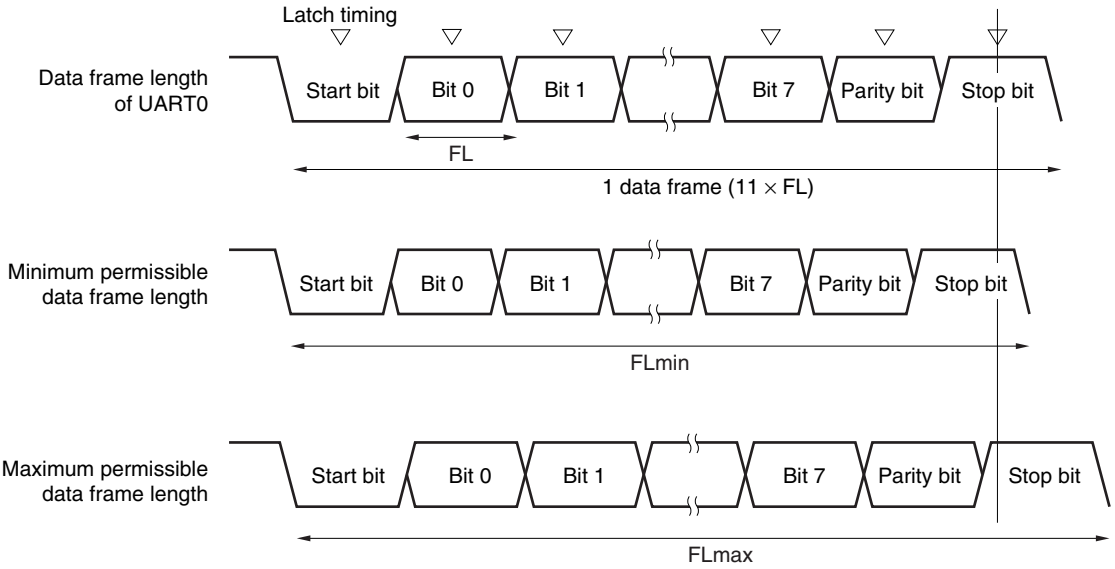
ANI0 to ANI7: Products other than above

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 14-12. Permissible Baud Rate Range During Reception



As shown in Figure 14-12, the latch timing of the receive data is determined by the counter set by baud rate generator control register 0 (BRGC0) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.

Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART0
k: Set value of BRGC0
FL: 1-bit data length
Margin of latch timing: 2 clocks

- Serial operation mode register 11 (CSIM11)

Address: FF88H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CSIM11	CSIE11	TRMD11	SSE11	DIR11	0	0	0	CSOT11

CSIE11	Operation control in 3-wire serial I/O mode
0	Disables operation[Note 1] and asynchronously resets the internal circuit[Note 2].

Notes 1. To use P02/SO11, P04/$\overline{\text{SCK11}}$, and P05/$\overline{\text{SSI11}}$/TI001 as general-purpose ports, set CSIM11 in the default status (00H).

2. Bit 0 (CSOT11) of CSIM11 and serial I/O shift register 11 (SIO11) are reset.

16.4.2 3-wire serial I/O mode

The 3-wire serial I/O mode is used for connecting peripheral ICs and display controllers with a clocked serial interface.

In this mode, communication is executed by using three lines: the serial clock ($\overline{\text{SCK1n}}$), serial output (SO1n), and serial input (SI1n) lines.

(1) Registers used

- Serial operation mode register 1n (CSIM1n)
- Serial clock selection register 1n (CSIC1n)
- Port mode register 0 (PM0) or port mode register 1 (PM1)
- Port register 0 (P0) or port register 1 (P1)

The basic procedure of setting an operation in the 3-wire serial I/O mode is as follows.

<1> Set the CSIC1n register (see **Figures 16-5** and **16-6**).

<2> Set bits 4 to 6 (DIR1n, SSE11 (serial interface CSI11 only), and TRMD1n) of the CSIM1n register (see **Figures 16-3** and **16-4**).

<3> Set bit 7 (CSIE1n) of the CSIM1n register to 1. → Transmission/reception is enabled.

<4> Write data to transmit buffer register 1n (SOTB1n). → Data transmission/reception is started.
Read data from serial I/O shift register 1n (SIO1n). → Data reception is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(5) SO1n output (see Figures 16-1 and 16-2)

The status of the SO1n output is as follows depending on the setting of CSIE1n, TRMD1n, DAP1n, and DIR1n.

Table 16-3. SO1n Output Status

CSIE1n	TRMD1n	DAP1n	DIR1n	SO1n Output[Note 1]
CSIE1n = 0[Note 2]	TRMD1n = 0[Notes 2, 3]	–	–	Low level output[Note 2]
	TRMD1n = 1	DAP1n = 0	–	Low level output
		DAP1n = 1	DIR1n = 0	Value of bit 7 of SOTB1n
			DIR1n = 1	Value of bit 0 of SOTB1n
CSIE1n = 1	TRMD1n = 0[Note 3]	–	–	Low level output
	TRMD1n = 1	–	–	Transmission data[Note 4]

Notes 1. The actual output of the SO10/P12 or SO11/P02 pin is determined according to PM12 and P12 or PM02 and P02, as well as the SO1n output.

2. This is a status after reset.

3. To use the P12/SO10 or P02/SO11 pin as general-purpose port, set the serial clock selection register 1n (CSIC1n) in the default status (00H).

4. After transmission has been completed, the SO1n pin holds the output value of the last bit of transmission data.

Caution If a value is written to CSIE1n, TRMD1n, DAP1n, and DIR1n, the output value of SO1n changes.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Table 20-2. Flags Corresponding to Interrupt Request Sources (2/2)

KB2	KC2	KD2	KE2	KF2	Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register
√	√	√	√	√	INTAD	ADIF	IF1L	ADMK	MK1L	ADPR	PR1L
√	√	√	√	√	INTSR0	SRIF0		SRMK0		SRPR0	
–	√	√	√	√	INTWTI	WTIIF		WTIMK		WTIPR	
√	√	√	√	√	INTTM51 Note 4	TMIF51		TMMK51		TMPR51	
–	√	√	√	√	INTKR	KRIF		KRMK		KRPR	
–	√	√	√	√	INTWT	WTIF		WTMK		WTPR	
–	√ Note 1	√	√	√	INTP6	PIF6		PMK6		PPR6	
–	√	√	√	√	INTP7	PIF7		PMK7		PPR7	
√ Note 2	√ Note 2	√ Note 2	√ Note 2	√	INTIIC0 Note 5	IICIF0 Note 6	IF1H	IICMK0 Note 7	MK1H	IICPR0 Note 8	PR1H
					INTDMU Note 5	DMUIF Note 6		DMUMK Note 7		DMUPR Note 8	
–	–	–	√ Note 3	√	INTCSI11	CSIIF11		CSIMK11		CSIPR11	
–	–	–	√ Note 3	√	INTTM001	TMIF001		TMMK001		TMPR001	
–	–	–	√ Note 3	√	INTTM011	TMIF011		TMMK011		TMPR011	
–	–	–	–	√	INTACSI	ACSIIF		ACSIMK		ACSIPR	

Notes 1. 48-pin products only.

2. INTIIC0: products whose flash memory is less than 32 KB
INTIIC0/INTDMU: products whose flash memory is at least 48 KB

3. Products whose flash memory is at least 48 KB only.

4. When 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (see **Figure 9-13 Transfer Timing**).

5. Do not use serial interface IIC0 and multiplier/divider simultaneously, because the flags corresponding to the interrupt request sources of serial interface IIC0 and multiplier/divider support both of these interrupt request sources. If software which operates serial interface IIC0 is developed by CC78K0 which is C compiler, do not select the check box of “Using Multiplier/Divider” on GUI of PM+.

6. If either interrupt source INTIIC0 or INTDMU is generated, bit 0 of IF1H is set (1).

7. Bit 0 of MK1H supports both interrupt sources INTIIC0 and INTDMU.

8. Bit 0 of PR1H supports both interrupt sources INTIIC0 and INTDMU.

Figure 20-13. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KC2)

Address: FFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	DUALPR0 CSIPR10 STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR1L	1	PPR6Note 1	WTPR	KRPR	TMPR51	WTIPR	SRPR0	ADPR

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	<0>
PR1H	1	1	1	1	1	1	1	IICPR0 DMUPRNote 2

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Notes 1. 48-pin products only.

2. Products whose flash memory is at least 48 KB only.

Cautions 1. Be sure to set bits 6 and 7 of PR1L to 1 in the 38-pin and 44-pin products.
Be sure to set bit 7 of PR1L to 1 in the 48-pin products.

2. Be sure to set bits 1 to 7 of PR1H to 1.

CHAPTER 25 LOW-VOLTAGE DETECTOR

25.1 Functions of Low-Voltage Detector

The low-voltage detector (LVI) is mounted onto all 78K0/Kx2 microcontroller products.
The low-voltage detector has the following functions.

- The LVI circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVI}) or the input voltage from an external input pin (EXLVI) with the detection voltage (V_{EXLVI} = 1.21 V (TYP.): fixed), and generates an internal reset or internal interrupt signal.
- The supply voltage (V_{DD}) or input voltage from an external input pin (EXLVI) can be selected by software.
- Reset or interrupt function can be selected by software.
- Detection levels (16 levels [Note]) of supply voltage can be changed by software.
- Operable in STOP mode.

Note Standard products and (A) grade products: 16 levels
(A2) grade products: 10 levels

The reset and interrupt signals are generated as follows depending on selection by software.

Selection of Level Detection of Supply Voltage (V_{DD}) (LVISEL = 0)		Selection Level Detection of Input Voltage from External Input Pin (EXLVI) (LVISEL = 1)	
Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).	Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).
Generates an internal reset signal when $V_{DD} < V_{LVI}$ and releases the reset signal when $V_{DD} \geq V_{LVI}$.	Generates an internal interrupt signal when V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$).	Generates an internal reset signal when EXLVI < V_{EXLVI} and releases the reset signal when EXLVI ≥ V_{EXLVI}.	Generates an internal interrupt signal when EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).

Remark LVISEL: Bit 2 of low-voltage detection register (LVIM)
LVIMD: Bit 1 of LVIM

While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of RESF, see **CHAPTER 23 RESET FUNCTION**.

CHAPTER 32 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: T_A = –40 to +110°C)

Target Products	Conventional-specification Products	Expanded-specification Products
78K0/KB2	μPD78F0500(A2), 78F0501(A2), 78F0502(A2), 78F0503(A2)	μPD78F0500A(A2), 78F0501A(A2), 78F0502A(A2), 78F0503A(A2)
78K0/KC2	μPD78F0511(A2), 78F0512(A2), 78F0513(A2), 78F0514(A2), 78F0515(A2)	μPD78F0511A(A2), 78F0512A(A2), 78F0513A(A2), 78F0514A(A2), 78F0515A(A2)
78K0/KD2	μPD78F0521(A2), 78F0522(A2), 78F0523(A2), 78F0524(A2), 78F0525(A2), 78F0526(A2), 78F0527(A2)	μPD78F0521A(A2), 78F0522A(A2), 78F0523A(A2), 78F0524A(A2), 78F0525A(A2), 78F0526A(A2), 78F0527A(A2)
78K0/KE2	μPD78F0531(A2), 78F0532(A2), 78F0533(A2), 78F0534(A2), 78F0535(A2), 78F0536(A2), 78F0537(A2)	μPD78F0531A(A2), 78F0532A(A2), 78F0533A(A2), 78F0534A(A2), 78F0535A(A2), 78F0536A(A2), 78F0537A(A2)
78K0/KF2	μPD78F0544(A2), 78F0545(A2), 78F0546(A2), 78F0547(A2)	μPD78F0544A(A2), 78F0545A(A2), 78F0546A(A2), 78F0547A(A2)

The following items are described separately for conventional-specification products (μPD78F05xx(A2)) and expanded-specification products (μPD78F05xxA(A2)).

- X1 clock oscillation frequency (**X1 oscillator characteristics**)
- Instruction cycle, peripheral hardware clock frequency, external main system clock frequency, external main system clock input high-level width, and external main system clock input low-level width (**(1) Basic operation** in **AC characteristics**)
- A/D conversion time (**A/D Converter Characteristics**)
- Number of rewrites per chip (**Flash Memory Programming Characteristics**)

Caution The pins mounted depend on the product as follows.

(1) Port functions

Port	78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
	30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Port 0	P00, P01				P00 to P03	P00 to P06	
Port 1	P10 to P17						
Port 2	P20 to P23	P20 to P25	P20 to P27				
Port 3	P30 to P33						
Port 4	–		P40, P41			P40 to P43	P40 to P47
Port 5	–					P50 to P53	P50 to P57
Port 6	P60, P61	P60 to P63					P60 to P67
Port 7	–	P70, P71	P70 to P73	P70 to P75	P70 to P77		
Port 12	P120 to P122	P120 to P124					
Port 13	–			P130			
Port 14	–			P140		P140, P141	P140 to P145

(The remaining table is on the next page.)

Notes 1. Total current flowing into the internal power supply (V_{DD}, EV_{DD}), including the peripheral operation current and the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, the current flowing into the pull-up resistors and the output current of the port are not included.

2. Not including the operating current of the 8 MHz internal oscillator, 240 kHz internal oscillator, and XT1 oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

3. When AMPH (bit 0 of clock operation mode select register (OSCCTL)) = 0.

4. Not including the operating current of the X1 oscillator, XT1 oscillator, and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

5. Not including the operating current of the X1 oscillation, 8 MHz internal oscillator and 240 kHz internal oscillator, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

6. Not including the operating current of the 240 kHz internal oscillator and XT1 oscillation, and the current flowing into the A/D converter, watchdog timer and LVI circuit.

7. Current flowing only to the A/D converter (AV_{REF}). The current value of the 78K0/Kx2 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

8. Current flowing only to the watchdog timer (including the operating current of the 240 kHz internal oscillator). The current value of the 78K0/Kx2 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

9. Current flowing only to the LVI circuit. The current value of the 78K0/Kx2 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

DC Characteristics (3/4)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 4.0 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 2.0 mA				0.7	V
	V_{OL2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA				0.4	V
		P121 to P124	I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.0 mA				2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA				0.6	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 2.0 mA				0.6	V
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P140 to P145, FLMD0, $\overline{\text{RESET}}$	V_I = V_{DD}				5	μA
	I_{LIH2}	P20 to P27	V_I = AV_{REF} = V_{DD}				5	μA
	I_{LIH3}	P121 to 124 (X1, X2, XT1, XT2)	V_I = V_{DD}	I/O port mode			5	μA
				OSC mode			20	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P140 to P145, FLMD0, $\overline{\text{RESET}}$	V_I = V_{SS}				–5	μA
	I_{LIL2}	P20 to P27	V_I = V_{SS}, AV_{REF} = V_{DD}				–5	μA
	I_{LIL3}	P121 to 124 (X1, X2, XT1, XT2)	V_I = V_{SS}	I/O port mode			–5	μA
				OSC mode			–20	μA
Pull-up resistor	R_U	V_I = V_{SS}			10	20	100	kΩ
FLMD0 supply voltage	V_{IL}	In normal operation mode			0		0.2V_{DD}	V
	V_{IH}	In self-programming mode			0.8V_{DD}		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.