Renesas Electronics America Inc - UPD78F0531AGC-GAL-AX Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

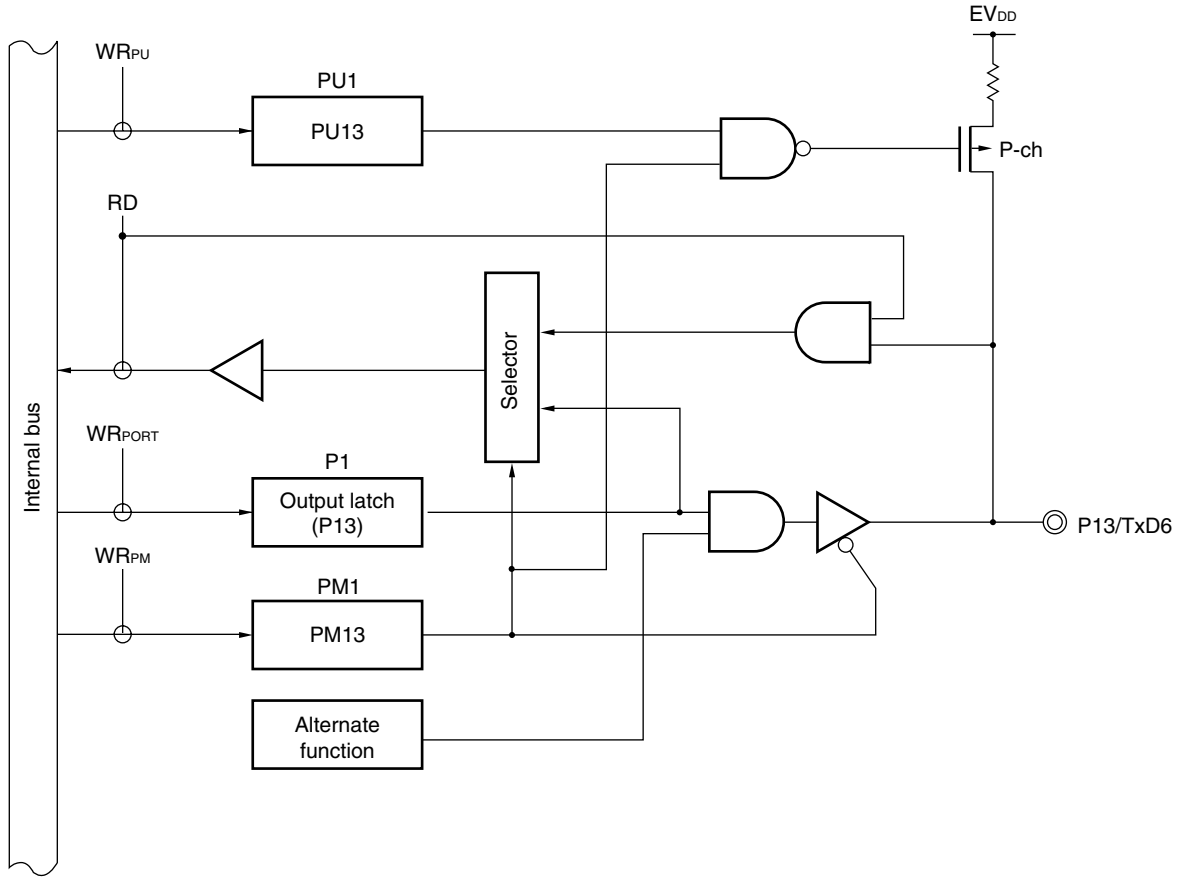
Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0531agc-gal-ax

How to Use This Manual

Readers This manual is intended for user engineers who wish to understand the functions of the 78K0/Kx2 microcontrollers and design and develop application systems and programs for these devices.
The target products are as follows.

	Conventional-specification Products	Expanded-specification Products
78K0/KB2	μPD78F0500, 78F0501, 78F0502, 78F0503, 78F0503D, 78F0500(A), 78F0501(A), 78F0502(A), 78F0503(A), 78F0500(A2), 78F0501(A2), 78F0502(A2), 78F0503(A2)	μPD78F0500A, 78F0501A, 78F0502A, 78F0503A, 78F0503DA, 78F0500A(A), 78F0501A(A), 78F0502A(A), 78F0503A(A), 78F0500A(A2), 78F0501A(A2), 78F0502A(A2), 78F0503A(A2)
78K0/KC2	μPD78F0511, 78F0512, 78F0513, 78F0514, 78F0515, 78F0513D, 78F0515D, 78F0511(A), 78F0512(A), 78F0513(A), 78F0514(A), 78F0515(A), 78F0511(A2), 78F0512(A2), 78F0513(A2), 78F0514(A2), 78F0515(A2)	μPD78F0511A, 78F0512A, 78F0513A, 78F0514A, 78F0515A, 78F0513DA, 78F0515DA, 78F0511A(A), 78F0512A(A), 78F0513A(A), 78F0514A(A), 78F0515A(A), 78F0511A(A2), 78F0512A(A2), 78F0513A(A2), 78F0514A(A2), 78F0515A(A2)
78K0/KD2	μPD78F0521, 78F0522, 78F0523, 78F0524, 78F0525, 78F0526, 78F0527, 78F0527D, 78F0521(A), 78F0522(A), 78F0523(A), 78F0524(A), 78F0525(A), 78F0526(A), 78F0527(A), 78F0521(A2), 78F0522(A2), 78F0523(A2), 78F0524(A2), 78F0525(A2), 78F0526(A2), 78F0527(A2)	μPD78F0521A, 78F0522A, 78F0523A, 78F0524A, 78F0525A, 78F0526A, 78F0527A, 78F0527DA, 78F0521A(A), 78F0522A(A), 78F0523A(A), 78F0524A(A), 78F0525A(A), 78F0526A(A), 78F0527A(A), 78F0521A(A2), 78F0522A(A2), 78F0523A(A2), 78F0524A(A2), 78F0525A(A2), 78F0526A(A2), 78F0527A(A2)
78K0/KE2	μPD78F0531, 78F0532, 78F0533, 78F0534, 78F0535, 78F0536, 78F0537, 78F0537D, 78F0531(A), 78F0532(A), 78F0533(A), 78F0534(A), 78F0535(A), 78F0536(A), 78F0537(A), 78F0531(A2), 78F0532(A2), 78F0533(A2), 78F0534(A2), 78F0535(A2), 78F0536(A2), 78F0537(A2)	μPD78F0531A, 78F0532A, 78F0533A, 78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA, 78F0531A(A), 78F0532A(A), 78F0533A(A), 78F0534A(A), 78F0535A(A), 78F0536A(A), 78F0537A(A), 78F0531A(A2), 78F0532A(A2), 78F0533A(A2), 78F0534A(A2), 78F0535A(A2), 78F0536A(A2), 78F0537A(A2)
78K0/KF2	μPD78F0544, 78F0545, 78F0546, 78F0547, 78F0547D, 78F0544(A), 78F0545(A), 78F0546(A), 78F0547(A), 78F0544(A2), 78F0545(A2), 78F0546(A2), 78F0547(A2)	μPD78F0544A, 78F0545A, 78F0546A, 78F0547A, 78F0547DA, 78F0544A(A), 78F0545A(A), 78F0546A(A), 78F0547A(A), 78F0544A(A2), 78F0545A(A2), 78F0546A(A2), 78F0547A(A2)

Figure 5-10. Block Diagram of P13



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

(1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock[Note 1]

<1> Setting restart of oscillation of the internal high-speed oscillation clock (RCM register)
When RSTOP is cleared to 0, the internal high-speed oscillation clock starts operating.

<2> Waiting for the oscillation accuracy stabilization time of internal high-speed oscillation clock (RCM register)
Wait until RSTS is set to 1[Note 2].

Notes 1. After a reset release, the internal high-speed oscillator automatically starts oscillating and the internal high-speed oscillation clock is selected as the CPU clock.

2. This wait time is not necessary if high accuracy is not necessary for the CPU clock and peripheral hardware clock.

(2) Example of setting procedure when using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock

<1> • Restarting oscillation of the internal high-speed oscillation clock[Note]
(See **6.6.2 (1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock**).

• Oscillating the high-speed system clock[Note]
(This setting is required when using the high-speed system clock as the peripheral hardware clock. See **6.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when the internal high-speed oscillation clock or high-speed system clock is already operating.

<2> Selecting the clock supplied as the main system clock and peripheral hardware clock (MCM register)
Set the main system clock and peripheral hardware clock using XSEL and MCM0.

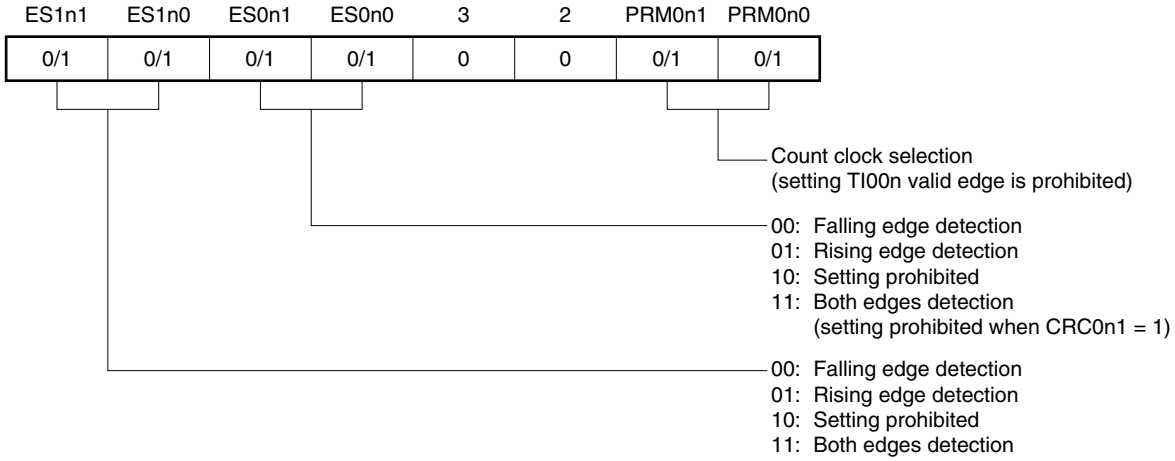
XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{RH})	Internal high-speed oscillation clock (f_{RH})
0	1		
1	0		High-speed system clock (f_{XH})

<3> Selecting the CPU clock division ratio (PCC register)
When CSS is cleared to 0, the main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	0	f_{XP}
	0	0	1	$f_{XP}/2$ (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
	Other than above			Setting prohibited

Figure 7-35. Example of Register Settings in Clear & Start Mode Entered by TI00n Pin Valid Edge Input (2/2)

(d) Prescaler mode register 0n (PRM0n)



(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM00n) is generated. The count value of TM0n is not cleared.

To use this register as a capture register, select either the TI00n or TI01n pin[Note] input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR00n.

Note The timer output (TO0n) cannot be used when detection of the valid edge of the TI01n pin is used.

(g) 16-bit capture/compare register 01n (CR01n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM01n) is generated. The count value of TM0n is not cleared.

When this register is used as a capture register, the TI00n pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR01n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

7.4.6 PPG output operation

A square wave having a pulse width set in advance by CR01n is output from the TO0n pin as a PPG (Programmable Pulse Generator) signal during a cycle set by CR00n when bits 3 and 2 (TMC0n3 and TMC0n2) of 16-bit timer mode control register 0n (TMC0n) are set to 11 (clear & start upon a match between TM0n and CR00n).

The pulse cycle and duty factor of the pulse generated as the PPG output are as follows.

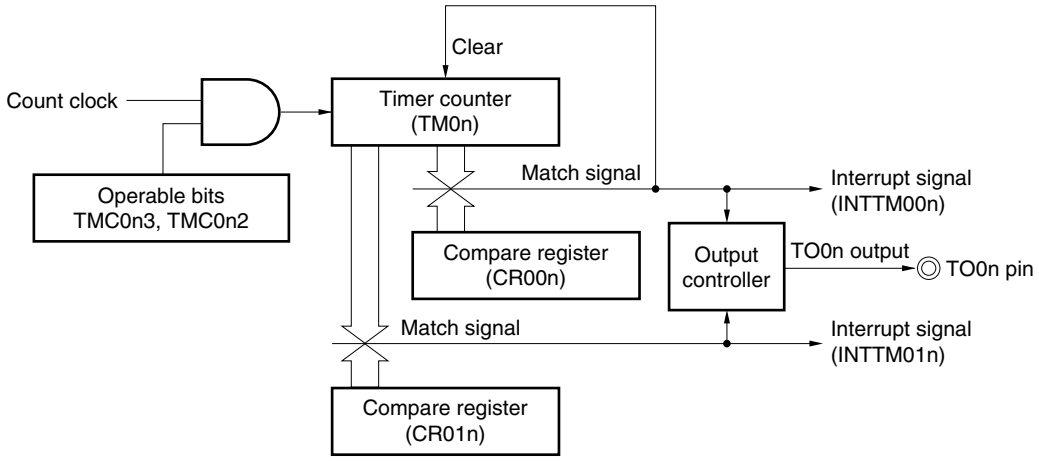
- Pulse cycle = (Set value of CR00n + 1) × Count clock cycle
- Duty = (Set value of CR01n + 1) / (Set value of CR00n + 1)

Caution To change the duty factor (value of CR01n) during operation, see 7.5.1 Rewriting CR01n during TM0n operation.

Remarks 1. For the setting of I/O pins, see **7.3 (5) Port mode register 0 (PM0)**.

2. For how to enable the INTTM00n signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

Figure 7-45. Block Diagram of PPG Output Operation

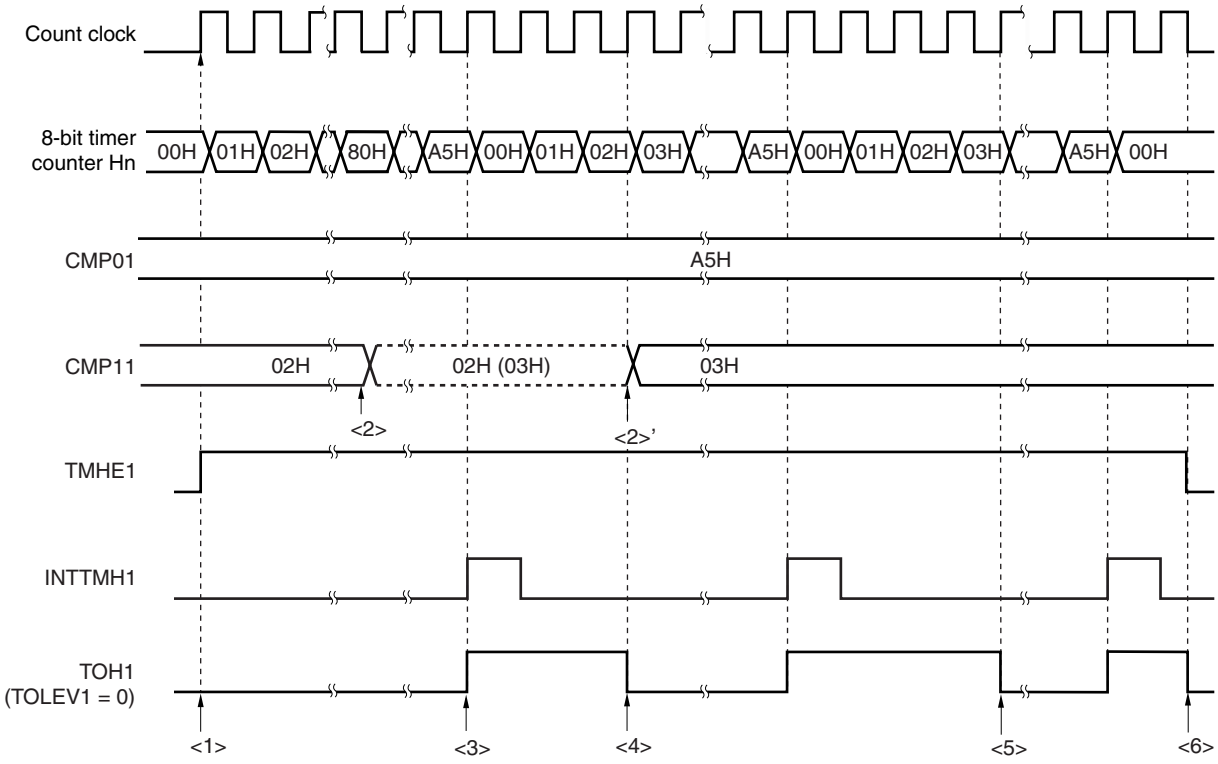


Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 9-12. Operation Timing in PWM Output Mode (4/4)

(e) Operation by changing CMP1n (CMP1n = 02H → 03H, CMP0n = A5H)



<1> The count operation is enabled by setting TMHEn = 1. Start the 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> The CMP1n register value can be changed during timer counter operation. This operation is asynchronous to the count clock.

<3> When the values of the 8-bit timer counter Hn and the CMP0n register match, the value of the 8-bit timer counter Hn is cleared, an active level is output, and the INTTMHn signal is output.

<4> If the CMP1n register value is changed, the value is latched and not transferred to the register. When the values of the 8-bit timer counter Hn and the CMP1n register before the change match, the value is transferred to the CMP1n register and the CMP1n register value is changed (<2>').

However, three count clocks or more are required from when the CMP1n register value is changed to when the value is transferred to the register. If a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

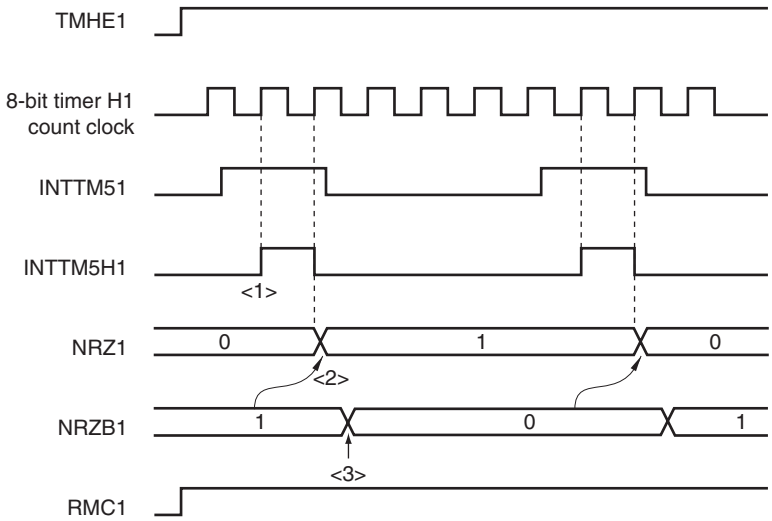
<5> When the values of the 8-bit timer counter Hn and the CMP1n register after the change match, an inactive level is output. The 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<6> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

Remark n = 0, 1

To control the carrier pulse output during a count operation, the NRZ1 and NRZB1 bits of the TMCYC1 register have a master and slave bit configuration. The NRZ1 bit is read-only but the NRZB1 bit can be read and written. The INTTM51 signal is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal. The INTTM5H1 signal becomes the data transfer signal of the NRZ1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit. The timing for transfer from the NRZB1 bit to the NRZ1 bit is as shown below.

Figure 9-13. Transfer Timing



<1> The INTTM51 signal is synchronized with the count clock of the 8-bit timer H1 and is output as the INTTM5H1 signal.

<2> The value of the NRZB1 bit is transferred to the NRZ1 bit at the second clock from the rising edge of the INTTM5H1 signal.

<3> Write the next value to the NRZB1 bit in the interrupt servicing program that has been started by the INTTM5H1 interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR51 register.

Cautions 1. Do not rewrite the NRZB1 bit again until at least the second clock after it has been rewritten, or else the transfer from the NRZB1 bit to the NRZ1 bit is not guaranteed.

2. When the 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated at the timing of <1>. When the 8-bit timer/event counter 51 is used in a mode other than the carrier generator mode, the timing of the interrupt generation differs.

Remark INTTM5H1 is an internal signal and not an interrupt source.

10.4 Watch Timer Operations

10.4.1 Watch timer operation

The watch timer generates an interrupt request signal (INTWT) at a specific time interval by using the peripheral hardware clock or subsystem clock.

When bit 0 (WTM0) and bit 1 (WTM1) of the watch timer operation mode register (WTM) are set to 1, the count operation starts. When these bits are cleared to 0, the 5-bit counter is cleared and the count operation stops.

When the interval timer is simultaneously operated, zero-second start can be achieved only for the watch timer by clearing WTM1 to 0. In this case, however, the 11-bit prescaler is not cleared. Therefore, an error up to $2^9 \times 1/fw$ seconds occurs in the first overflow (INTWT) after zero-second start.

The interrupt request is generated at the following time intervals.

Table 10-4. Watch Timer Interrupt Time

WTM3	WTM2	Interrupt Time Selection	When Operated at f_{SUB} = 32.768 kHz (WTM7 = 1)	When Operated at f_{PRS} = 2 MHz (WTM7 = 0)	When Operated at f_{PRS} = 5 MHz (WTM7 = 0)	When Operated at f_{PRS} = 10 MHz (WTM7 = 0)	When Operated at f_{PRS} = 20 MHz (WTM7 = 0)
0	0	$2^{14}/fw$	0.5 s	1.05 s	0.419 s	0.210 s	0.105 s
0	1	$2^{13}/fw$	0.25 s	0.52 s	0.210 s	0.105 s	52.5 ms
1	0	$2^5/fw$	977 μs	2.05 ms	819 μs	410 μs	205 μs
1	1	$2^4/fw$	488 μs	1.02 ms	410 μs	205 μs	102 μs

Remarks 1. fw: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

10.4.2 Interval timer operation

The watch timer operates as interval timer which generates interrupt request signals (INTWTI) repeatedly at an interval of the preset count value.

The interval time can be selected with bits 4 to 6 (WTM4 to WTM6) of the watch timer operation mode register (WTM).

When bit 0 (WTM0) of the WTM is set to 1, the count operation starts. When this bit is set to 0, the count operation stops.

Table 10-5. Interval Timer Interval Time

WTM6	WTM5	WTM4	Interval Time	When Operated at f_{SUB} = 32.768 kHz (WTM7 = 1)	When Operated at f_{PRS} = 2 MHz (WTM7 = 0)	When Operated at f_{PRS} = 5 MHz (WTM7 = 0)	When Operated at f_{PRS} = 10 MHz (WTM7 = 0)	When Operated at f_{PRS} = 20 MHz (WTM7 = 0)
0	0	0	$2^4/fw$	488 μs	1.02 ms	410 μs	205 μs	102 μs
0	0	1	$2^5/fw$	977 μs	2.05 ms	820 μs	410 μs	205 μs
0	1	0	$2^6/fw$	1.95 ms	4.10 ms	1.64 ms	820 μs	410 μs
0	1	1	$2^7/fw$	3.91 ms	8.20 ms	3.28 ms	1.64 ms	820 μs
1	0	0	$2^8/fw$	7.81 ms	16.4 ms	6.55 ms	3.28 ms	1.64 ms
1	0	1	$2^9/fw$	15.6 ms	32.8 ms	13.1 ms	6.55 ms	3.28 ms
1	1	0	$2^{10}/fw$	31.3 ms	65.5 ms	26.2 ms	13.1 ms	6.55 ms
1	1	1	$2^{11}/fw$	62.5 ms	131.1 ms	52.4 ms	26.2 ms	13.1 ms

Remarks 1. fw: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

Caution When data is read from ADCR and ADCRH, a wait cycle is generated. Do not read data from ADCR and ADCRH when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. Make this pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

The signal input to ANI0 to ANI7 is converted into a digital signal, based on the voltage applied across AV_{REF} and AV_{SS}.

(10) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always use this pin at the same potential as that of the V_{SS} pin even when the A/D converter is not used.

(11) A/D converter mode register (ADM)

This register is used to set the conversion time of the analog input signal to be converted, and to start or stop the conversion operation.

(12) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 pins to analog input of A/D converter or digital I/O of port.

(13) Analog input channel specification register (ADS)

This register is used to specify the port that inputs the analog voltage to be converted into a digital signal.

(14) Port mode register 2 (PM2)

This register switches the ANI0/P20 to ANI7/P27 pins to input or output.

Remark ANI0 to ANI3: 78K0/KB2
ANI0 to ANI5: 38-pin products of the 78K0/KC2
ANI0 to ANI7: Products other than above

Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when $f_{PRS} = f_{XH}$ (XSEL = 1).)

2. Set the serial clock to satisfy the following conditions.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD) and Expanded-specification Products (μPD78F05xxA and 78F05xxDA)		
	Standard Products	(A) Grade Products	(A2) Grade Products
4.0 V ≤ V_{DD} ≤ 5.5 V	Serial clock ≤ 6.25 MHz	Serial clock ≤ 5 MHz	Serial clock ≤ 5 MHz
2.7 V ≤ V_{DD} < 4.0 V	Serial clock ≤ 4 MHz	Serial clock ≤ 2.5 MHz	Serial clock ≤ 2.5 MHz
1.8 V ≤ V_{DD} < 2.7 V	Serial clock ≤ 2 MHz	Serial clock ≤ 1.66 MHz	–

3. Do not start communication with the external clock from the $\overline{SCK10}$ pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. Do not write to CSIC10 while CSIE10 = 1 (operation enabled).

2. To use P10/$\overline{SCK10}$/TxD0 and P12/SO10 as general-purpose ports, set CSIC10 in the default status (00H).

3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock frequency

Table 18-7. Wait Periods

CL01	CL00	Wait Period
0	0	6 clocks
0	1	6 clocks
1	0	12 clocks
1	1	3 clocks

18.5.15 Cautions

(1) When STCEN (bit 1 of IIC flag register 0 (IICF0)) = 0

Immediately after I^2C operation is enabled (IICE0 = 1), the bus communication status (IICBSY flag (bit 6 of IICF0) = 1) is recognized regardless of the actual bus status. When changing from a mode in which no stop condition has been detected to a master device communication mode, first generate a stop condition to release the bus, then perform master device communication.

When using multiple masters, it is not possible to perform master device communication when the bus has not been released (when a stop condition has not been detected).

Use the following sequence for generating a stop condition.

<1> Set IIC clock selection register 0 (IICCL0).
<2> Set bit 7 (IICE0) of IIC control register 0 (IICC0) to 1.
<3> Set bit 0 (SPT0) of IICC0 to 1.

(2) When STCEN = 1

Immediately after I^2C operation is enabled (IICE0 = 1), the bus released status (IICBSY = 0) is recognized regardless of the actual bus status. To generate the first start condition (STT0 (bit 1 of IIC control register 0 (IICC0)) = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

(3) If other I^2C communications are already in progress

If I^2C operation is enabled and the device participates in communication already in progress when the SDA0 pin is low and the SCL0 pin is high, the macro of I^2C recognizes that the SDA0 pin has gone low (detects a start condition). If the value on the bus at this time can be recognized as an extension code, $\overline{ACK}$ is returned, but this interferes with other I^2C communications. To avoid this, start I^2C in the following sequence.

<1> Clear bit 4 (SPIE0) of IICC0 register to 0 to disable generation of an interrupt request signal (INTIIC0) when the stop condition is detected.
<2> Set bit 7 (IICE0) of IICC0 register to 1 to enable the operation of I^2C.
<3> Wait for detection of the start condition.
<4> Set bit 6 (LREL0) of IICC0 register to 1 before $\overline{ACK}$ is returned (4 to 80 clocks after setting IICE0 bit to 1), to forcibly disable detection.

(4) Determine the transfer clock frequency by using SMC0, CL01, CL00 bits (bits 3, 1, and 0 of IICL0 register), and CLX0 bit (bit 0 of IICX0 register) before enabling the operation (IICE0 = 1). To change the transfer clock frequency, clear IICE0 bit to 0 once.

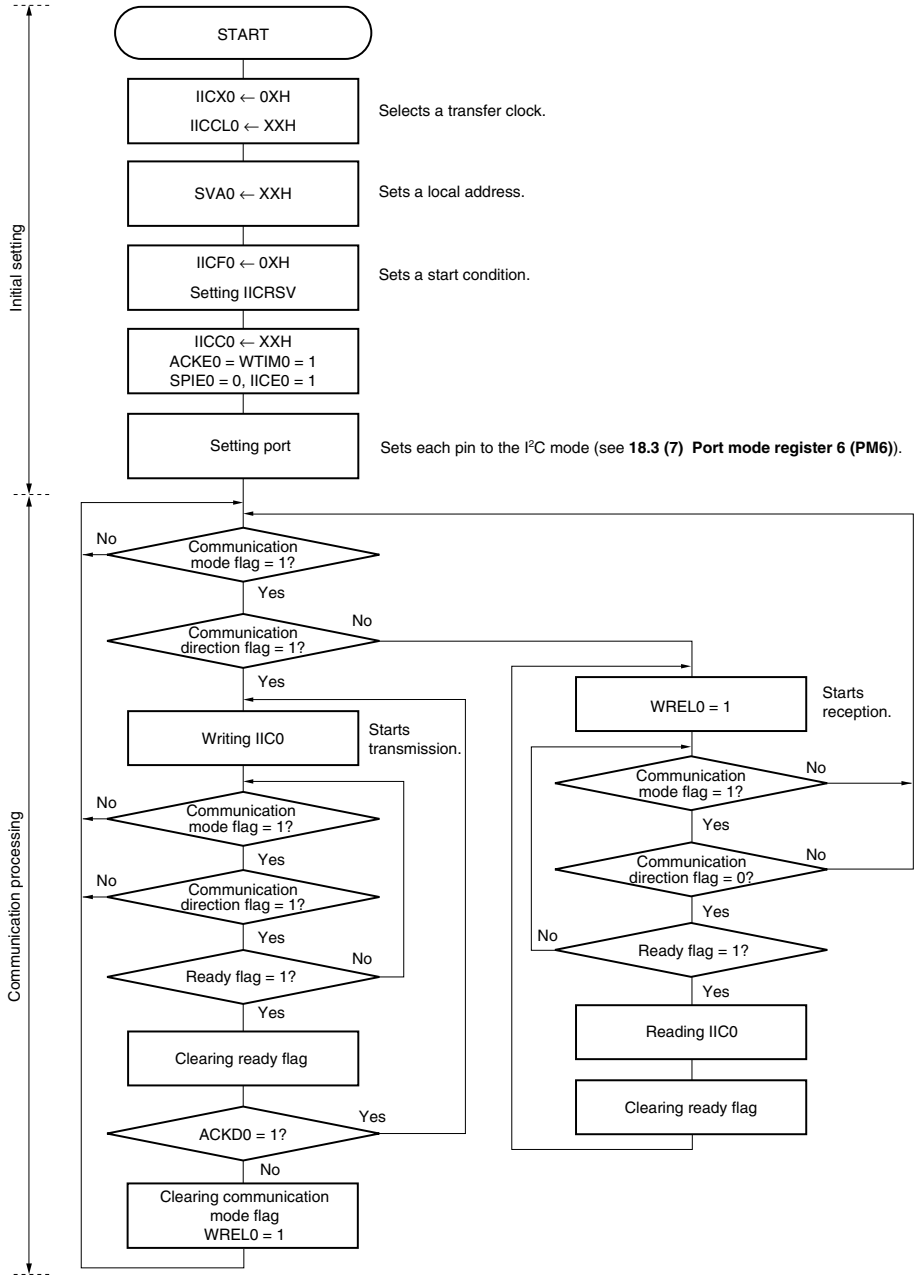
The main processing of the slave operation is explained next.

Start serial interface IIC0 and wait until communication is enabled. When communication is enabled, execute communication by using the communication mode flag and ready flag (processing of the stop condition and start condition is performed by an interrupt. Here, check the status by using the flags).

The transmission operation is repeated until the master no longer returns $\overline{ACK}$. If $\overline{ACK}$ is not returned from the master, communication is completed.

For reception, the necessary amount of data is received. When communication is completed, $\overline{ACK}$ is not returned as the next data. After that, the master generates a stop condition or restart condition. Exit from the communication status occurs in this way.

Figure 18-25. Slave Operation Flowchart (1)



Remark Conform to the specifications of the product that is in communication, regarding the transmission and reception formats.

19.3 Register Controlling Multiplier/Divider

The multiplier/divider is controlled by multiplier/divider control register 0 (DMUC0).

(1) Multiplier/divider control register 0 (DMUC0)

DMUC0 is an 8-bit register that controls the operation of the multiplier/divider.

DMUC0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears DMUC0 to 00H.

Figure 19-5. Format of Multiplier/Divider Control Register 0 (DMUC0)

Address: FF68H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
DMUC0	DMUE	0	0	0	0	0	0	DMUSEL0

DMUE[Note]	Operation start/stop
0	Stops operation
1	Starts operation

DMUSEL0	Operation mode (multiplication/division) selection
0	Division mode
1	Multiplication mode

Note When DMUE is set to 1, the operation is started. DMUE is automatically cleared to 0 after the operation is complete.

Cautions 1. If DMUE is cleared to 0 during operation processing (when DMUE is 1), the operation result is not guaranteed. If the operation is completed while the clearing instruction is being executed, the operation result is guaranteed, provided that the interrupt flag is set.

2. Do not change the value of DMUSEL0 during operation processing (while DMUE is 1). If it is changed, undefined operation results are stored in multiplication/division data register A0 (MDA0) and remainder data register 0 (SDR0).

3. If DMUE is cleared to 0 during operation processing (while DMUE is 1), the operation processing is stopped. To execute the operation again, set multiplication/division data register A0 (MDA0), multiplication/division data register B0 (MDB0), and multiplier/divider control register 0 (DMUC0), and start the operation (by setting DMUE to 1).

CHAPTER 20 INTERRUPT FUNCTIONS

		78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
					Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
Maskable interrupts	External	6	38/44 pins: 7 ch 48 pins: 8 ch	8	9	9	9
	internal	14	16	16	16	19	20

20.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into a high interrupt priority group and a low interrupt priority group by setting the priority specification flag registers (PR0L, PR0H, PR1L, PR1H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. For the priority order, see **Table 20-1**.

A standby release signal is generated and STOP and HALT modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

20.2 Interrupt Sources and Configuration

The interrupt sources consist of maskable interrupts and software interrupts. In addition, they also have up to four reset sources (see **Table 20-1**).

27.6.6 Other signal pins

Connect X1 and X2 in the same status as in the normal operation mode when using the on-board clock.

To input the operating clock from the dedicated flash memory programmer, however, connect CLK of the programmer to EXCLK/X2/P122.

Cautions 1. Only the internal high-speed oscillation clock (f_{RH}) can be used when CSI10 is used.

2. Only the X1 clock (f_X) or external main system clock (f_{EXCLK}) can be used when UART6 is used.

3. For the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA), connect P31/INTP2/OCD1A and P121/X1/OCD0A as follows when writing the flash memory with a flash memory programmer.

- **P31/INTP2/OCD1A: Connect to EV_{SS}[Note] via a resistor.**
- **P121/X1/OCD0A: Connect to V_{SS}[Note] via a resistor.**

Note With products without an EV_{SS} pin, connect them to V_{SS}.

27.6.7 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

However, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer, even when using the on-board supply voltage.

Supply the same other power supplies (EV_{DD}, EV_{SS}, AV_{REF}, and AV_{SS}) as those in the normal operation mode.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit operation	**SUB**	A, #byte	2	4	–	A, CY ← A – byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte	× × ×
		A, r Note 3	2	4	–	A, CY ← A – r	× × ×
		r, A	2	4	–	r, CY ← r – A	× × ×
		A, saddr	2	4	5	A, CY ← A – (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A – (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A – (HL)	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B)	× × ×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C)	× × ×
	SUBC	A, #byte	2	4	–	A, CY ← A – byte – CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte – CY	× × ×
		A, r Note 3	2	4	–	A, CY ← A – r – CY	× × ×
		r, A	2	4	–	r, CY ← r – A – CY	× × ×
		A, saddr	2	4	5	A, CY ← A – (saddr) – CY	× × ×
		A, !addr16	3	8	9	A, CY ← A – (addr16) – CY	× × ×
		A, [HL]	1	4	5	A, CY ← A – (HL) – CY	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte) – CY	× × ×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B) – CY	× × ×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C) – CY	× × ×
	AND	A, #byte	2	4	–	A ← A ∧ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∧ byte	×
		A, r Note 3	2	4	–	A ← A ∧ r	×
		r, A	2	4	–	r ← r ∧ A	×
		A, saddr	2	4	5	A ← A ∧ (saddr)	×
		A, !addr16	3	8	9	A ← A ∧ (addr16)	×
		A, [HL]	1	4	5	A ← A ∧ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ∧ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ∧ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ∧ (HL + C)	×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(f) CSIA0 (master mode, $\overline{\text{SCKA0}}$…internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKA0}}$ cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V		600			ns
		2.7 V ≤ V_{DD} < 4.0 V		1200			ns
		1.8 V ≤ V_{DD} < 2.7 V		1800			ns
$\overline{\text{SCKA0}}$ high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3}/2 - 50$			ns
		2.7 V ≤ V_{DD} < 4.0 V		$t_{KCY3}/2 - 100$			ns
		1.8 V ≤ V_{DD} < 2.7 V		$t_{KCY3}/2 - 200$			ns
SIA0 setup time (to $\overline{\text{SCKA0}}$↑)	t_{SIK3}	2.7 V ≤ V_{DD} ≤ 5.5 V		100			ns
		1.8 V ≤ V_{DD} < 2.7 V		200			ns
SIA0 hold time (from $\overline{\text{SCKA0}}$↑)	t_{KSI3}			300			ns
Delay time from $\overline{\text{SCKA0}}$↓ to SOA0 output	t_{KSO3}	C = 100 pF[Note]	4.0 V ≤ V_{DD} ≤ 5.5 V			200	ns
			2.7 V ≤ V_{DD} < 4.0 V			300	ns
			1.8 V ≤ V_{DD} < 2.7 V			400	ns
Time from $\overline{\text{SCKA0}}$↑ to STB0↑	t_{SBD}			$t_{KCY3}/2 - 100$			ns
Strobe signal high-level width	t_{SBW}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3} - 30$			ns
		2.7 V ≤ V_{DD} < 4.0 V		$t_{KCY3} - 60$			ns
		1.8 V ≤ V_{DD} < 2.7 V		$t_{KCY3} - 120$			ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}	2.7 V ≤ V_{DD} ≤ 5.5 V		100			ns
		1.8 V ≤ V_{DD} < 2.7 V		200			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}			100			ns
Time from busy inactive to $\overline{\text{SCKA0}}$↓	t_{SPS}	4.0 V ≤ V_{DD} ≤ 5.5 V				$2t_{KCY3} + 100$	ns
		2.7 V ≤ V_{DD} < 4.0 V				$2t_{KCY3} + 150$	ns
		1.8 V ≤ V_{DD} < 2.7 V				$2t_{KCY3} + 200$	ns

Note C is the load capacitance of the $\overline{\text{SCKA0}}$ and SOA0 output lines.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

2.7 V POC Circuit Characteristics (T_A = –40 to +110°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option bye) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until V_{POC} = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC}, similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until V_{DDPOC} = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at V_{POC} = 1.59 V (TYP.) and not at V_{DDPOC}. The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH}.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

LVI Circuit Characteristics (T_A = –40 to +110°C, $V_{POC} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $AV_{REF} \leq V_{DD}$, $V_{SS} = EV_{SS}$ = 0 V)

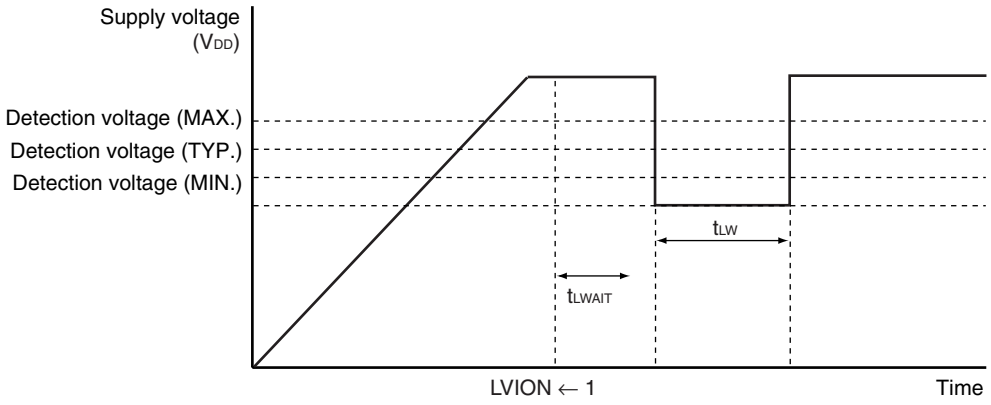
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.14	4.24	4.34	V
		V_{LVI1}		3.99	4.09	4.19	V
		V_{LVI2}		3.83	3.93	4.03	V
		V_{LVI3}		3.68	3.78	3.88	V
		V_{LVI4}		3.52	3.62	3.72	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.06	3.16	3.26	V
		V_{LVI8}		2.91	3.01	3.11	V
		V_{LVI9}		2.75	2.85	2.95	V
	External input pin[Note 1]	EXLVI	EXLVI < V_{DD}, 2.7 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note 2]		t_{LWAIT}		10			μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 9

LVI Circuit Timing



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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 6	Hard	Clock generator operation when power supply voltage is turned on	–	It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK and EXCLKS pins is used.	pp. 246, 247 ☐
				A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the power supply voltage reaches 1.59 V (TYP.). If the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) within 1.93 ms, the power supply oscillation stabilization time of 0 to 5.39 ms is automatically generated before reset processing.	p. 247 ☐
	Soft	Controlling high-speed system clock	X1/P121 and X2/EXCLK/P122	The X1/P121 and X2/EXCLK/P122 pins are in the I/O port mode after a reset release.	p. 248 ☐
			X1 clock	Do not change the value of EXCLK and OSCSEL while the X1 clock is operating.	p. 249 ☐
				Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS : T_A = • 40 to +125°C)).	p. 249 ☐
			External main system clock	Do not change the value of EXCLK and OSCSEL while the external main systerm clock is operating.	p. 249 ☐
				Set the external main system clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS : T_A = • 40 to +125°C)).	p. 249 ☐
			Main system clock	If the high-speed system clock is selected as the main system clock, a clock other than the high-speed system clock cannot be set as the peripheral hardware clock.	p. 250 ☐
			High-speed system clock	Be sure to confirm that MCS = 0 or CLS = 1 when setting MSTOP to 1. In addition, stop peripheral hardware that is operating on the high-speed system clock.	p. 251 ☐
			Internal high-speed oscillation clock	Be sure to confirm that MCS = 1 or CLS = 1 when setting RSTOP to 1. In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock.	p. 253 ☐
			XT1/P123, XT2/EXCLKS/ P124	The XT1/P123 and XT2/EXCLKS/P124 pins are in the I/O port mode after a reset release.	p. 254 ☐
			External clock from peripheral hardware pins	Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.	p. 254 ☐
			XT1 clock, external subsystem clock	Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.	p. 254 ☐
			Subsystem clock	Be sure to confirm that CLS = 0 when clearing OSCSELS to 0. In addition, stop the watch timer if it is operating on the subsystem clock.	p. 255 ☐
				The subsystem clock oscillation cannot be stopped using the STOP instruction.	p. 255 ☐
		Controlling internal low-speed oscillation clock	Internal low-speed oscillation clock	If “Internal low-speed oscillator cannot be stopped” is selected by the option byte, oscillation of the internal low-speed oscillation clock cannot be controlled.	p. 256 ☐