Renesas Electronics America Inc - UPD78F0531AGK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0531agk-gaj-ax

Table 4-1. Memory Bank Address Representation

Memory Bank Number	CPU Address	Flash Memory Real Address	Address Representation in Simulator and Debugger[Note 1]
Memory bank 0	08000H-0BFFFH[Note 2]	08000H-0BFFFH	08000H-0BFFFH
Memory bank 1		0C000H-0FFFFH	18000H-1BFFFH
Memory bank 2		10000H-13FFFH	28000H-2BFFFH
Memory bank 3		14000H-17FFFH	38000H-3BFFFH
Memory bank 4		18000H-1BFFFH	48000H-4BFFFH
Memory bank 5		1C000H-1FFFFH	58000H-5BFFFH

Notes 1. SM+ for 78K0, SM+ for 78K0/Kx2, and ID78K0-QB

2. Set the memory bank to be used by the memory bank select register (BANK) (see **Figure 4-3**).

For details, see the **RA78K0 Ver. 3.80 Assembler Package Operation User's Manual (U17199E)** and the **78K0 Microcontrollers Self Programming Library Type01 User's Manual (U18274E)**.

4.3 Memory Bank Select Register (BANK)

The memory bank select register (BANK) is used to select a memory bank to be used.

BANK can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears BANK to 00H.

Figure 4-3. Format of Memory Bank Select Register (BANK)

Address: FFF3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BANK	0	0	0	0	0	BANK2	BANK1	BANK0

BANK2	BANK1	BANK0	Bank setting	
			μPD78F05x6 and 78F05x6A	μPD78F05x7, 78F05x7A, 78F05x7D, and 78F05x7DA
0	0	0	Common area (32 KB) + memory bank 0 (16 KB)	
0	0	1	Common area (32 KB) + memory bank 1 (16 KB)	
0	1	0	Common area (32 KB) + memory bank 2 (16 KB)	
0	1	1	Common area (32 KB) + memory bank 3 (16 KB)	
1	0	0	Setting prohibited	Common area (32 KB) + memory bank 4 (16 KB)
1	0	1		Common area (32 KB) + memory bank 5 (16 KB)
Other than above			Setting prohibited	

Caution Be sure to change the value of the BANK register in the common area (0000H to 7FFFH). If the value of the BANK register is changed in the bank area (8000H to BFFFH), an inadvertent program loop occurs in the CPU. Therefore, never change the value of the BANK register in the bank area.

Remark x = 2 to 4

(3) Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode of the pins to which the use of an on-chip pull-up resistor has been specified in these registers. On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins, regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 5-39. Format of Pull-up Resistor Option Register (78K0/KB2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	0	0	PU01	PU00	FF30H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3, 12; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

7.6 Cautions for 16-Bit Timer/Event Counters 00 and 01

(1) Restrictions for each channel of 16-bit timer/event counter 0n

Table 7-3 shows the restrictions for each channel.

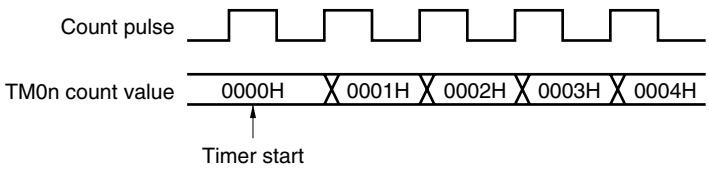
Table 7-3. Restrictions for Each Channel of 16-Bit Timer/Event Counter 0n

Operation	Restriction
As interval timer	–
As square-wave output	
As external event counter	
As clear & start mode entered by TI00n pin valid edge input	Using timer output (TO0n) is prohibited when detection of the valid edge of the TI01n pin is used. (TOC0n = 00H)
As free-running timer	–
As PPG output	0000H ≤ CP01n < CR00n ≤ FFFFH
As one-shot pulse output	Setting the same value to CR00n and CP01n is prohibited.
As pulse width measurement	Using timer output (TO0n) is prohibited (TOC0n = 00H)

(2) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM0n is started asynchronously to the count pulse.

Figure 7-60. Start Timing of TM0n Count



(3) Setting of CR00n and CR01n (clear & start mode entered upon a match between TM0n and CR00n)

Set a value other than 0000H to CR00n and CR01n (TM0n cannot count one pulse when it is used as an external event counter).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(3) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

When using the P15/TOH0 and P16/TOH1/INTP5 pins for timer output, clear PM15 and PM16 and the output latches of P15 and P16 to 0.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 9-8. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

9.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

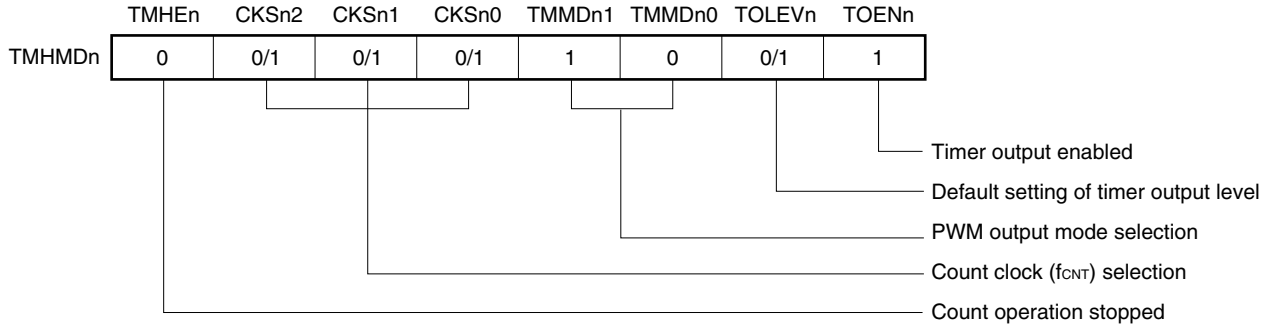
PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

Setting

<1> Set each register.

Figure 9-11. Register Setting in PWM Output Mode

(i) Setting timer H mode register n (TMHMDn)



(ii) Setting CMP0n register

- Compare value (N): Cycle setting

(iii) Setting CMP1n register

- Compare value (M): Duty setting

Remarks 1. n = 0, 1

2. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, and an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

<4> When the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output and the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP1n register to the CMP0n register. At this time, the 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

14.4 Operation of Serial Interface UART0

Serial interface UART0 has the following two modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode

14.4.1 Operation stop mode

In this mode, serial communication cannot be executed, thus reducing the power consumption. In addition, the pins can be used as ordinary port pins in this mode. To set the operation stop mode, clear bits 7, 6, and 5 (POWER0, TXE0, and RXE0) of ASIM0 to 0.

(1) Register used

The operation stop mode is set by asynchronous serial interface operation mode register 0 (ASIM0).

ASIM0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Address: FF70H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].

TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

Caution Clear POWER0 to 0 after clearing TXE0 and RXE0 to 0 to set the operation stop mode. To start the communication, set POWER0 to 1, and then set TXE0 or RXE0 to 1.

Remark To use the RxD0/SI10/P11 and TxD0/$\overline{\text{SCK10}}$/P10 pins as general-purpose port pins, see **CHAPTER 5 PORT FUNCTIONS**.

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- Error (%) = $\left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1\right) \times 100$ [%]

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 10 MHz = 10,000,000 Hz
Set value of MDL67 to MDL60 bits of BRGC6 register = 00100001B (k = 33)
Target baud rate = 153600 bps

Baud rate = 10 M / (2 × 33)
= 10000000 / (2 × 33) = 151,515 [bps]

Error = (151515/153600 − 1) × 100
= −1.357 [%]

(3) Example of setting baud rate

Table 15-5. Set Data of Baud Rate Generator

Baud Rate [bps]	f_{PRS} = 2.0 MHz				f_{PRS} = 5.0 MHz				f_{PRS} = 10.0 MHz				f_{PRS} = 20.0 MHz			
	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]
300	8H	13	301	0.16	7H	65	301	0.16	8H	65	301	0.16	9H	65	301	0.16
600	7H	13	601	0.16	6H	65	601	0.16	7H	65	601	0.16	8H	65	601	0.16
1200	6H	13	1202	0.16	5H	65	1202	0.16	6H	65	1202	0.16	7H	65	1202	0.16
2400	5H	13	2404	0.16	4H	65	2404	0.16	5H	65	2404	0.16	6H	65	2404	0.16
4800	4H	13	4808	0.16	3H	65	4808	0.16	4H	65	4808	0.16	5H	65	4808	0.16
9600	3H	13	9615	0.16	2H	65	9615	0.16	3H	65	9615	0.16	4H	65	9615	0.16
19200	2H	13	19231	0.16	1H	65	19231	0.16	2H	65	19231	0.16	3H	65	19231	0.16
24000	1H	21	23810	−0.79	3H	13	24038	0.16	4H	13	24038	0.16	5H	13	24038	0.16
31250	1H	16	31250	0	4H	5	31250	0	5H	5	31250	0	6H	5	31250	0
38400	1H	13	38462	0.16	0H	65	38462	0.16	1H	65	38462	0.16	2H	65	38462	0.16
48000	0H	21	47619	−0.79	2H	13	48077	0.16	3H	13	48077	0.16	4H	13	48077	0.16
76800	0H	13	76923	0.16	0H	33	75758	−1.36	0H	65	76923	0.16	1H	65	76923	0.16
115200	0H	9	111111	−3.55	1H	11	113636	−1.36	0H	43	116279	0.94	0H	87	114943	−0.22
153600	−	−	−	−	1H	8	156250	1.73	0H	33	151515	−1.36	1H	33	151515	−1.36
312500	−	−	−	−	0H	8	312500	0	1H	8	312500	0	2H	8	312500	0
625000	−	−	−	−	0H	4	625000	0	1H	4	625000	0	2H	4	625000	0

Remark TPS63 to TPS60: Bits 3 to 0 of clock selection register 6 (CKSR6) (setting of base clock (f_{XCLK6}))
k: Value set by MDL67 to MDL60 bits of baud rate generator control register 6 (BRGC6) (k = 4, 5, 6, ..., 255)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

(2) Serial status register 0 (CSIS0)

This is an 8-bit register used to select the base clock, control the communication operation, and indicate the status of serial interface CSIA0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction. However, rewriting CSIS0 is prohibited when bit 0 (TSF0) is 1.

Reset signal generation clears this register to 00H.

Figure 17-3. Format of Serial Status Register 0 (CSIS0) (1/2)

Address: FF91H After reset: 00H R/W[Note 1]

Symbol	7	6	5	4	3	2	1	0
CSIS0	0	CKS00[Note 2]	STBE0	BUSYE0	BUSYLV0	ERRE0	ERRF0	TSF0

CKS00	Base clock (f_W) selection[Note 3]				
		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	f_{PRS}[Note 4]	2 MHz	5 MHz	10 MHz	20 MHz[Note 5]
1	f_{PRS}/2	1 MHz	2.5 MHz	5 MHz	10 MHz

STBE0[Notes 6, 7]	Strobe output enable/disable
0	Strobe output disabled
1	Strobe output enabled

Notes 1. Bits 0 and 1 are read-only.

2. Make sure that bit 7 (CSIAE0) of the Serial Operation Mode Specification Register 0 (CSIMA0) = 0 when rewriting the CKS00 bit.

3. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when f_{PRS} = f_{XH} (XSEL = 1).)

4. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V ≤ V_{DD} < 2.7 V, the setting of CKS00 = 0 (base clock: f_{PRS}) is prohibited.

5. This is settable only if 4.0 V ≤ V_{DD} ≤ 5.5 V.

6. STBE0 is valid only in master mode.

7. When STBE0 is set to 1, two transfer clocks are consumed between byte transfers regardless of the setting of automatic data transfer interval specification register 0 (ADTI0). That is, 10 transfer clocks are used for 1-byte transfer if ADTI0 = 00H is set.

Caution Be sure to clear bit 7 to 0.

Remark f_{PRS}: Peripheral hardware clock frequency

(4) Divisor selection register 0 (BRGCA0)

This is an 8-bit register used to select the base clock divisor of CSIA0.

This register can be set by an 8-bit memory manipulation instruction. However, when bit 0 (TSF0) of serial status register 0 (CSIS0) is 1, rewriting BRGCA0 is prohibited.

Reset signal generation sets this register to 03H.

Figure 17-5. Format of Divisor Selection Register 0 (BRGCA0)

Address: FF93H After reset: 03H R/W

Symbol	7	6	5	4	3	2	1	0
BRGCA0	0	0	0	0	0	0	BRGCA01	BRGCA00

BRGCA01	BRGCA00	Selection of base clock (f_W) divisor of CSIA0[Note]						
			f_W = 1 MHz	f_W = 2 MHz	f_W = 2.5 MHz	f_W = 5 MHz	f_W = 10 MHz	f_W = 20 MHz
0	0	$f_W/6$	166.67 kHz	333.3 kHz	416.67 kHz	833.33 kHz	1.67 MHz	Setting prohibited
0	1	$f_W/2^3$	125 kHz	250 kHz	312.5 kHz	625 kHz	1.25 MHz	Setting prohibited
1	0	$f_W/2^4$	62.5 kHz	125 kHz	156.25 kHz	312.5 kHz	625 kHz	1.25 MHz
1	1	$f_W/2^5$	31.25 kHz	62.5 kHz	78.125 kHz	156.25 kHz	312.5 kHz	625 kHz

Note Set the transfer clock so as to satisfy the following conditions.

- When 4.0 V ≤ V_{DD} ≤ 5.5 V: transfer clock ≤ 1.67 MHz
- When 2.7 V ≤ V_{DD} < 4.0 V: transfer clock ≤ 833.33 kHz
- When 1.8 V ≤ V_{DD} < 2.7 V: transfer clock ≤ 555.56 kHz (Standard products and (A) grade products only)

Remark f_W: Base clock frequency selected by CKS00 bit of CSIS0 register (f_{PRS} or $f_{PRS}/2$)

f_{PRS}: Peripheral hardware clock frequency

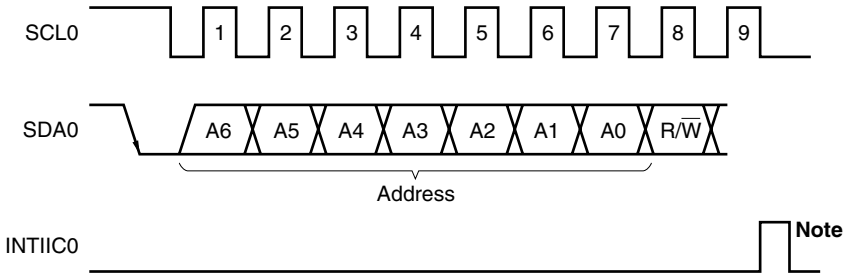
18.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in slave address register 0 (SVA0). If the address data matches the SVA0 register values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 18-14. Address



Note INTIIC0 is not issued if data other than a local address or extension code is received during slave device operation.

The slave address and the eighth bit, which specifies the transfer direction as described in **18.5.3 Transfer direction specification** below, are together written to IIC shift register 0 (IIC0) and are then output. Received addresses are written to IIC0.

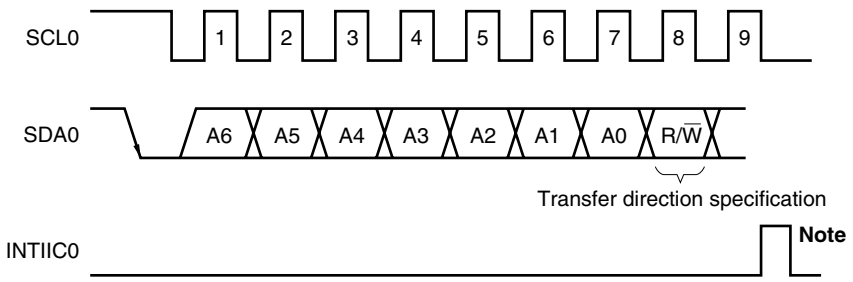
The slave address is assigned to the higher 7 bits of IIC0 register.

18.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of “0”, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of “1”, it indicates that the master device is receiving data from a slave device.

Figure 18-15. Transfer Direction Specification



Note INTIIC0 is not issued if data other than a local address or extension code is received during slave device operation.

(5) Setting STT0 and SPT0 bits (bits 1 and 0 of IICC0 register) again after they are set and before they are cleared to 0 is prohibited.

(6) When transmission is reserved, set SPIE0 bit (bit 4 of IICL0 register) to 1 so that an interrupt request is generated when the stop condition is detected. Transfer is started when communication data is written to IIC status register 0 (IICS0) after the interrupt request is generated. Unless the interrupt is generated when the stop condition is detected, the device stops in the wait state because the interrupt request is not generated when communication is started. However, it is not necessary to set SPIE0 bit to 1 when MSTS0 bit (bit 7 of IIC status register 0 (IICS0) is detected by software.

18.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the 78K0/Kx2 microcontrollers as the master in a single master system is shown below.
This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the 78K0/Kx2 microcontrollers takes part in a communication with bus released state.
This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the 78K0/Kx2 microcontrollers looses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

An example of when the 78K0/Kx2 microcontrollers is used as the I^2C bus slave is shown below.
When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIIC0 interrupt occurrence (communication waiting). When an INTIIC0 interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.
By checking the flags, necessary communication processing is performed.

Figure 20-6. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KF2)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	DUALIF0 CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	PIF7	PIF6	WTIF	KRIF	TMIF51	WTIIF	SRIF0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF1H	0	0	0	ACSIIF	TMIF011	TMIF001	CSIIF11	IICIF0 DMUIF

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

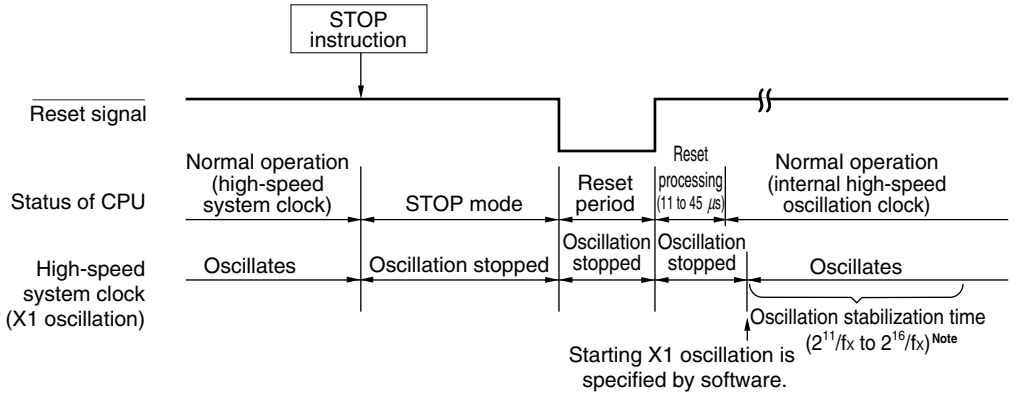
Caution Be sure to clear bits 5 to 7 of IF1H to 0.

(b) Release by reset signal generation

When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

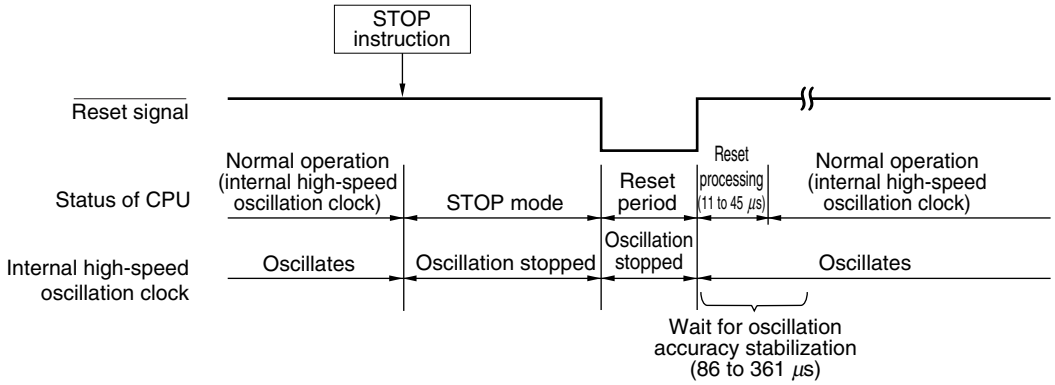
Figure 22-7. STOP Mode Release by Reset

(1) When high-speed system clock is used as CPU clock



<R> **Note** Oscillation stabilization time is not required when using the external main system clock (f_{EXCLK}) as the high-speed system clock.

(2) When internal high-speed oscillation clock is used as CPU clock



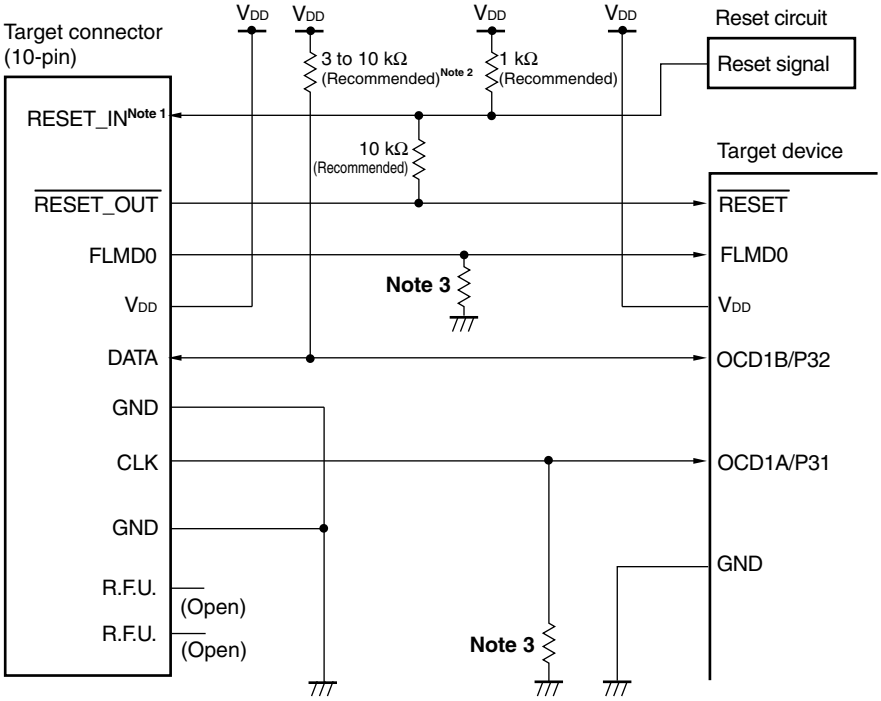
Remark fx: X1 clock oscillation frequency

Table 22-4. Operation in Response to Interrupt Request in STOP Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	STOP mode held
Reset	–	–	×	×	Reset processing

×: don't care

Figure 28-2. Connection Example of QB-MINI2 and μPD78F05xxD and 78F05xxDA (When OCD1A/P31 and OCD1B/P32 Are Used)



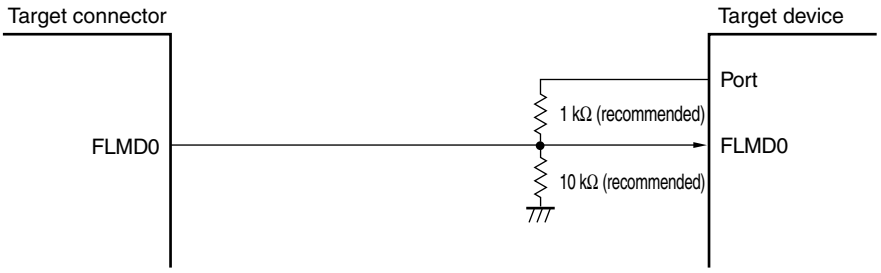
Notes 1. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **QB-MINI2 User's Manual (U18371E)**.

2. This is the processing of the pin when OCD1B/P32 is set as the input port (to prevent the pin from being left opened when not connected to QB-MINI2).

3. Make pull-down resistor 470 Ω or more (10 kΩ: recommended).

Connect the FLMD0 pin as follows when performing self programming by means of on-chip debugging.

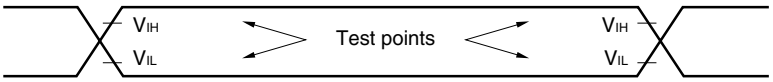
Figure 28-3. Connection of FLMD0 Pin for Self Programming by Means of On-Chip Debugging



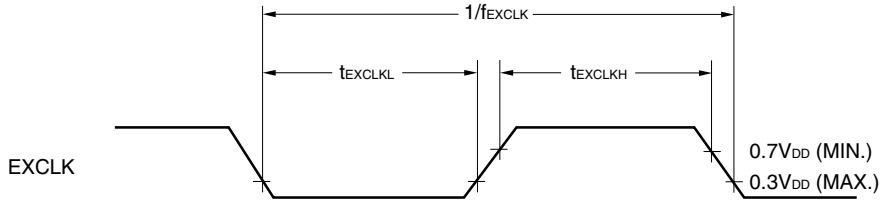
Caution When using the port that controls the FLMD0 pin, make sure that it satisfies the values of the high-level output current and FLMD0 supply voltage (minimum value: 0.8VDD) stated in CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: TA = –40 to +125°C).

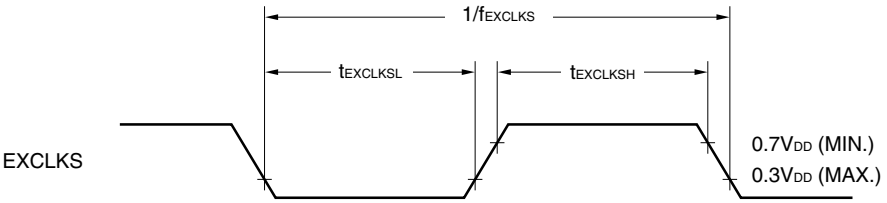
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

AC Timing Test Points

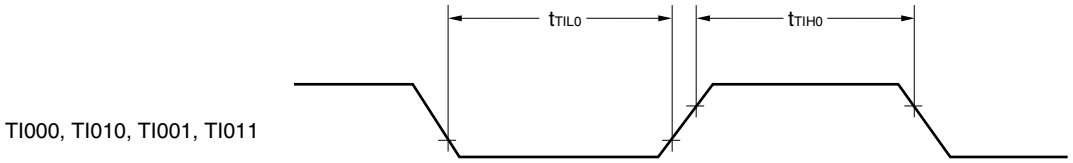


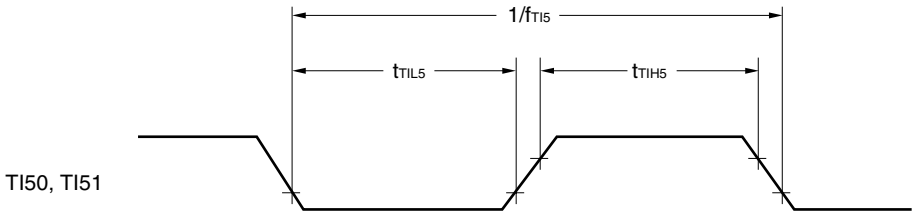
External Main System Clock Timing, External Subsystem Clock Timing



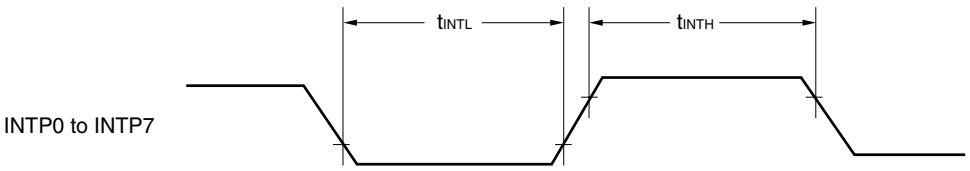


TI Timing



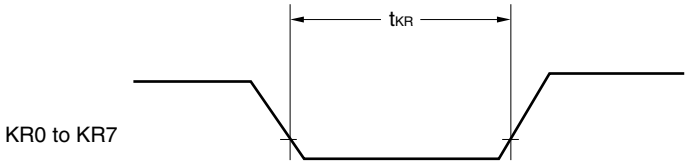


Interrupt Request Input Timing

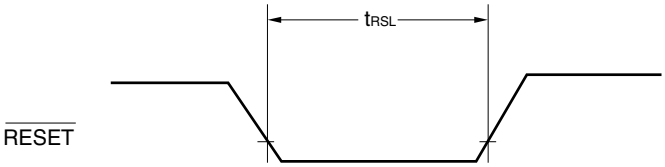


Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	−10	mA
		Total of all pins −80 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	−25	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P64 to P67, P70 to P77	−55	mA
		Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
		Per pin	P121 to P124	−1	mA
		Total of all pins		−4	mA
Output current, low	I_{OL}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P130, P140 to P145	30	mA
		Total of all pins 200 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	60	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P60 to P67, P70 to P77	140	mA
		Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
		Per pin	P121 to P124	4	mA
		Total of all pins		10	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Cautions 1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Non-port functions

Port		78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
		30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Power supply, ground		V_{DD}, EV_{DD}[Note 1], V_{SS}, EV_{SS}[Note 1], AV_{REF}, AV_{SS}	V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, V_{SS}, EV_{SS}, AV_{REF}, AV_{SS}	
Regulator		REGC						
Reset		$\overline{\text{RESET}}$						
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK, EXCLKS					
Writing to flash memory		FLMD0						
Interrupt		INTP0 to INTP5			INTP0 to INTP6		INTP0 to INTP7	
Key interrupt		–	KR0, KR1	KR0 to KR3		KR0 to KR7		
Timer	TM00	TI000, TI010, TO00						
	TM01	–					TI001[Note 2], TI011[Note 2], TO01[Note 2]	
	TM50	TI50, TO50						
	TM51	TI51, TO51						
	TMH0	TOH0						
	TMH1	TOH1						
Serial interface	UART0	RxD0, TxD0						
	UART6	RxD6, TxD6						
	IIC0	SCL0, SDA0	SCL0, SDA0, EXSCL0					
	CSI10	$\overline{\text{SCK10}}$, SI10, SO10						
	CSI11	–					$\overline{\text{SCK11}}$[Note 2], SI11[Note 2], SO11[Note 2], $\overline{\text{SSI11}}$[Note 2]	
	CSIA0	–						$\overline{\text{SCKA0}}$, SIA0, SOA0, BUSY0, STB0
A/D converter		ANI0 to ANI3	ANI0 to ANI5	ANI0 to ANI7				
Clock output		–			PCL			
Buzzer output		–					BUZ	
Low-voltage detector (LVI)		EXLVI						

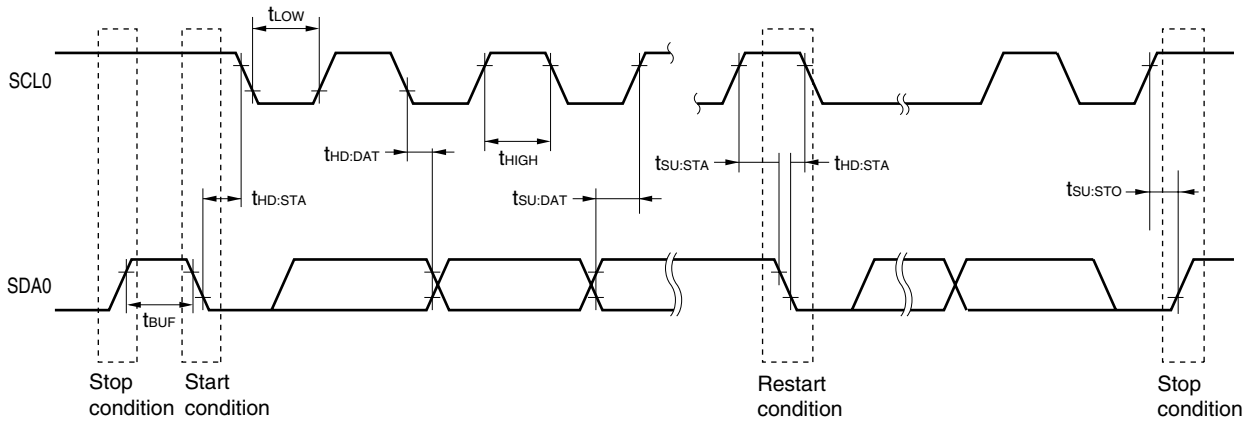
Notes 1. This is not mounted onto 30-pin products.

2. This is not mounted onto the 78K0/KE2 products whose flash memory is less than 32 KB.

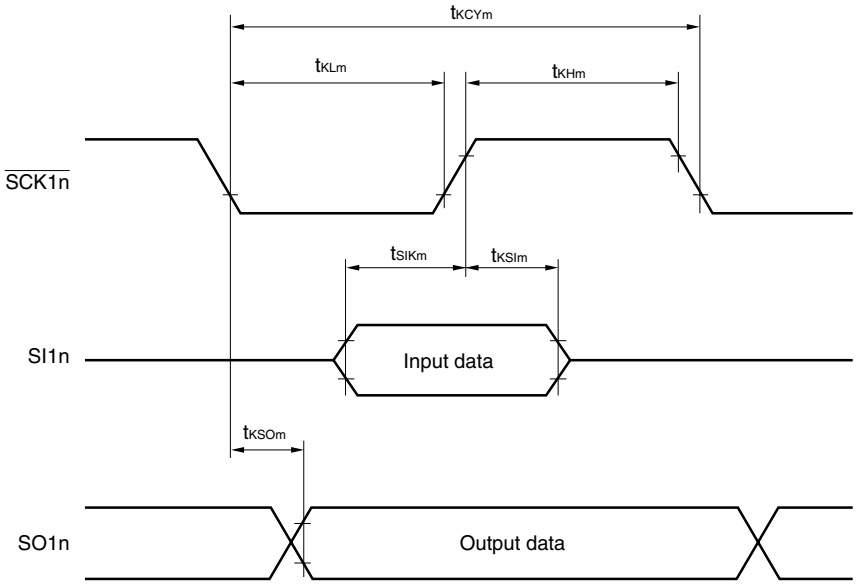
Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Serial Transfer Timing (1/2)

IIC0:



CSI1n:



Remark m = 1, 2
n = 0, 1

(11/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 9	Soft	8-bit timers H0, H1	TMCYC1: 8-bit timer H carrier register 1	Do not rewrite RMC1 when TMHE = 1. However, TMCYC1 can be refreshed (the same value is written).	p. 371 ☐
	Hard		PWM output	The set value of the CMP1n register can be changed while the timer counter is operating. However, this takes a duration of three operating clocks (signal selected by the CKSn2 to CKSn0 bits of the TMHMDn register) from when the value of the CMP1n register is changed until the value is transferred to the register.	p. 377 ☐
	Soft			Be sure to set the CMP1n register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMP1n register).	p. 377 ☐
				Make sure that the CMP1n register setting value (M) and CMP0n register setting value (N) are within the following range. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH	p. 377 ☐
			Carrier generator (8-bit timer H1 only)	Do not rewrite the NRZB1 bit again until at least the second clock after it has been rewritten, or else the transfer from the NRZB1 bit to the NRZ1 bit is not guaranteed.	p. 383 ☐
				When the 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated at the timing of <1>. When the 8-bit timer/event counter 51 is used in a mode other than the carrier generator mode, the timing of the interrupt generation differs.	p. 383 ☐
				Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).	p. 385 ☐
				Set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.	p. 385 ☐
				Set the values of the CMP01 and CMP11 registers in a range of 01H to FFH.	p. 385 ☐
				The set value of the CMP11 register can be changed while the timer counter is operating. However, it takes the duration of three operating clocks (signal selected by the CKS12 to CKS10 bits of the TMHMD1 register) since the value of the CMP11 register has been changed until the value is transferred to the register.	p. 385 ☐
				Be sure to set the RMC1 bit before the count operation is started.	p. 385 ☐
Chapter 10	Soft	Watch timer	WTM: Watch timer operation mode register	Do not change the count clock and interval time (by setting bits 4 to 7 (WTM4 to WTM7) of WTM) during watch timer operation.	p. 393 ☐
	Hard		Interrupt request	When operation of the watch timer and 5-bit counter is enabled by the watch timer mode control register (WTM) (by setting bits 0 (WTM0) and 1 (WTM1) of WTM to 1), the interval until the first interrupt request signal (INTWT) is generated after the register is set does not exactly match the specification made with bits 2 and 3 (WTM2, WTM3) of WTM. Subsequently, however, the INTWT signal is generated at the specified intervals.	p. 395 ☐
Chapter 11	Soft	Watchdog timer	WDTE: Watchdog timer enable register	If a value other than ACH is written to WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.	p. 398 ☐
				If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.	p. 398 ☐
				The value read from WDTE is 9AH/1AH (this differs from the written value (ACH)).	p. 398 ☐
			Operation control	The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.	p. 399 ☐
				If the watchdog timer is cleared by writing “ACH” to WDTE, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f_{RL} seconds.	p. 399 ☐