Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

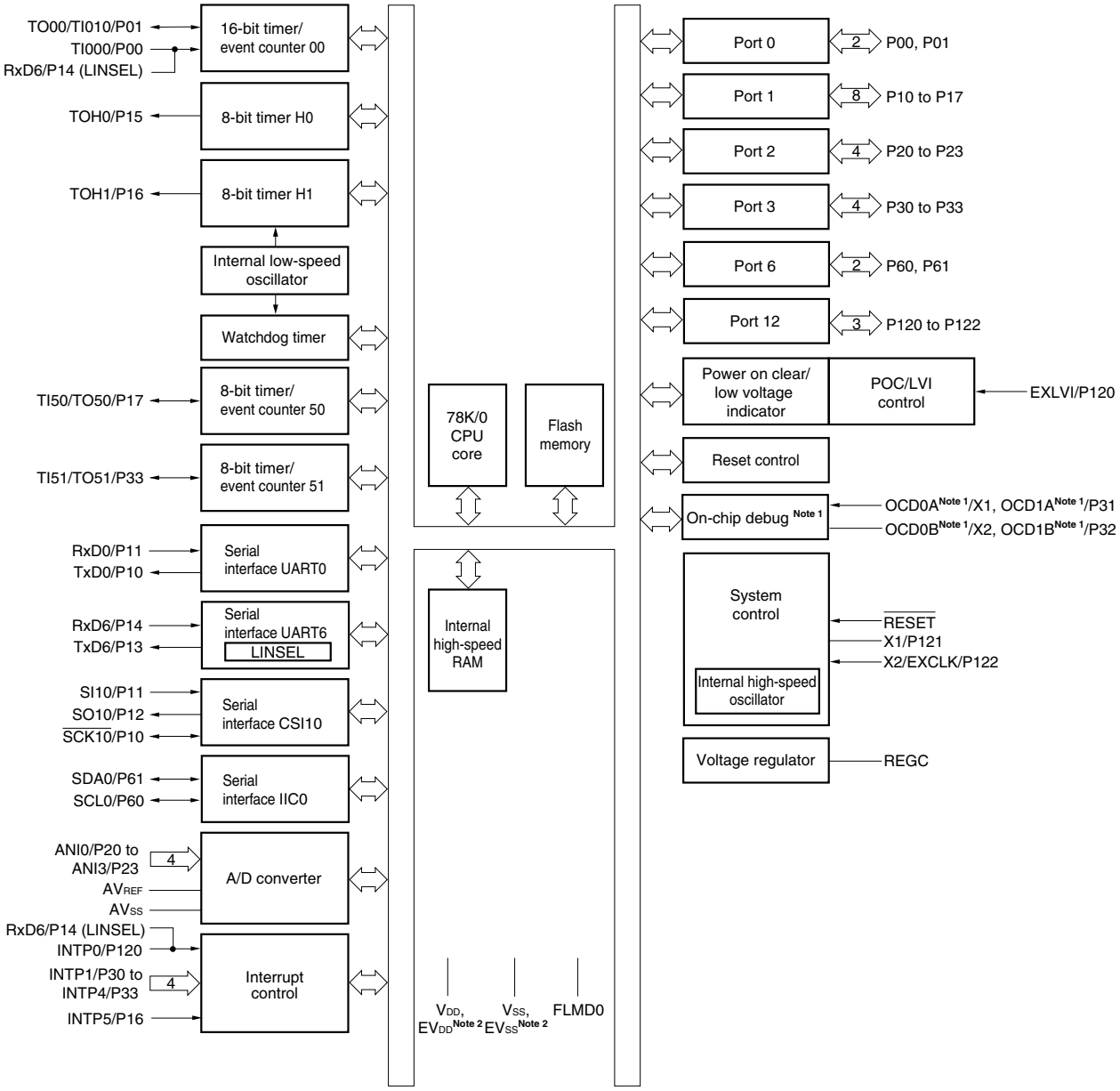
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFLGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0532afc-aa1-a

1.7 Block Diagram

1.7.1 78K0/KB2



Notes 1. Available only in the products with on-chip debug function.

2. Available only in the 36-pin products.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuits and the recommended connections of unused pins.
See **Figure 2-1** for the configuration of the I/O circuit of each type.

Remark The pins mounted depend on the product. See **1.5 Ordering Information (Top View)** and **2.1 Pin Function List**.

Table 2-3. Pin I/O Circuit Types (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000	5-AQ	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P01/TI010/TO00			
P02/SO11	5-AG		
P03/SI11	**Note 1**		
P04/$\overline{SCK11}$			
P05/TI001/$\overline{SSI11}$			
P06/TI011/TO01			
P10/$\overline{SCK10}$/TxD0	5-AQ		
P11/SI10/RxD0			
P12/SO10	5-AG		
P13/TxD6			
P14/RxD6	5-AQ		
P15/TOH0	5-AG		
P16/TOH1/INTP5	5-AQ		
P17/TI50/TO50			
ANI0/P20 to ANI7/P27[Note 2]	11-G		< Digital input setting and analog input setting> Independently connect to AV_{REF} or AV_{SS} via a resistor. <Digital output setting> Leave open.

Notes 1. "5-AG" type: 78K0/KE2 whose flash memory is less than 32 KB and 78K0/KD2
"5-AQ" type: 78K0/KE2 whose flash memory is at least 48 KB and 78K0/KF2
(Products other than the above are not mounted with P03 to P06.)

2. ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Table 2-3. Pin I/O Circuit Types (3/3)

	Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
	P140/PCL/INTP6	5-AQ	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
	P141/BUZ/BUSY0/INTP7			
	P142/$\overline{SCKA0}$			
	P143/SIA0			
	P144/SOA0	5-AG		
	P145/STB0			
<R>	AV_{REF}	–	–	<When one or more of P20 to P27 are set as a digital port> Make this pin the same potential as EV_{DD} and V_{DD}. <When all of P20 to P27 are set as analog ports> Make this pin to have a potential where 1.8 V ≤ AV_{REF} ≤ V_{DD}.
<R>	AV_{SS}	–	–	Make this pin the same potential as the EV_{SS} and V_{SS}.
	FLMD0	38-A	–	Connect to EV_{SS} or V_{SS}[Note].
<R>	$\overline{RESET}$	2	Input	Connect directly to EV_{DD} or via a resistor.
<R>	REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF).

Note FLMD0 is a pin that is used to write data to the flash memory. To rewrite the data of the flash memory on-board, connect this pin to EV_{SS} or V_{SS} via a resistor (10 kΩ: recommended). The same applies when executing on-chip debugging with a product with an on-chip debug function (μPD78F05xxD and 78F05xxDA).

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 3-15. Correspondence Between Data Memory and Addressing
(μPD78F0503, 78F0503A, 78F0513, 78F0513A, 78F0523, 78F0523A, 78F0533, 78F0533A, 78F0503D, 78F0503DA, 78F0513D, and 78F0513DA)

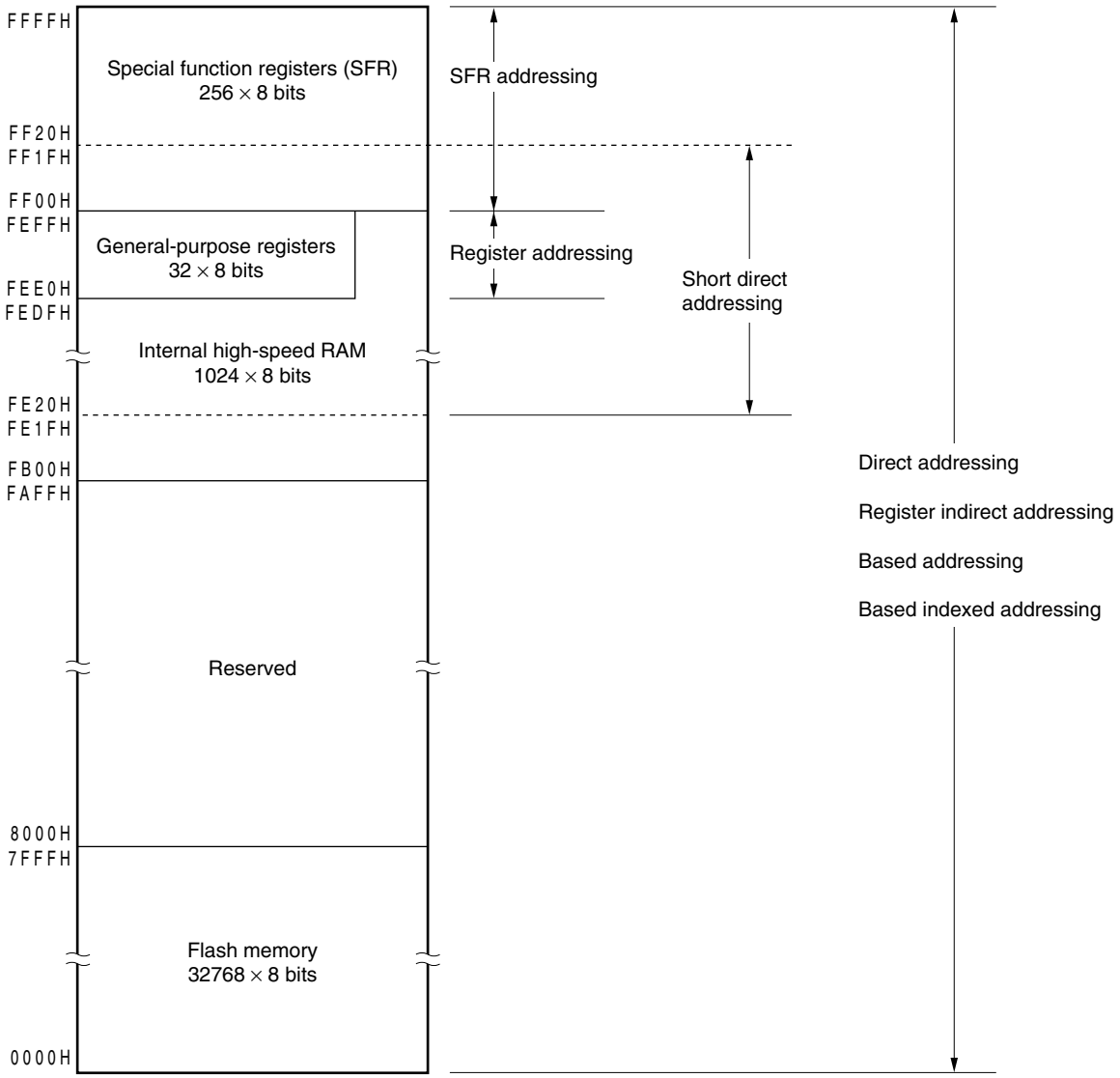
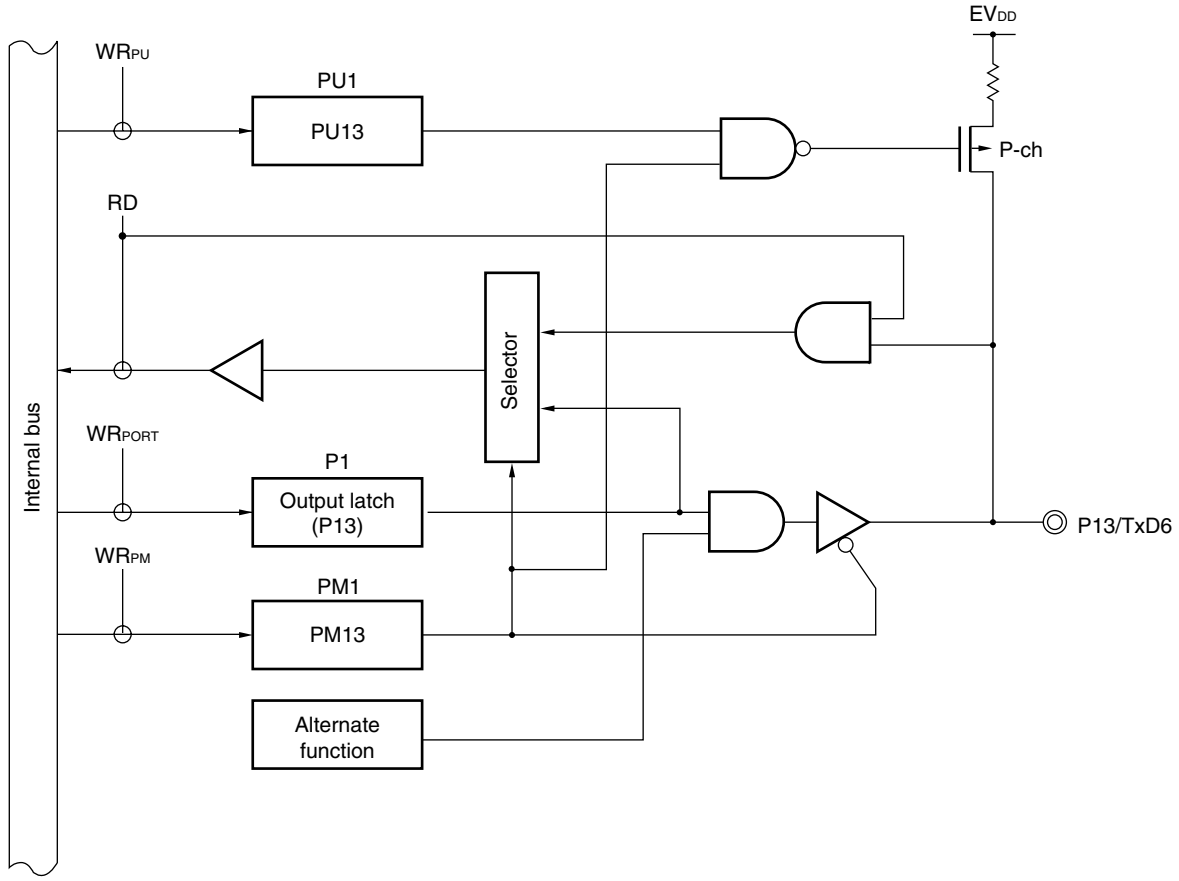


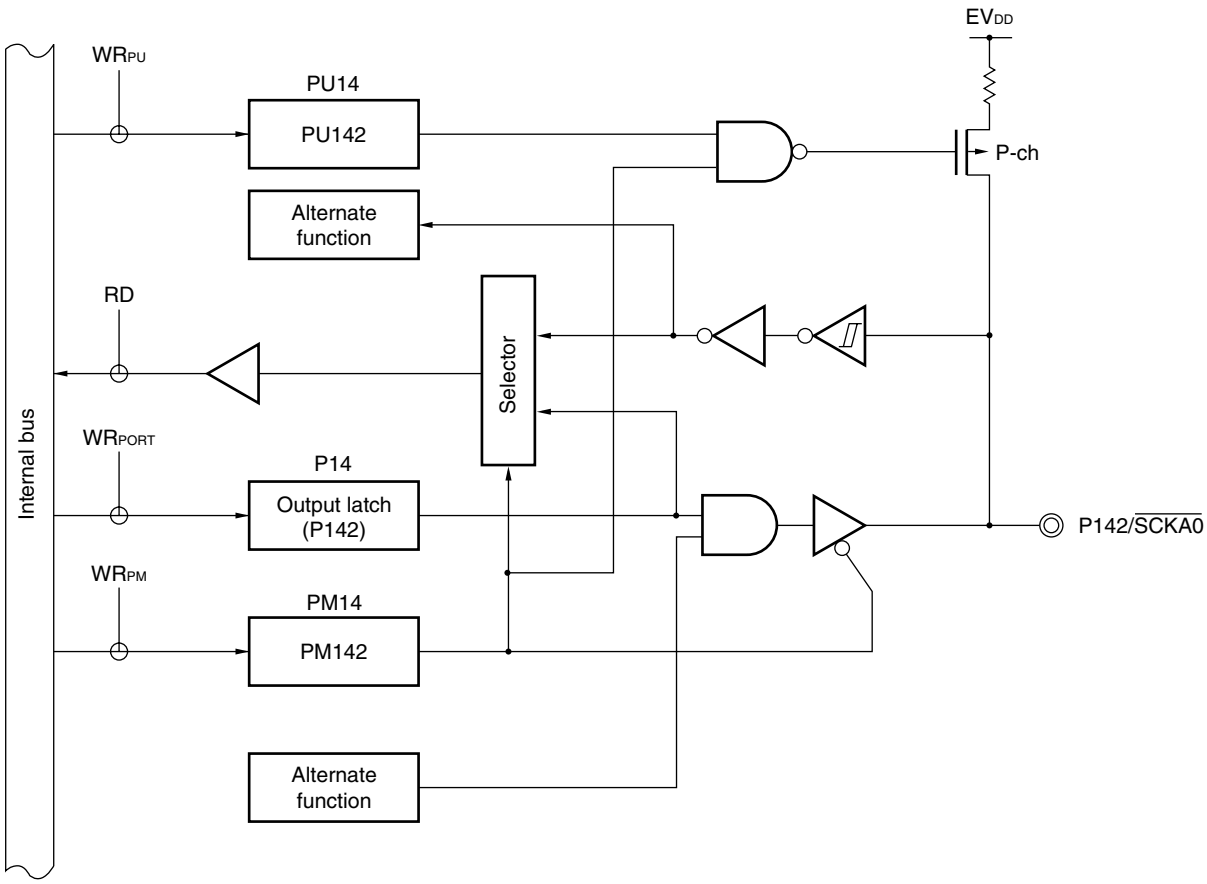
Figure 5-10. Block Diagram of P13



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

Figure 5-26. Block Diagram of P142



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

5.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

5.4.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

5.4.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

5.4.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change.
The data of the output latch is cleared when a reset signal is generated.

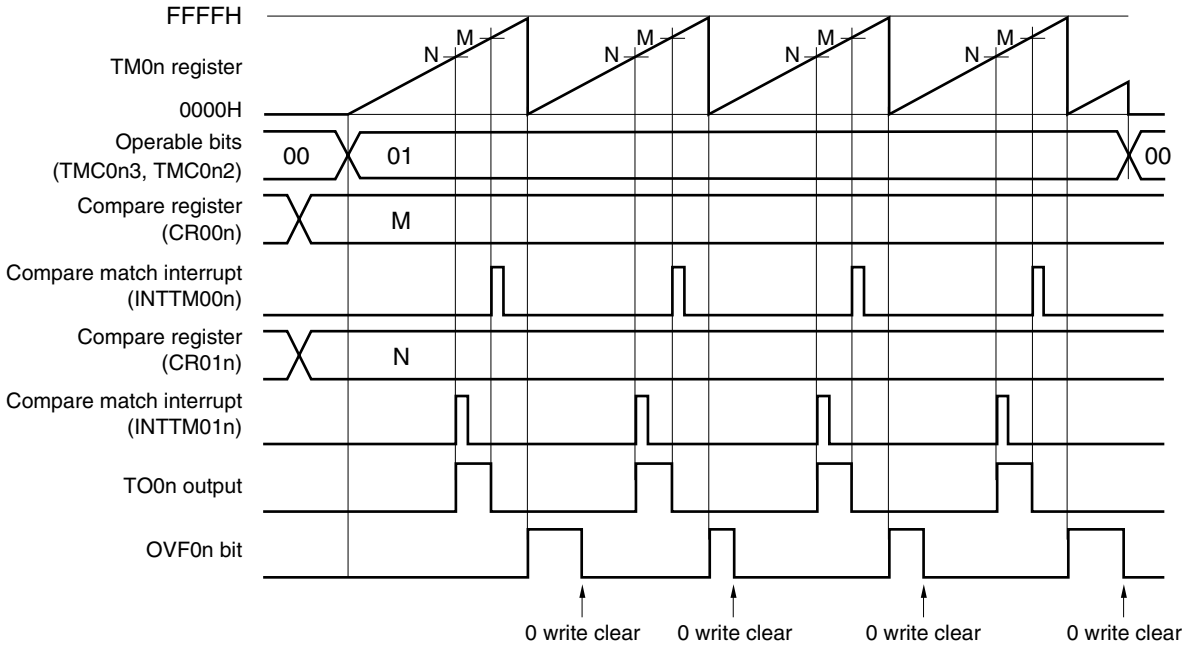
5.5 Settings of Port Mode Register and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the port mode register and output latch as shown in Table 5-6.

Remark The port pins mounted depend on the product. See **Table 5-3. Port Functions**.

Figure 7-38. Timing Example of Free-Running Timer Mode
(CR00n: Compare Register, CR01n: Compare Register)

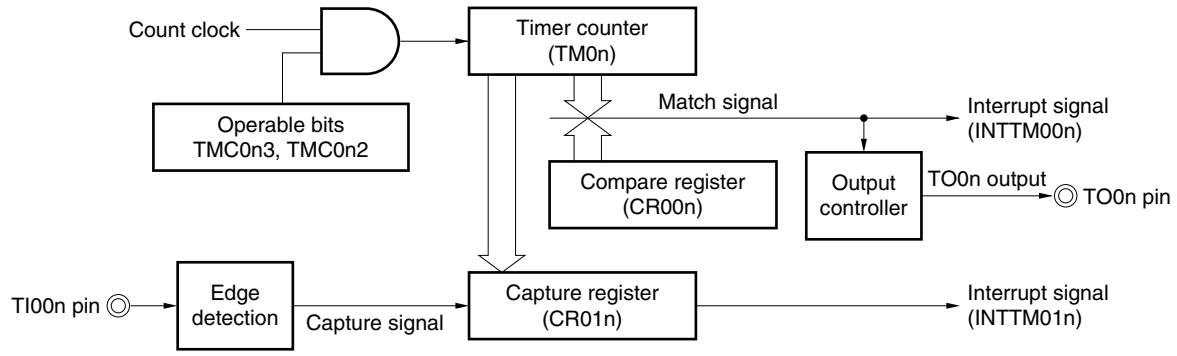
• TOC0n = 13H, PRM0n = 00H, CRC0n = 00H, TMC0n = 04H



This is an application example where two compare registers are used in the free-running timer mode.
The TO0n output level is reversed each time the count value of TM0n matches the set value of CR00n or CR01n. When the count value matches the register value, the INTTM00n or INTTM01n signal is generated.

(2) Free-running timer mode operation
(CR00n: compare register, CR01n: capture register)

Figure 7-39. Block Diagram of Free-Running Timer Mode
(CR00n: Compare Register, CR01n: Capture Register)



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(7) Operation of OVF0n flag

(a) Setting OVF0n flag (1)

The OVF0n flag is set to 1 in the following case, as well as when TM0n overflows.

Select the clear & start mode entered upon a match between TM0n and CR00n.

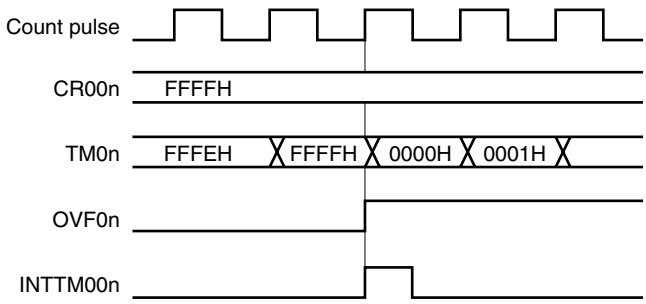
↓

Set CR00n to FFFFH.

↓

When TM0n matches CR00n and TM0n is cleared from FFFFH to 0000H

Figure 7-62. Operation Timing of OVF0n Flag



(b) Clearing OVF0n flag

Even if the OVF0n flag is cleared to 0 after TM0n overflows and before the next count clock is counted (before the value of TM0n becomes 0001H), it is set to 1 again and clearing is invalid.

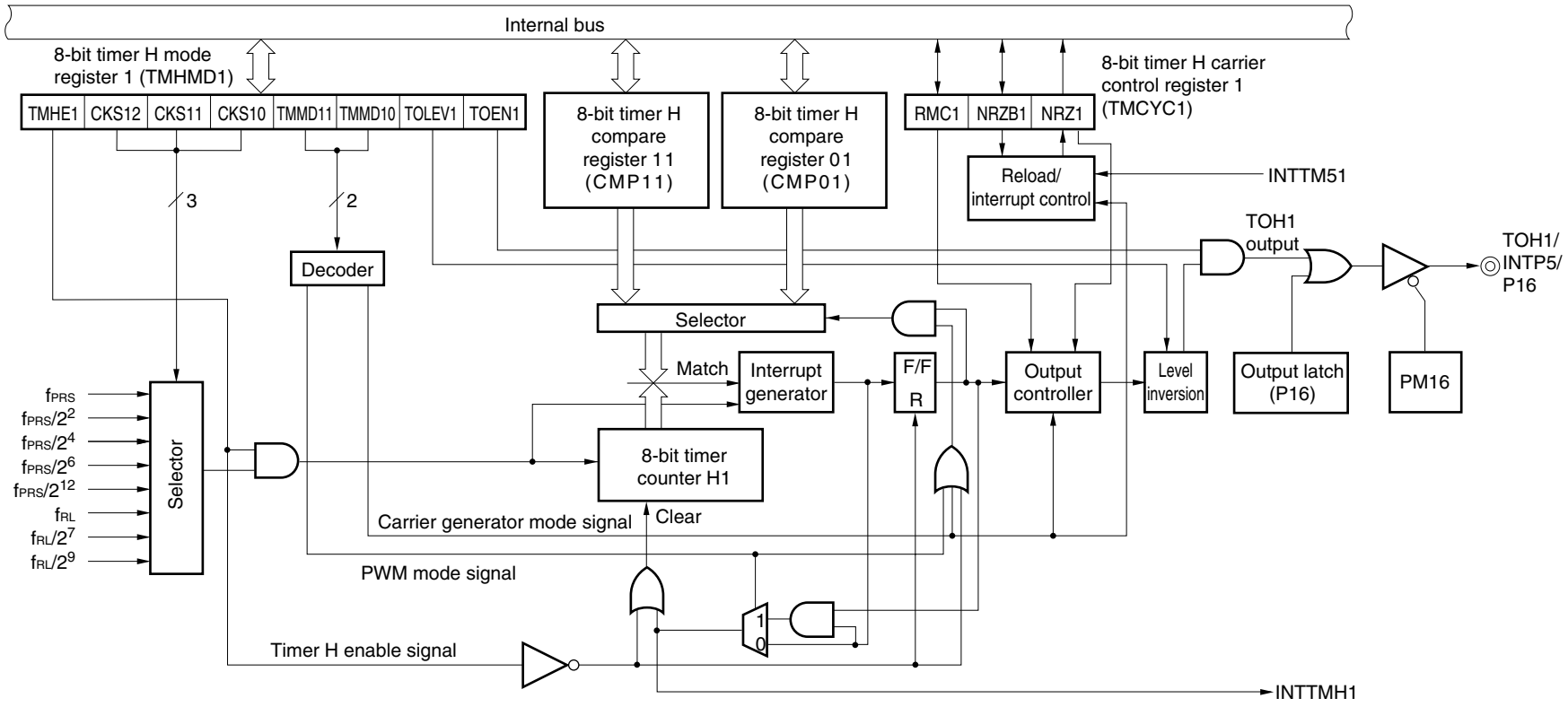
(8) One-shot pulse output

One-shot pulse output operates correctly in the free-running timer mode or the clear & start mode entered by the TI00n pin valid edge. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM0n and CR00n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 9-2. Block Diagram of 8-Bit Timer H1



10.2 Configuration of Watch Timer

The watch timer includes the following hardware.

Table 10-3. Watch Timer Configuration

Item	Configuration
Counter	5 bits × 1
Prescaler	11 bits × 1
Control register	Watch timer operation mode register (WTM)

10.3 Register Controlling Watch Timer

The watch timer is controlled by the watch timer operation mode register (WTM).

- **Watch timer operation mode register (WTM)**
  This register sets the watch timer count clock, enables/disables operation, prescaler interval time, and 5-bit counter operation control.
  WTM is set by a 1-bit or 8-bit memory manipulation instruction.
  Reset signal generation clears WTM to 00H.

11.4 Operation of Watchdog Timer

11.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (0080H).

   - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (0080H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 26**).

WDTON	Operation Control of Watchdog Timer Counter/Illegal Access Detection
0	Counter operation disabled (counting stopped after reset), illegal access detection operation disabled
1	Counter operation enabled (counting started after reset), illegal access detection operation enabled

   - Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (0080H) (for details, see **11.4.2** and **CHAPTER 26**).
   - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (0080H) (for details, see **11.4.3** and **CHAPTER 26**).

2. After a reset release, the watchdog timer starts counting.
3. By writing “ACH” to WDTE after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
4. After that, write WDTE the second time or later after a reset release during the window open period. If WDTE is written during a window close period, an internal reset signal is generated.
5. If the overflow time expires without “ACH” written to WDTE, an internal reset signal is generated.
   A internal reset signal is generated in the following cases.

   - If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
   - If data other than “ACH” is written to WDTE
   - If the instruction is fetched from an area not set by the IMS and IXS registers (detection of an invalid check during a CPU program loop)
   - If the CPU accesses an area not set by the IMS and IXS registers (excluding FB00H to FFCFH and FFE0H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

Cautions 1. The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.

2. If the watchdog timer is cleared by writing “ACH” to WDTE, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f_{RL} seconds.

3. The watchdog timer can be cleared immediately before the count value overflows (FFFFH).

(4) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark ANI0 to ANI3: 78K0/KB2
ANI0 to ANI5: 38-pin products of the 78K0/KC2
ANI0 to ANI7: Products other than above

Figure 13-8. Format of Analog Input Channel Specification Register (ADS)

Address: FF29H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

Products other than the right / 38-pin products of KC2 / KB2

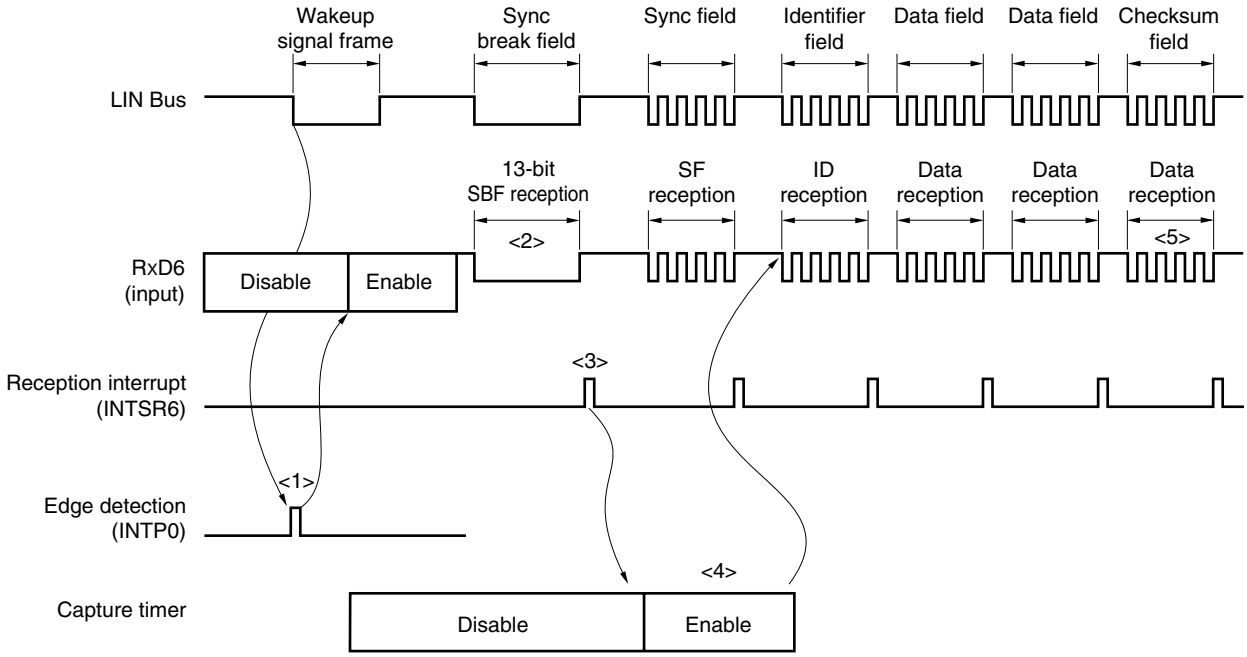
ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Note 1 (Products other than the right)
Note 1 (38-pin products of KC2)
Note 2 (38-pin products of KC2)
Note 1 (KB2)
Note 2 (KB2)

Notes 1. Setting permitted
2. Setting prohibited

Cautions 1. Be sure to clear bits 3 to 7 to "0".
2 Set a channel to be used for A/D conversion in the input mode by using port mode register 2 (PM2).
3. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

Figure 15-2. LIN Reception Operation



Reception processing is as follows.

<1> The wakeup signal is detected at the edge of the pin, and enables UART6 and sets the SBF reception mode.

<2> Reception continues until the STOP bit is detected. When an SBF with low-level data of 11 bits or more has been detected, it is assumed that SBF reception has been completed correctly, and an interrupt signal is output. If an SBF with low-level data of less than 11 bits has been detected, it is assumed that an SBF reception error has occurred. The interrupt signal is not output and the SBF reception mode is restored.

<3> If SBF reception has been completed correctly, an interrupt signal is output. Start 16-bit timer/event counter 00 by the SBF reception end interrupt servicing and measure the bit interval (pulse width) of the sync field (see **7.4.8 Pulse width measurement operation**). Detection of errors OVE6, PE6, and FE6 is suppressed, and error detection processing of UART communication and data transfer of the shift register and RXB6 is not performed. The shift register holds the reset value FFH.

<4> Calculate the baud rate error from the bit interval of the sync field, disable UART6 after SF reception, and then re-set baud rate generator control register 6 (BRGC6).

<5> Distinguish the checksum field by software. Also perform processing by software to initialize UART6 after reception of the checksum field and to set the SBF reception mode again.

Figure 15-3 shows the port configuration for LIN reception operation.

The wakeup signal transmitted from the LIN master is received by detecting the edge of the external interrupt (INTP0). The length of the sync field transmitted from the LIN master can be measured using the external event capture operation of 16-bit timer/event counter 00, and the baud rate error can be calculated.

The input source of the reception port input (RxD6) can be input to the external interrupt (INTP0) and 16-bit timer/event counter 00 by port input switch control (ISC0/ISC1), without connecting RxD6 and INTP0/TI000 externally.

(c) Repeat transmission mode

In this mode, data stored in the internal buffer RAM is transmitted repeatedly.

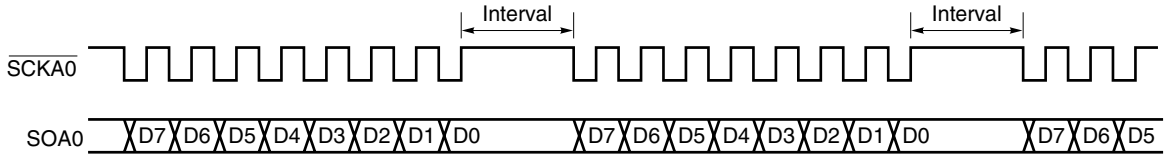
Serial communication is started when bit 0 (ATSTA0) of serial trigger register 0 (CSIT0) is set to 1 while bit 7 (CSIAE0), bit 6 (ATE0), bit 5 (ATM0), and bit 3 (TXEA0) of serial operation mode specification register 0 (CSIMA0) are set to 1.

Unlike the automatic transmission mode, after the number of setting bytes has been transmitted, the interrupt request flag (ACSIIF) is not set, automatic data transfer address count register 0 (ADTC0) is reset to 0, and the internal buffer RAM contents are transmitted again.

When a reception operation, busy control and strobe control are not performed, the SIA0/P143, BUSY0/BUZ/INTP7/P141, and STB0/P145 pins can be used as ordinary I/O port pins.

The example of the repeat transmission mode operation timing is shown in Figure 17-19, and the operation flowchart in Figure 17-20.

Figure 17-19. Example of Repeat Transmission Mode Operation Timing



Cautions 1. Because, in the repeat transmission mode, a read is performed on the buffer RAM after the transmission of one byte, the interval is included in the period up to the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the interval is dependent upon automatic data transfer interval specification register 0 (ADTI0) and the set values of bits 5 and 4 (STBE0, BUSYE0) of serial status register 0 (CSIS0) (see (5) Automatic transmit/receive interval time).

2. If an access to the buffer RAM by the CPU conflicts with an access to the buffer RAM by serial interface CSIA0 during the interval period, the interval time specified by automatic data transfer interval specification register 0 (ADTI0) may be extended.

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM0 bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM0 bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- Writing data to IIC shift register 0 (IIC0)
- Setting bit 5 (WREL0) of IIC control register 0 (IICC0) (canceling wait)
- Setting bit 1 (STT0) of IIC0 register (generating start condition)[Note]
- Setting bit 0 (SPT0) of IIC0 register (generating stop condition)[Note]

Note Master only.

When an 8-clock wait has been selected (WTIM0 = 0), the presence/absence of $\overline{\text{ACK}}$ generation must be determined prior to wait cancellation.

(5) Stop condition detection

INTIIC0 is generated when a stop condition is detected (only when SPIE0 = 1).

18.5.9 Address match detection method

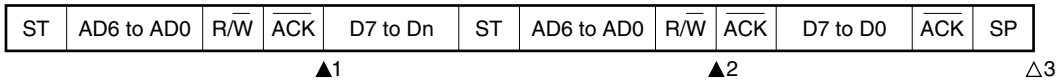
In I^2C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match can be detected automatically by hardware. An interrupt request (INTIIC0) occurs when a local address has been set to slave address register 0 (SVA0) and when the address set to SVA0 matches the slave address sent by the master device, or when an extension code has been received.

18.5.10 Error detection

In I^2C bus mode, the status of the serial data bus (SDA0) during data transmission is captured by IIC shift register 0 (IIC0) of the transmitting device, so the IIC0 data prior to transmission can be compared with the transmitted IIC0 data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

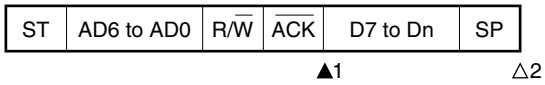
(ii) Extension code



▲1: IICS0 = 1000×110B
▲2: IICS0 = 01100010B
Sets LREL0 = 1 by software
△3: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care
n = 6 to 0

(e) When loss occurs due to stop condition during data transfer



▲1: IICS0 = 10000110B
△2: IICS0 = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care
n = 6 to 0

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

DC Characteristics (4/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		3.2	5.5	mA
				Resonator connection		4.5	6.9	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		1.6	2.8	mA
				Resonator connection		2.3	3.9	mA
			f_{XH} = 10 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		1.5	2.7	mA
				Resonator connection		2.2	3.2	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.9	1.6	mA
				Resonator connection		1.3	2.0	mA
			f_{XH} = 5 MHz, V_{DD} = 2.0 V [Notes 2, 3]	Square wave input		0.7	1.4	mA
				Resonator connection		1.0	1.6	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			1.4	2.5	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		6	25	μA
				Resonator connection		15	30	μA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		0.8	2.6	mA
				Resonator connection		2.0	4.4	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		0.4	1.3	mA
				Resonator connection		1.0	2.4	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.2	0.65	mA
				Resonator connection		0.5	1.1	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			0.4	1.2	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		3.0	22	μA
				Resonator connection		12	25	μA
	I_{DD3}[Note 6]	STOP mode				1	20	μA
			T_A = −40 to +70 °C			1	10	μA
A/D converter operating current	I_{ADC}[Note 7]	2.3 V ≤ AV_{REF} ≤ V_{DD}, ADCS = 1				0.86	1.9	mA
Watchdog timer operating current	I_{WDT}[Note 8]	During 240 kHz internal low-speed oscillation clock operation				5	10	μA
LVI operating current	I_{LVI}[Note 9]					9	18	μA

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or external subsystem clock frequency)

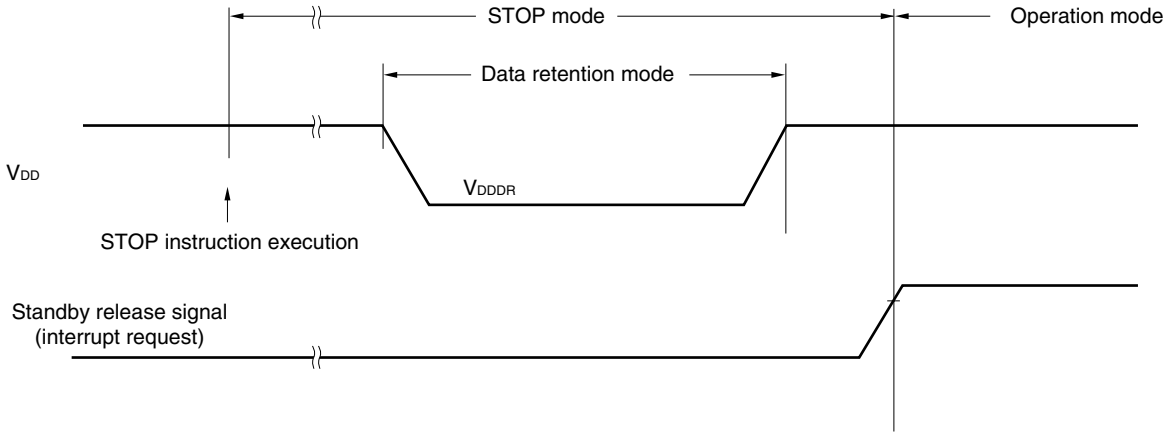
(Notes on next page)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Note The part numbers of the exchange adapter, space adapter, YQ connector, mount adapter, and target connector and the packages of the target device are described below.

Package		Exchange Adapter	Space Adapter	YQ Connector	Mount Adapter	Target Connector
78K0/KB2	30-pin plastic SSOP (MC-5A4 and MC-CAB types)	QB-30MC-EA-02T	QB-30MC-YS-01T	QB-30MC-YQ-01T	QB-30MC-HQ-01T	QB-30MC-NQ-01T
	36-pin plastic FLGA (FC-AA3 type)	QB-36FC-EA-01T	None	None	None	QB-36FC-NQ-01T
78K0/KC2	38-pin plastic SSOP (MC-GAA type)	QB-38MC-EA-01T	QB-38MC-YQ-01T	QB-38MC-YQ-01T	QB-38MC-HQ-01T	QB-38MC-NQ-01T
	44-pin plastic LQFP (GB-UES and GB-GAF types)	QB-44GB-EA-03T	QB-44GB-YS-01T	QB-44GB-YQ-01T	QB-44GB-HQ-01T	QB-44GB-NQ-01T
	48-pin plastic LQFP (GA-8EU and GA-GAM types)	QB-48GA-EA-02T	QB-48GA-YS-01T	QB-48GA-YQ-01T	QB-48GA-HQ-01T	QB-48GA-NQ-01T
78K0/KD2	52-pin plastic LQFP (GB-UET and GB-GAG types)	QB-52GB-EA-02T	QB-52GB-YS-01T	QB-52GB-YQ-01T	QB-52GB-HQ-01T	QB-52GB-NQ-01T
78K0/KE2	64-pin plastic LQFP (GB-UEU and GB-GAH types)	QB-64GB-EA-04T	QB-64GB-YS-01T	QB-64GB-YQ-01T	QB-64GB-HQ-01T	QB-64GB-NQ-01T
	64-pin plastic LQFP (GC-UBS and GC-GAL types)	QB-64GC-EA-03T	QB-64GC-YS-01T	QB-64GC-YQ-01T	QB-64GC-HQ-01T	QB-64GC-NQ-01T
	64-pin plastic LQFP (GK-UET and GK-GAJ types)	QB-64GK-EA-04T	QB-64GK-YS-01T	QB-64GK-YQ-01T	QB-64GK-HQ-01T	QB-64GK-NQ-01T
	64-pin plastic TQFP (GA-9EV and GA-HAB types)	QB-64GA-EA-01T	QB-64GA-YS-01T	QB-64GA-YQ-01T	QB-64GA-HQ-01T	QB-64GA-NQ-01T
	64-pin plastic FLGA (FC-AA1 type)	QB-64FC-EA-01T	None	None	None	QB-64FC-NQ-01T
78K0/KF2	80-pin plastic LQFP (GC-UBT and GC-GAD types)	QB-80GC-EA-01T	QB-80GC-YS-01T	QB-80GC-YQ-01T	QB-80GC-HQ-01T	QB-80GC-NQ-01T
	80-pin plastic LQFP (GK-8EU and GK-GAK type)	QB-80GK-EA-01T	QB-80GK-YS-01T	QB-80GK-YQ-01T	QB-80GK-HQ-01T	QB-80GK-NQ-01T