Renesas Electronics America Inc - UPD78F0532AGB-GAH-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0532agb-gah-ax

(1) Conventional-specification products (μPD78F05xx and 78F05xxD) (3/3)

<4> When high-speed system clock (X1 oscillation or external clock input) is used and entry RAM is located in short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		34/f_{CPU}			
Initialize library		49/f_{CPU} + 224.6875			
Mode check library		35/f_{CPU} + 113.625		29/f_{CPU} + 113.625	
Block blank check library		174/f_{CPU} + 6120.9375		134/f_{CPU} + 6120.9375	
Block erase library		174/f_{CPU} + 30820.75	174/f_{CPU} + 298675	134/f_{CPU} + 30820.75	134/f_{CPU} + 298675
Word write library		318 (321)/f_{CPU} + 383	318 (321)/f_{CPU} + 1230.5	262 (265)/f_{CPU} + 383	262 (265)/f_{CPU} + 1230.5
Block verify library		174/f_{CPU} + 13175.4375		134/f_{CPU} + 13175.4375	
Self programming end library		34/f_{CPU}			
Get information library	Option value: 03H	171 (172)/f_{CPU} + 171.3125		129 (130)/f_{CPU} + 171.3125	
	Option value: 04H	181 (182)/f_{CPU} + 166.75		139 (140)/f_{CPU} + 166.75	
	Option value: 05H	404 (411)/f_{CPU} + 231.875		362 (369)/f_{CPU} + 231.875	
Set information library		75/f_{CPU} + 78884.5625	75/f_{CPU} + 527566.875	67/f_{CPU} + 78884.5625	67/f_{CPU} + 527566.875
EEPROM write library		318 (321)/f_{CPU} + 538.75	318 (321)/f_{CPU} + 1386.25	262 (265)/f_{CPU} + 538.75	262 (265)/f_{CPU} + 1386.25

Remarks 1. Values in parentheses indicate values when a write start address structure is located other than in the internal high-speed RAM.

2. The above processing times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

3. f_{CPU}: CPU operation clock frequency

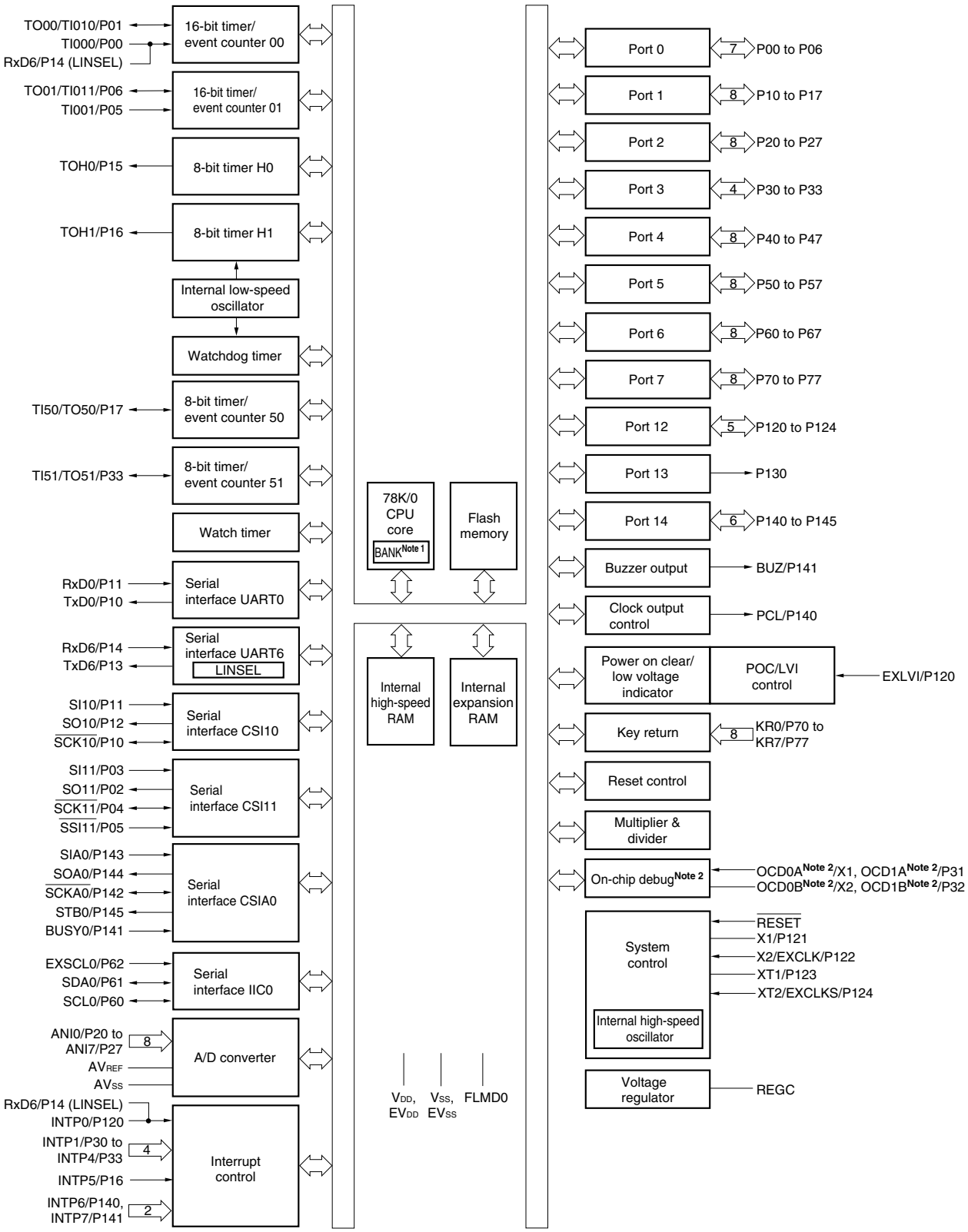
4. RSTS: Bit 7 of the internal oscillation mode register (RCM)

(6/6)

78K0/Kx2 Microcontrollers	Package	Product type	Quality grace	Part Number
78K0/KE2	64-pin plastic FLGA (5x5)	Conventional-specification products	Standard products	μPD78F0531FC-AA1-A, 78F0532FC-AA1-A, 78F0533FC-AA1-A, 78F0534FC-AA1-A, 78F0535FC-AA1-A, 78F0536FC-AA1-A, 78F0537FC-AA1-A, 78F0537DFC-AA1-A[Note]
		Expanded-specification products	Standard products	μPD78F0531AFC-AA1-A, 78F0532AFC-AA1-A, 78F0533AFC-AA1-A, 78F0534AFC-AA1-A, 78F0535AFC-AA1-A, 78F0536AFC-AA1-A, 78F0537AFC-AA1-A, 78F0537DAFC-AA1-A[Note]
<R>	64-pin plastic FBGA (4x4)	Expanded-specification products	Standard products	μPD78F0531AF1-AA2-A, 78F0532AF1-AA2-A, 78F0533AF1-AA2-A, 78F0534AF1-AA2-A, 78F0535AF1-AA2-A, 78F0536AF1-AA2-A, 78F0537AF1-AA2-A, 78F0537DAF1-AA2-A[Note]
78K0/KF2	80-pin plastic LQFP (14x14)	Conventional-specification products	Standard products	μPD78F0544GC-UBT-A, 78F0545GC-UBT-A, 78F0546GC-UBT-A, 78F0547GC-UBT-A, 78F0547DGC-UBT-A[Note]
			(A) grade products	μPD78F0544GC(A)-GAD-AX, 78F0545GC(A)-GAD-AX, 78F0546GC(A)-GAD-AX, 78F0547GC(A)-GAD-AX
			(A2) grade products	μPD78F0544GC(A2)-GAD-AX, 78F0545GC(A2)-GAD-AX, 78F0546GC(A2)-GAD-AX, 78F0547GC(A2)-GAD-AX
		Expanded-specification products	Standard products	μPD78F0544AGC-GAD-AX, 78F0545AGC-GAD-AX, 78F0546AGC-GAD-AX, 78F0547AGC-GAD-AX, 78F0547DAGC-GAD-AX[Note]
			(A) grade products	μPD78F0544AGCA-GAD-G, 78F0545AGCA-GAD-G, 78F0546AGCA-GAD-G, 78F0547AGCA-GAD-G
			(A2) grade products	μPD78F0544AGCA2-GAD-G, 78F0545AGCA2-GAD-G, 78F0546AGCA2-GAD-G, 78F0547AGCA2-GAD-G
	80-pin plastic LQFP (fine pitch) (12x12)	Conventional-specification products	Standard products	μPD78F0544GK-8EU-A, 78F0545GK-8EU-A, 78F0546GK-8EU-A, 78F0547GK-8EU-A, 78F0547DGK-8EU-A[Note]
			(A) grade products	μPD78F0544GK(A)-GAK-AX, 78F0545GK(A)-GAK-AX, 78F0546GK(A)-GAK-AX, 78F0547GK(A)-GAK-AX
			(A2) grade products	μPD78F0544GK(A2)-GAK-AX, 78F0545GK(A2)-GAK-AX, 78F0546GK(A2)-GAK-AX, 78F0547GK(A2)-GAK-AX
		Expanded-specification products	Standard products	μPD78F0544AGK-GAK-AX, 78F0545AGK-GAK-AX, 78F0546AGK-GAK-AX, 78F0547AGK-GAK-AX, 78F0547DAGK-GAK-AX[Note]
			(A) grade products	μPD78F0544AGKA-GAK-G, 78F0545AGKA-GAK-G, 78F0546AGKA-GAK-G, 78F0547AGKA-GAK-G
			(A2) grade products	μPD78F0544AGKA2-GAK-G, 78F0545AGKA2-GAK-G, 78F0546AGKA2-GAK-G, 78F0547AGKA2-GAK-G

Note The μPD78F0537D, 78F0537DA, 78F0547D, and 78F0547DA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

1.7.5 78K0/KF2



Notes 1. Available only in the products whose flash memory is at least 96 KB.

2. Available only in the products with on-chip debug function.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

(e) XT1, XT2

These are the pins for connecting a resonator for subsystem clock.

(f) EXCLKS

This is an external clock input pin for subsystem clock.

Caution Process the P121/X1/OCD0A pin of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P121/X1/OCD0A
Flash memory programmer connection		Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset	
	During reset released	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

Remark X1 and X2 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A and OCD0B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD and 78F05xxDA ONLY).**

2.2.10 P130 (port 13)

P130 functions as an output-only port.

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P130	–	√Note	√			

Note This is not mounted onto 38-pin and 44-pin products of the 78K0/KC2.

Remarks 1. When the device is reset, P130 outputs a low level. Therefore, to output a high level from P130 before the device is reset, the output signal of P130 can be used as a pseudo reset signal of the CPU (see the figure for **Remark** in **5.2.10 Port 13**).

2. √: Mounted, –: Not mounted

5.2.2 Port 1

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P10/$\overline{\text{SCK10}}$/TxD0	√					
P11/SI10/RxD0	√					
P12/SO10	√					
P13/TxD6	√					
P14/RxD6	√					
P15/TOH0	√					
P16/TOH1/INTP5	√					
P17/TI50/TO50	√					

Remark √: Mounted

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

This port can also be used for external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

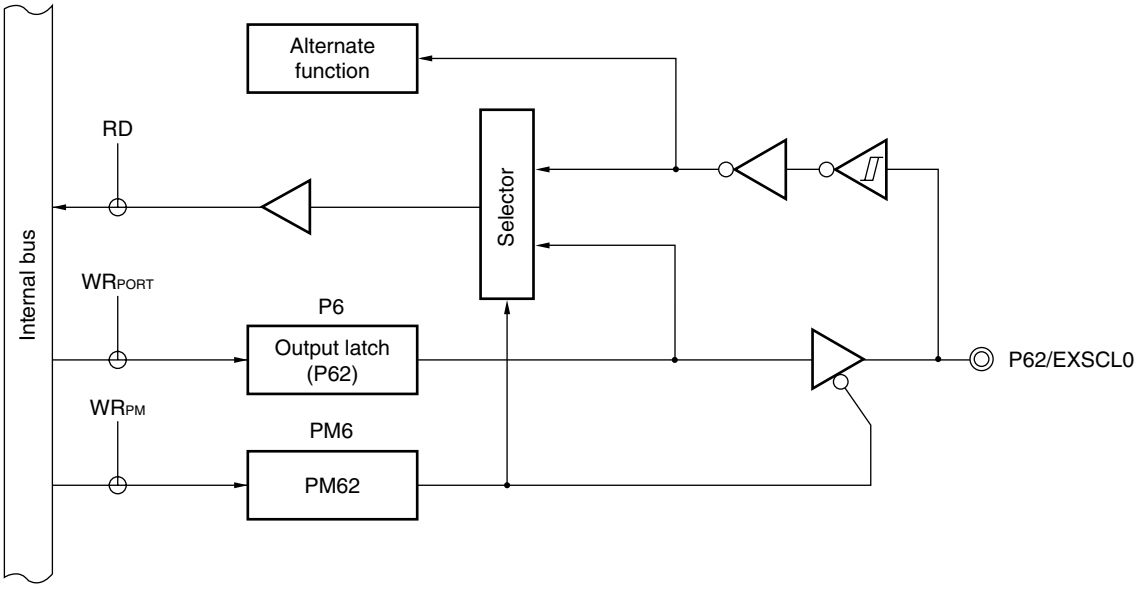
Reset signal generation sets port 1 to input mode.

Figures 5-7 to 5-11 show block diagrams of port 1.

Cautions 1. To use P10/$\overline{\text{SCK10}}$/TxD0 and P12/SO10 as general-purpose ports, set serial operation mode register 10 (CSIM10) and serial clock selection register 10 (CSIC10) to the default status (00H).

2. To use P13/TxD6 as general-purpose port, clear bit 0 (TXDLV6) of asynchronous serial interface control register 6 (ASICL6) to 0 (normal output of TxD6).

Figure 5-18. Block Diagram of P62



P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

Caution A through current flows through P62 if an intermediate potential is input to this pin, because the input buffer is also turned on when P62 is in output mode. Consequently, do not input an intermediate potential when P62 is in output mode.

Figure 6-4. Format of Clock Operation Mode Select Register (OSCCTL)
(78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)

Address: FF9FH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	<0>
OSCCTL	EXCLK	OSCSEL	EXCLKS[Note]	OSCSELS[Note]	0	0	0	AMPH

EXCLK	OSCSEL	High-speed system clock pin operation mode	P121/X1 pin	P122/X2/EXCLK pin
0	0	I/O port mode	I/O port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	I/O port mode	I/O port	
1	1	External clock input mode	I/O port	External clock input

AMPH	Operating frequency control
0	1 MHz ≤ f_{XH} ≤ 10 MHz
1	10 MHz < f_{XH} ≤ 20 MHz

Note EXCLKS and OSCSELS are used in combination with XTSTART (bit 6 of the processor clock control register (PCC)). See **(3) Setting of operation mode for subsystem clock pin**.

Cautions 1. Be sure to set AMPH to 1 if the high-speed system clock oscillation frequency exceeds 10 MHz.

<R> **2. Set AMPH before setting the main clock mode register (MCM).**

3. Set AMPH before setting the peripheral functions after a reset release. The value of AMPH can be changed only once after a reset release. When the high-speed system clock (X1 oscillation) is selected as the CPU clock, supply of the CPU clock is stopped for 4.06 to 16.12 μs after AMPH is set to 1. When the high-speed system clock (external clock input) is selected as the CPU clock, supply of the CPU clock is stopped for the duration of 160 external clocks after AMPH is set to 1.

4. If the STOP instruction is executed when AMPH = 1, supply of the CPU clock is stopped for 4.06 to 16.12 μs after the STOP mode is released when the internal high-speed oscillation clock is selected as the CPU clock, or for the duration of 160 external clocks when the high-speed system clock (external clock input) is selected as the CPU clock. When the high-speed system clock (X1 oscillation) is selected as the CPU clock, the oscillation stabilization time is counted after the STOP mode is released.

5. To change the value of EXCLK and OSCSEL, be sure to confirm that bit 7 (MSTOP) of the main OSC control register (MOC) is 1 (the X1 oscillator stops or the external clock from the EXCLK pin is disabled).

6. Be sure to clear bits 1 to 3 to 0.

Remark f_{XH}: High-speed system clock oscillation frequency

Table 6-6. CPU Clock Transition and SFR Register Setting Examples (2/5)

(4) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	AMPH[Note]	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0
(B) → (C) (X1 clock: 1 MHz ≤ f_{XH} ≤ 10 MHz)	0	0	1	0	Must be checked	1	1
(B) → (C) (external main clock: 1 MHz ≤ f_{XH} ≤ 10 MHz)	0	1	1	0	Must not be checked	1	1
(B) → (C) (X1 clock: 10 MHz < f_{XH} ≤ 20 MHz)	1	0	1	0	Must be checked	1	1
(B) → (C) (external main clock: 10 MHz < f_{XH} ≤ 20 MHz)	1	1	1	0	Must not be checked	1	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: T_A = –40 to +125°C)).

(5) CPU clock changing from internal high-speed oscillation clock (B) to subsystem clock (D)[Note]

Note The 78K0/KB2 is not provided with a subsystem clock.

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	XTSTART	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(B) → (D) (XT1 clock)	0	0	1	Necessary	1
	1	×	×		
(B) → (D) (external subsystem clock)	0	1	1	Unnecessary	1

Unnecessary if the CPU is operating with the subsystem clock

Remarks 1. (A) to (I) in Table 6-6 correspond to (A) to (I) in Figure 6-17 and 6-18.

2. EXCLK, OSCSEL, EXCLKS, OSCSELS, AMPH: Bits 7 to 4 and 0 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)
XTSTART, CSS: Bits 6 and 4 of the processor clock control register (PCC)
×: Don't care

<5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.

<6> To stop the count operation, set TMHEn = 0.

If the setting value of the CMP0n register is N, the setting value of the CMP1n register is M, and the count clock frequency is f_{CNT}, the PWM pulse output cycle and duty are as follows.

- PWM pulse output cycle = (N + 1)/f_{CNT}
- Duty = (M + 1)/(N + 1)

Cautions 1. The set value of the CMP1n register can be changed while the timer counter is operating. However, this takes a duration of three operating clocks (signal selected by the CKSn2 to CKSn0 bits of the TMHMDn register) from when the value of the CMP1n register is changed until the value is transferred to the register.

2. Be sure to set the CMP1n register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMP1n register).

3. Make sure that the CMP1n register setting value (M) and CMP0n register setting value (N) are within the following range.

00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

Remarks 1. For the setting of the output pin, see **9.3 (3) Port mode register 1 (PM1)**.

2. For details on how to enable the INTTMHn signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

3. n = 0, 1

<10> By performing the procedures above, an arbitrary carrier clock is obtained. To stop the count operation, clear TMHE1 to 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the carrier clock output cycle and duty are as follows.

- Carrier clock output cycle = (N + M + 2)/f_{CNT}
- Duty = High-level width/carrier clock output width = (M + 1)/(N + M + 2)

Cautions 1. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

2. Set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

3. Set the values of the CMP01 and CMP11 registers in a range of 01H to FFH.

4. The set value of the CMP11 register can be changed while the timer counter is operating. However, it takes the duration of three operating clocks (signal selected by the CKS12 to CKS10 bits of the TMHMD1 register) since the value of the CMP11 register has been changed until the value is transferred to the register.

5. Be sure to set the RMC1 bit before the count operation is started.

Remarks 1. For the setting of the output pin, see **9.3 (3) Port mode register 1 (PM1)**.

2. For how to enable the INTTMH1 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

10.2 Configuration of Watch Timer

The watch timer includes the following hardware.

Table 10-3. Watch Timer Configuration

Item	Configuration
Counter	5 bits × 1
Prescaler	11 bits × 1
Control register	Watch timer operation mode register (WTM)

10.3 Register Controlling Watch Timer

The watch timer is controlled by the watch timer operation mode register (WTM).

- **Watch timer operation mode register (WTM)**
  This register sets the watch timer count clock, enables/disables operation, prescaler interval time, and 5-bit counter operation control.
  WTM is set by a 1-bit or 8-bit memory manipulation instruction.
  Reset signal generation clears WTM to 00H.

10.4 Watch Timer Operations

10.4.1 Watch timer operation

The watch timer generates an interrupt request signal (INTWT) at a specific time interval by using the peripheral hardware clock or subsystem clock.

When bit 0 (WTM0) and bit 1 (WTM1) of the watch timer operation mode register (WTM) are set to 1, the count operation starts. When these bits are cleared to 0, the 5-bit counter is cleared and the count operation stops.

When the interval timer is simultaneously operated, zero-second start can be achieved only for the watch timer by clearing WTM1 to 0. In this case, however, the 11-bit prescaler is not cleared. Therefore, an error up to $2^9 \times 1/fw$ seconds occurs in the first overflow (INTWT) after zero-second start.

The interrupt request is generated at the following time intervals.

Table 10-4. Watch Timer Interrupt Time

WTM3	WTM2	Interrupt Time Selection	When Operated at f_{SUB} = 32.768 kHz (WTM7 = 1)	When Operated at f_{PRS} = 2 MHz (WTM7 = 0)	When Operated at f_{PRS} = 5 MHz (WTM7 = 0)	When Operated at f_{PRS} = 10 MHz (WTM7 = 0)	When Operated at f_{PRS} = 20 MHz (WTM7 = 0)
0	0	$2^{14}/fw$	0.5 s	1.05 s	0.419 s	0.210 s	0.105 s
0	1	$2^{13}/fw$	0.25 s	0.52 s	0.210 s	0.105 s	52.5 ms
1	0	$2^5/fw$	977 μs	2.05 ms	819 μs	410 μs	205 μs
1	1	$2^4/fw$	488 μs	1.02 ms	410 μs	205 μs	102 μs

Remarks 1. fw: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

10.4.2 Interval timer operation

The watch timer operates as interval timer which generates interrupt request signals (INTWTI) repeatedly at an interval of the preset count value.

The interval time can be selected with bits 4 to 6 (WTM4 to WTM6) of the watch timer operation mode register (WTM).

When bit 0 (WTM0) of the WTM is set to 1, the count operation starts. When this bit is set to 0, the count operation stops.

Table 10-5. Interval Timer Interval Time

WTM6	WTM5	WTM4	Interval Time	When Operated at f_{SUB} = 32.768 kHz (WTM7 = 1)	When Operated at f_{PRS} = 2 MHz (WTM7 = 0)	When Operated at f_{PRS} = 5 MHz (WTM7 = 0)	When Operated at f_{PRS} = 10 MHz (WTM7 = 0)	When Operated at f_{PRS} = 20 MHz (WTM7 = 0)
0	0	0	$2^4/fw$	488 μs	1.02 ms	410 μs	205 μs	102 μs
0	0	1	$2^5/fw$	977 μs	2.05 ms	820 μs	410 μs	205 μs
0	1	0	$2^6/fw$	1.95 ms	4.10 ms	1.64 ms	820 μs	410 μs
0	1	1	$2^7/fw$	3.91 ms	8.20 ms	3.28 ms	1.64 ms	820 μs
1	0	0	$2^8/fw$	7.81 ms	16.4 ms	6.55 ms	3.28 ms	1.64 ms
1	0	1	$2^9/fw$	15.6 ms	32.8 ms	13.1 ms	6.55 ms	3.28 ms
1	1	0	$2^{10}/fw$	31.3 ms	65.5 ms	26.2 ms	13.1 ms	6.55 ms
1	1	1	$2^{11}/fw$	62.5 ms	131.1 ms	52.4 ms	26.2 ms	13.1 ms

Remarks 1. fw: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

(2) 1-byte transmission/reception communication operation

(a) 1-byte transmission/reception

When bit 7 (CSIAE0) and bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) = 1, 0, respectively, if communication data is written to serial I/O shift register 0 (SIOA0), the data is output via the SOA0 pin in synchronization with the $\overline{\text{SCKA0}}$ falling edge, and stored in the SIOA0 register in synchronization with the rising edge 1 clock later.

Data transmission and data reception can be performed simultaneously.

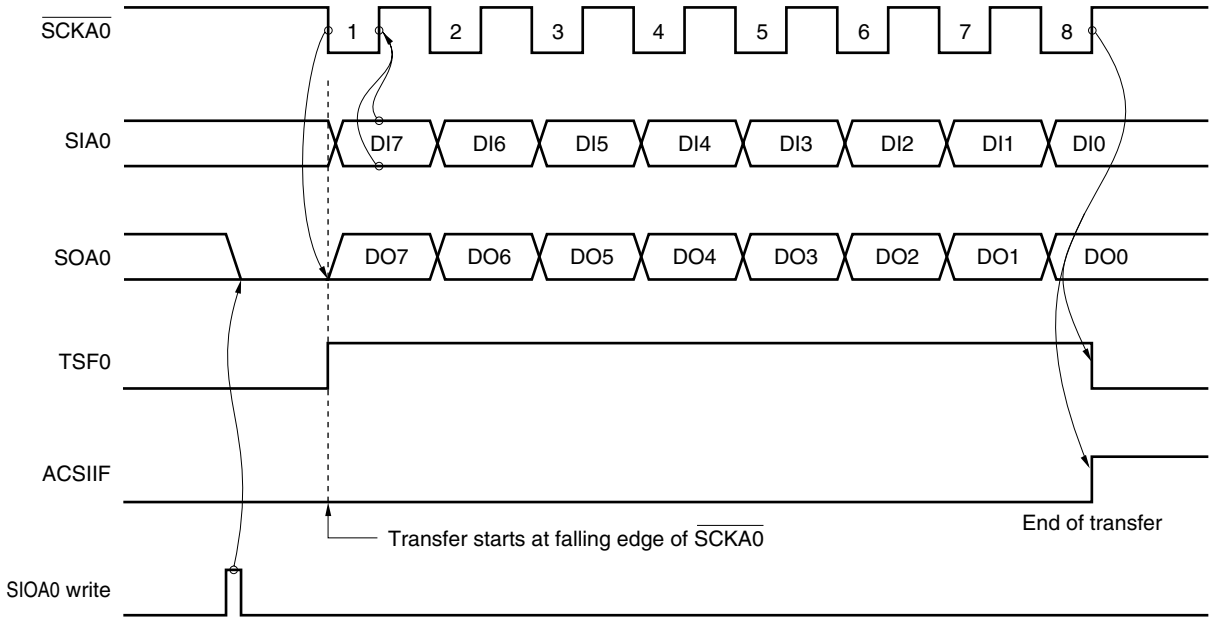
If only reception is to be performed, communication can only be started by writing a dummy value to the SIOA0 register.

When communication of 1 byte is complete, an interrupt request signal (INTACSI) is generated.

In 1-byte transmission/reception, the setting of bit 5 (ATM0) of CSIMA0 is invalid.

Be sure to read data after confirming that bit 0 (TSF0) of serial status register 0 (CSIS0) = 0.

Figure 17-10. 3-Wire Serial I/O Mode Timing



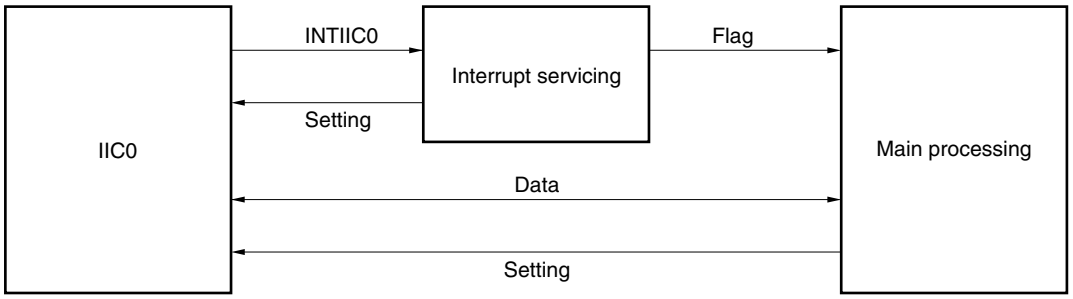
Caution The SOA0 pin becomes low level by an SIOA0 write.

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIIC0 interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIIC0 interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIIC0.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIIC0 interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as TRC0.

CHAPTER 22 STANDBY FUNCTION

22.1 Standby Function and Configuration

22.1.1 Standby function

The standby function is mounted onto all 78K0/Kx2 microcontroller products.

The standby function is designed to reduce the operating current of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, internal low-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

Note The 78K0/KB2 is not provided with a subsystem clock oscillator.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The subsystem clock oscillation cannot be stopped. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

23.1 Register for Confirming Reset Source

Many internal reset generation sources exist in the 78K0/Kx2 microcontrollers. The reset control flag register (RESF) is used to store which source has generated the reset request.

RESF can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset by power-on-clear (POC) circuit, and reading RESF set RESF to 00H.

Figure 23-5. Format of Reset Control Flag Register (RESF)

Address: FFACH After reset: 00H[Note] R

Symbol	7	6	5	4	3	2	1	0
RESF	0	0	0	WDTRF	0	0	0	LVIRF

WDTRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by low-voltage detector (LVI)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

Note The value after reset varies depending on the reset source.

Caution Do not read data by a 1-bit memory manipulation instruction.

The status of RESF when a reset request is generated is shown in Table 23-3.

Table 23-3. RESF Status When Reset Request Is Generated

Reset Source / Flag	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
WDTRF	Cleared (0)	Cleared (0)	Set (1)	Held
LVIRF			Held	Set (1)

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

DC Characteristics (4/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		3.2	5.5	mA
				Resonator connection		4.5	6.9	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		1.6	2.8	mA
				Resonator connection		2.3	3.9	mA
			f_{XH} = 10 MHz V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		1.5	2.7	mA
				Resonator connection		2.2	3.2	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.9	1.6	mA
				Resonator connection		1.3	2.0	mA
			f_{XH} = 5 MHz, V_{DD} = 2.0 V [Notes 2, 3]	Square wave input		0.7	1.4	mA
				Resonator connection		1.0	1.6	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			1.4	2.5	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		6	30	μA
				Resonator connection		15	35	μA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		0.8	2.6	mA
				Resonator connection		2.0	4.4	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		0.4	1.3	mA
				Resonator connection		1.0	2.4	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.2	0.65	mA
				Resonator connection		0.5	1.1	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			0.4	1.2	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		3.0	27	μA
				Resonator connection		12	32	μA
	I_{DD3}[Note 6]	STOP mode				1	20	μA
			T_A = −40 to +70 °C			1	10	μA
A/D converter operating current	I_{ADC}[Note 7]	2.3 V ≤ AV_{REF} ≤ V_{DD}, ADCS = 1				0.86	1.9	mA
Watchdog timer operating current	I_{WDT}[Note 8]	During 240 kHz internal low-speed oscillation clock operation				5	10	μA
LVI operating current	I_{LVI}[Note 9]					9	18	μA

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or external subsystem clock frequency)

(Notes on next page)

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

(2) Serial interface

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

(a) UART6 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(c) IIC0

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{SCL}		0	100	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7	–	0.6	–	μs
Hold time[Note 1]	$t_{HD:STA}$		4.0	–	0.6	–	μs
Hold time when SCL0 = "L"	t_{LOW}	Internal clock operation	4.7	–	1.3	–	μs
		EXSCL0 clock (6.4 MHz) operation	4.7	–	1.25	–	μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0	–	0.6	–	μs
Data setup time (reception)	$t_{SU:DAT}$		250	–	100	–	ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	$f_W = f_{XH}/2^N$ or $f_W = f_{EXSCL0}$ selected[Note 3]	0	3.45	0	0.9[Note 4]	μs
						1.00[Note 5]	
		$f_W = f_{RH}/2^N$ selected[Note 3]	0	3.45	0	1.05	μs
Setup time of stop condition	$t_{SU:STO}$		4.0	–	0.6	–	μs
Bus free time	t_{BUF}		4.7	–	1.3	–	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

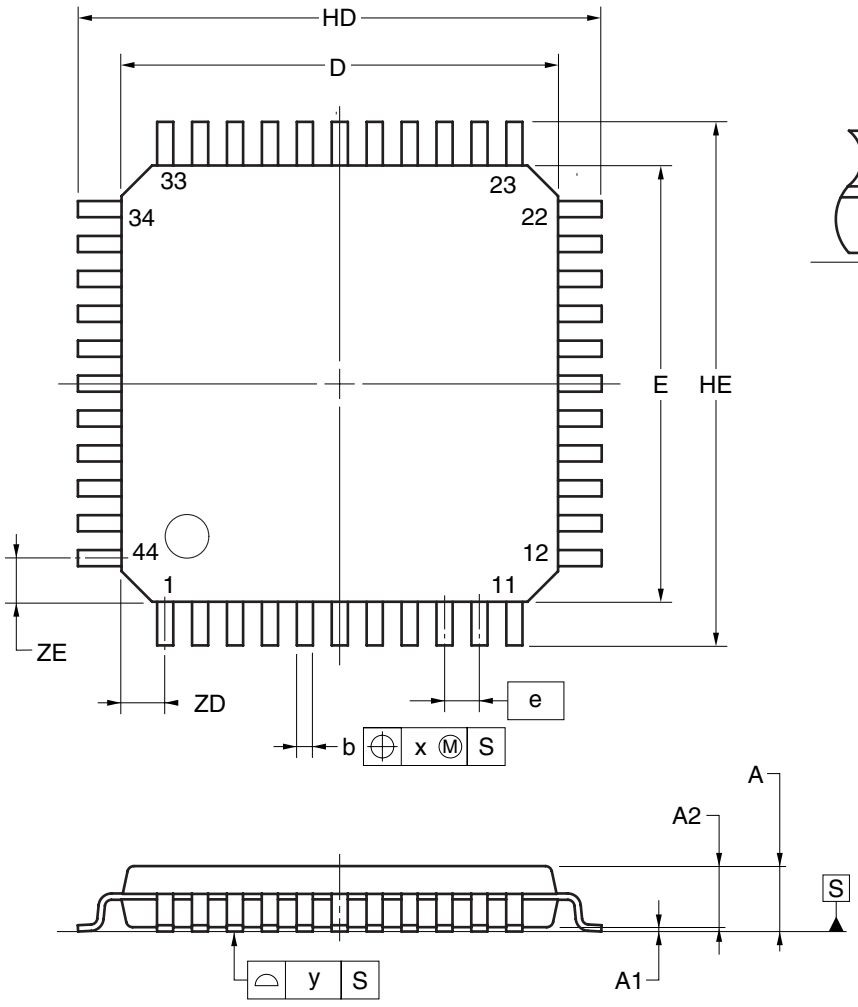
3. f_W indicates the IIC0 transfer clock selected by the IICCL and IICX0 registers.

4. When $f_W \geq 4.4$ MHz is selected

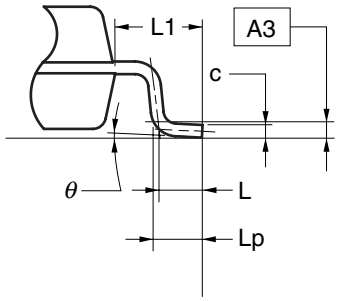
5. When $f_W < 4.4$ MHz is selected

- μPD78F0511GB(A)-GAF-AX, 78F0512GB(A)-GAF-AX, 78F0513GB(A)-GAF-AX
- μPD78F0511GB(A2)-GAF-AX, 78F0512GB(A2)-GAF-AX, 78F0513GB(A2)-GAF-AX
- μPD78F0511AGB-GAF-AX, 78F0512AGB-GAF-AX, 78F0513AGB-GAF-AX, 78F0513DAGB-GAF-AX
- μPD78F0511AGBA-GAF-G, 78F0512AGBA-GAF-G, 78F0513AGBA-GAF-G
- μPD78F0511AGBA2-GAF-G, 78F0512AGBA2-GAF-G, 78F0513AGBA2-GAF-G

44-PIN PLASTIC LQFP (10x10)



detail of lead end



(UNIT:mm)

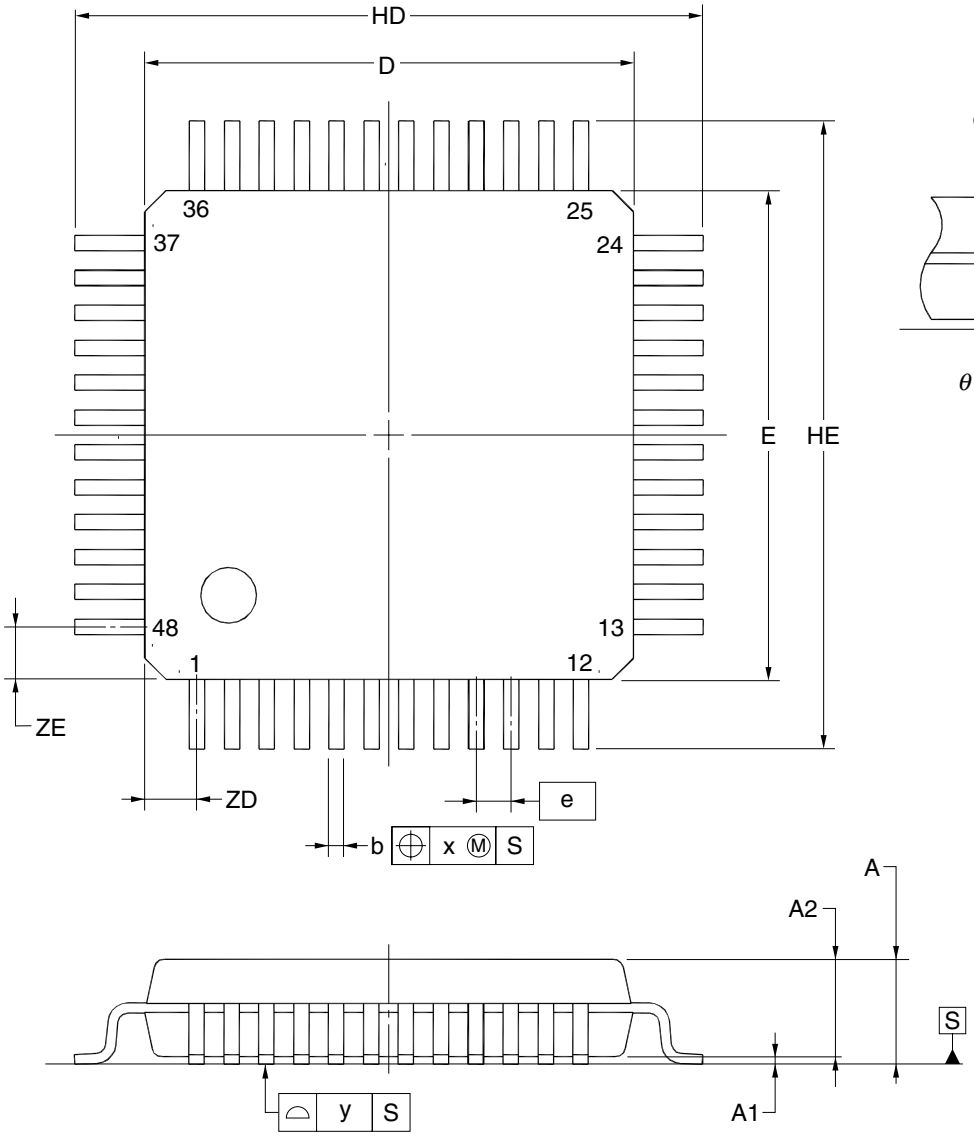
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.35^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

P44GB-80-GAF

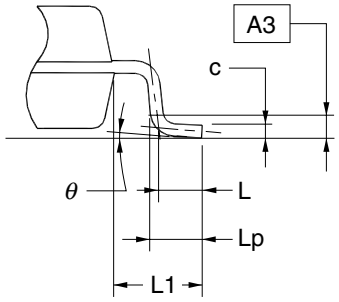
NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

- μPD78F0511GA-8EU-A, 78F0512GA-8EU-A, 78F0513GA-8EU-A, 78F0514GA-8EU-A, 78F0515GA-8EU-A, 78F0515DGA-8EU-A

48-PIN PLASTIC LQFP (FINE PITCH)(7x7)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-8EU

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.