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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFLGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0533afc-aa1-a

(3/6)

78K0/Kx2 Microcontrollers	Package	Product type	Quality grace	Part Number
78K0/KE2	64-pin plastic LQFP (fine pitch) (10x10)	Conventional-specification products	Standard products	μPD78F0531GB-UEU-A, 78F0532GB-UEU-A, 78F0533GB-UEU-A, 78F0534GB-UEU-A, 78F0535GB-UEU-A, 78F0536GB-UEU-A, 78F0537GB-UEU-A, 78F0537DGB-UEU-A[Note]
			(A) grade products	μPD78F0531GB(A)-GAH-AX, 78F0532GB(A)-GAH-AX, 78F0533GB(A)-GAH-AX, 78F0534GB(A)-GAH-AX, 78F0535GB(A)-GAH-AX, 78F0536GB(A)-GAH-AX, 78F0537GB(A)-GAH-AX
			(A2) grade products	μPD78F0531GB(A2)-GAH-AX, 78F0532GB(A2)-GAH-AX, 78F0533GB(A2)-GAH-AX, 78F0534GB(A2)-GAH-AX, 78F0535GB(A2)-GAH-AX, 78F0536GB(A2)-GAH-AX, 78F0537GB(A2)-GAH-AX
		Expanded-specification products	Standard products	μPD78F0531AGB-GAH-AX, 78F0532AGB-GAH-AX, 78F0533AGB-GAH-AX, 78F0534AGB-GAH-AX, 78F0535AGB-GAH-AX, 78F0536AGB-GAH-AX, 78F0537AGB-GAH-AX, 78F0537DAGB-GAH-AX[Note]
			(A) grade products	μPD78F0531AGBA-GAH-G, 78F0532AGBA-GAH-G, 78F0533AGBA-GAH-G, 78F0534AGBA-GAH-G, 78F0535AGBA-GAH-G, 78F0536AGBA-GAH-G, 78F0537AGBA-GAH-G
			(A2) grade products	μPD78F0531AGBA2-GAH-G, 78F0532AGBA2-GAH-G, 78F0533AGBA2-GAH-G, 78F0534AGBA2-GAH-G, 78F0535AGBA2-GAH-G, 78F0536AGBA2-GAH-G, 78F0537AGBA2-GAH-G

Note The μPD78F0537D and 78F0537DA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2.2.6 P50 to P57 (port 5)

P50 to P57 function as an I/O port. P50 to P57 can be set to input or output port in 1-bit units using port mode register 5 (PM5). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 5 (PU5).

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P50	–			√		√
P51	–			√		√
P52	–			√		√
P53	–			√		√
P54	–			–		√
P55	–			–		√
P56	–			–		√
P57	–			–		√

Remark √: Mounted, –: Not mounted

2.2.7 P60 to P67 (port 6)

P60 to P67 function as an I/O port. These pins also function as pins for serial interface data I/O, clock I/O, and external clock input.

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P60/SCL0	√	√				√
P61/SDA0	√	√				√
P62/EXSCL0	–	√				√
P63	–	√				√
P64	–	–				√
P65	–	–				√
P66	–	–				√
P67	–	–				√

Remark √: Mounted, –: Not mounted

The following operation modes can be specified in 1-bit units.

3.2.3 Special function registers (SFRs)

Unlike a general-purpose register, each special function register has a special function.

SFRs are allocated to the FF00H to FFFFH area.

Special function registers can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulatable bit units, 1, 8, and 16, depend on the special function register type.

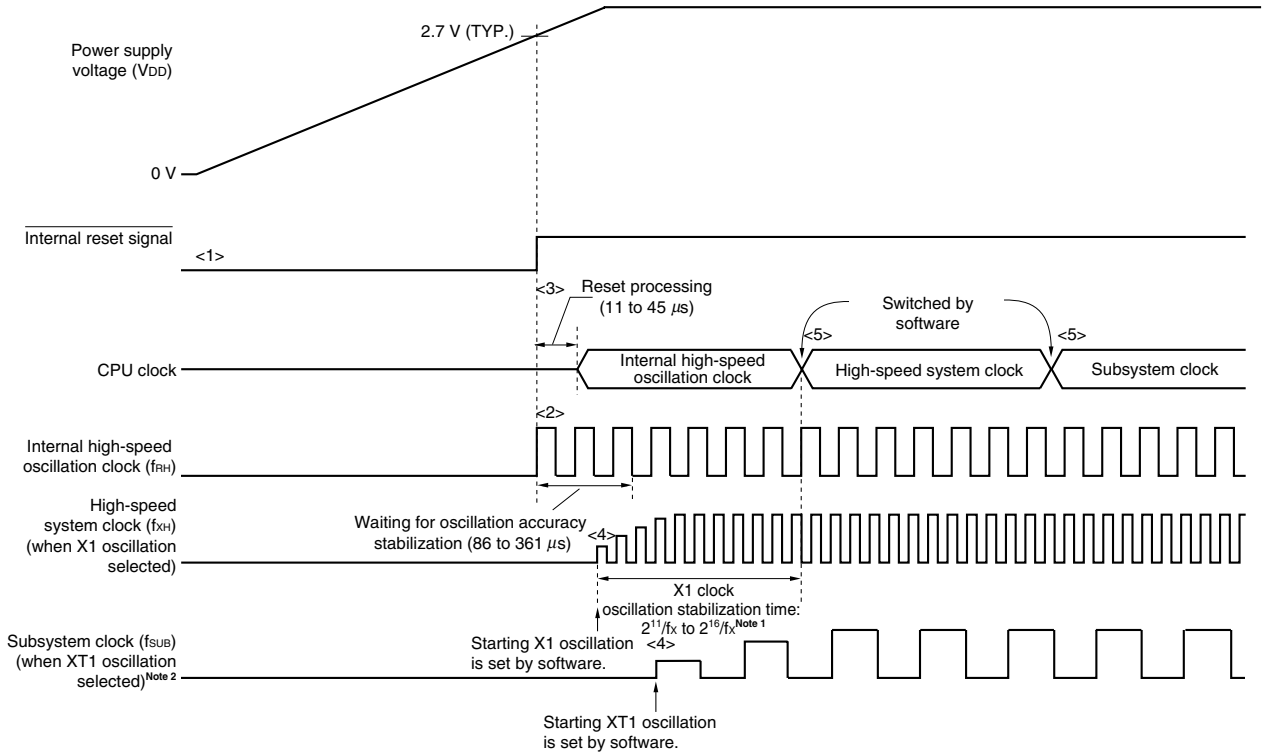
Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit).
  This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr).
  This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp).
  When specifying an address, describe an even address.

Table 3-8 gives a list of the special function registers. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of a special function register. It is a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0. When using the RA78K0, ID78K0-QB, SM+ for 78K0, and SM+ for 78K0/KX2, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding special function register can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulatable bit units
  Indicates the manipulatable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Figure 6-16. Clock Generator Operation When Power Supply Voltage Is Turned On (When 2.7 V/1.59 V POC Mode Is Set (Option Byte: POCMODE = 1))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 2.7 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> After the reset is released and reset processing is performed, the CPU starts operation on the internal high-speed oscillation clock.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **(1)** in **6.6.1 Example of controlling high-speed system clock** and **(1)** in **6.6.3 Example of controlling subsystem clock**).

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **(3)** in **6.6.1 Example of controlling high-speed system clock** and **(3)** in **6.6.3 Example of controlling subsystem clock**).

Notes 1. When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

2. The 78K0/KB2 is not provided with a subsystem clock.

Cautions 1. A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the supply voltage reaches 1.59 V (TYP.). If the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) within 1.93 ms, the power supply oscillation stabilization time of 0 to 5.39 ms is automatically generated before reset processing.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK and EXCLKS pins is used.

CHAPTER 12 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2
Clock output	–	38/44 pins: – 48 pins: √	√		
Buzzer output	–			√	

Remark √: Mounted, –: Not mounted

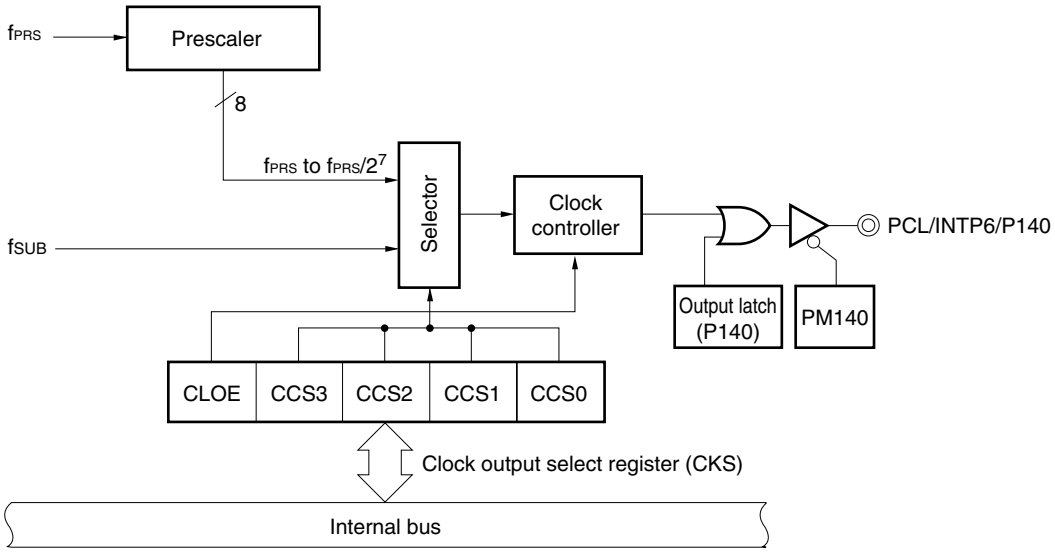
12.1 Functions of Clock Output/Buzzer Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs. The clock selected with the clock output selection register (CKS) is output.

In addition, the buzzer output is intended for square-wave output of buzzer frequency selected with CKS.

Figure 12-1 and 12-2 show the block diagram of clock output/buzzer output controller.

Figure 12-1. Block Diagram of Clock Output/Buzzer Output Controller (78K0/KD2, 48-pin Products of 78K0/KC2)



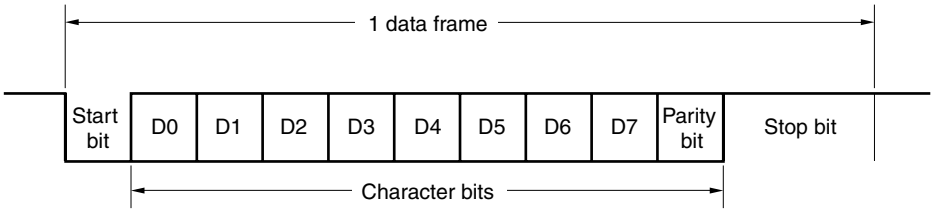
(2) Communication operation

(a) Format and waveform example of normal transmit/receive data

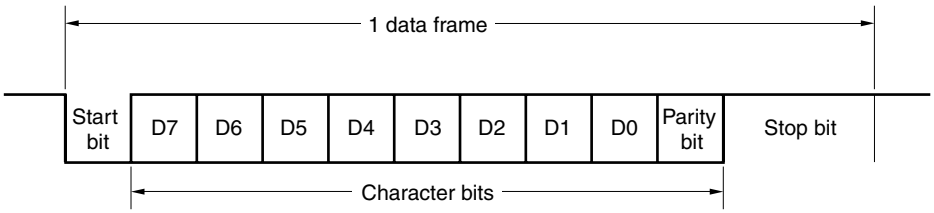
Figures 15-13 and 15-14 show the format and waveform example of the normal transmit/receive data.

Figure 15-13. Format of Normal UART Transmit/Receive Data

1. LSB-first transmission/reception



2. MSB-first transmission/reception



One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

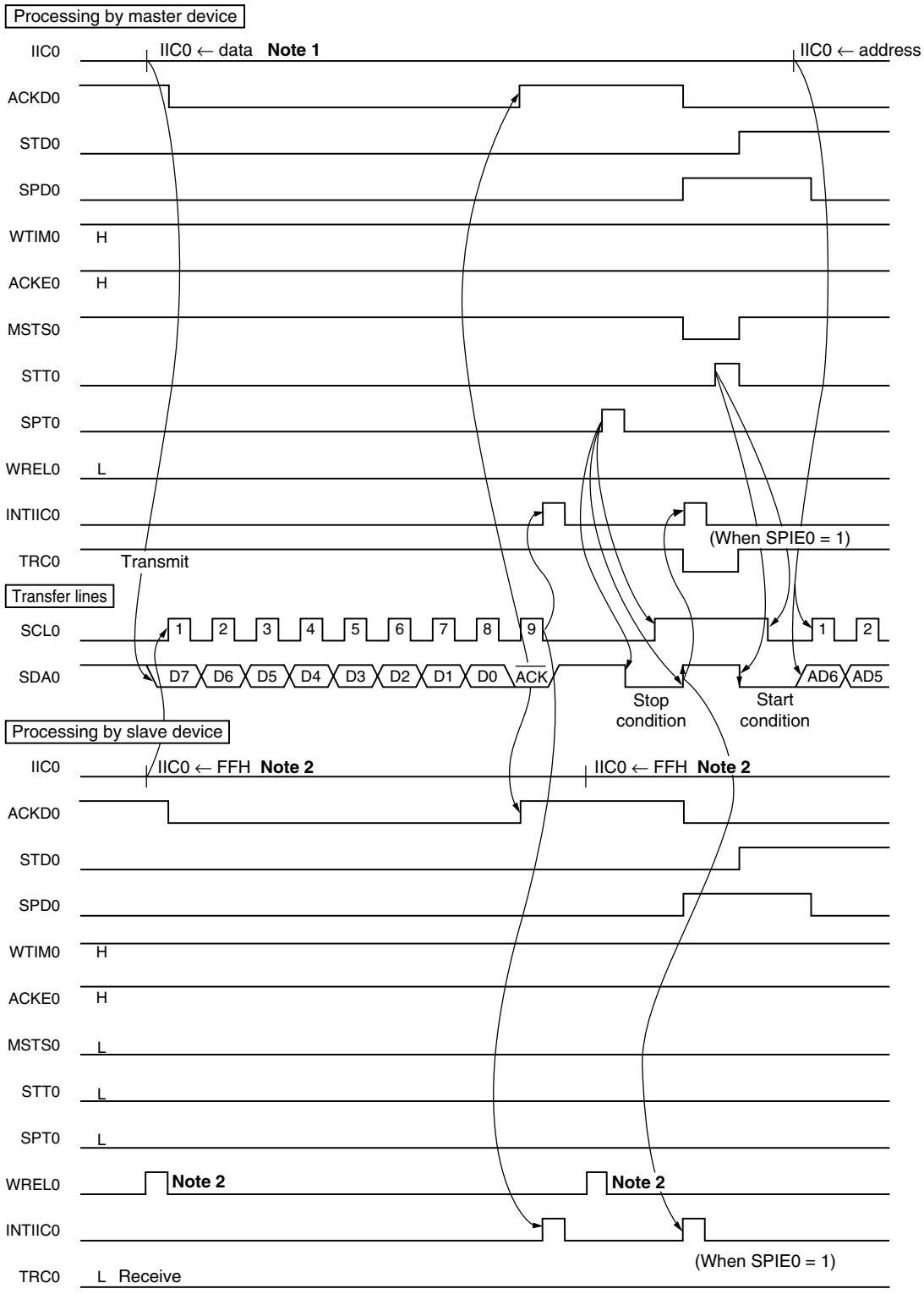
The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 6 (ASIM6).

Whether data is communicated with the LSB or MSB first is specified by bit 1 (DIR6) of asynchronous serial interface control register 6 (ASICL6).

Whether the TxD6 pin outputs normal or inverted data is specified by bit 0 (TXDLV6) of ASICL6.

Figure 18-27. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)

(3) Stop condition



Notes 1. Write data to IIC0, not setting WREL0, in order to cancel a wait state during master transmission.

2. To cancel slave wait, write “FFH” to IIC0 or set WREL0.

Figure 20-17. Format of External Interrupt Rising Edge Enable Register (EGP) and External Interrupt Falling Edge Enable Register (EGN) (1/2)

(1) 78K0/KB2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

(2) 38-pin and 44-pin products of 78K0/KC2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

(3) 48-pin products of 78K0/KC2, 78K0/KD2

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Caution Be sure to clear bits 6 and 7 of EGP and EGN to 0 in 78K0/KB2, and 38-pin and 44-pin products of 78K0/KC2.
Be sure to clear bit 7 of EGP and EGN to 0 in 78K0/KD2, and 48-pin products of 78K0/KC2.

Remark n = 0 to 5: 78K0/KB2, 38-pin and 44-pin products of 78K0/KC2
n = 0 to 6: 78K0/KD2, 48-pin products of 78K0/KC2

Figure 24-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source

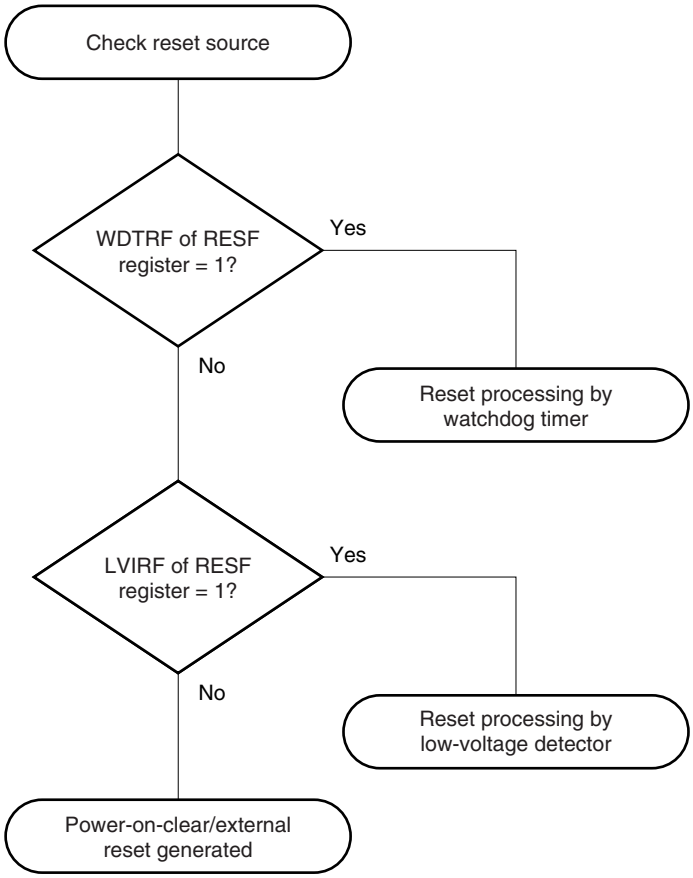


Table 27-15. Interrupt Response Time for Self Programming Library (Conventional-specification Products (μPD78F05xx and 78F05xxD)) (2/2)

(3) When high-speed system clock is used (static model of C compiler/assembler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	136/f_{CPU} + 507	136/f_{CPU} + 407	136/f_{CPU} + 1650	136/f_{CPU} + 714
Block erase library	136/f_{CPU} + 559	136/f_{CPU} + 460	136/f_{CPU} + 1702	136/f_{CPU} + 767
Word write library	272/f_{CPU} + 1589	272/f_{CPU} + 1298	272/f_{CPU} + 2732	272/f_{CPU} + 1605
Block verify library	136/f_{CPU} + 518	136/f_{CPU} + 418	136/f_{CPU} + 1661	136/f_{CPU} + 725
Set information library	72/f_{CPU} + 370	72/f_{CPU} + 165	72/f_{CPU} + 1513	72/f_{CPU} + 472
EEPROM write library[Note]	19/f_{CPU} + 1759	19/f_{CPU} + 1468	19/f_{CPU} + 1759	19/f_{CPU} + 1468
	268/f_{CPU} + 834	268/f_{CPU} + 512	268/f_{CPU} + 2061	268/f_{CPU} + 873

Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	−10	mA
		Total of all pins −80 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	−25	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P64 to P67, P70 to P77	−55	mA
		Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
		Per pin	P121 to P124	−1	mA
		Total of all pins		−4	mA
Output current, low	I_{OL}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P130, P140 to P145	30	mA
		Total of all pins 200 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	60	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P60 to P67, P70 to P77	140	mA
		Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
		Per pin	P121 to P124	4	mA
		Total of all pins		10	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Cautions 1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

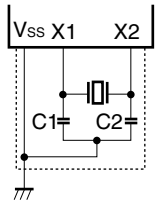
2. The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

X1 Oscillator Characteristics

(T_A = –40 to +110°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
Ceramic resonator, Crystal resonator		X1 clock oscillation frequency (f_X)Note 1	Conventional-specification Products (μPD78F05xx (A2))	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0Note 2		20.0	MHz
				2.7 V ≤ V_{DD} < 4.0 V	1.0Note 2		10.0	
			Expanded-specification Products (μPD78F05xxA(A2))		1.0Note 2		20.0	MHz

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

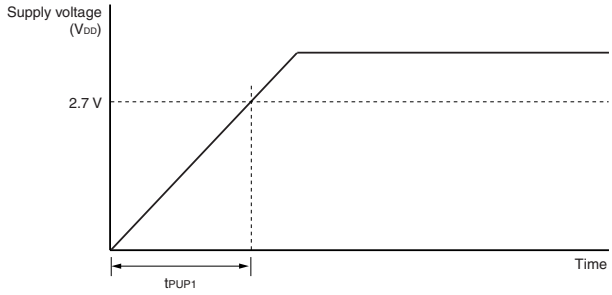
Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Supply Voltage Rise Time (T_A = –40 to +110°C, V_{SS} = EV_{SS} = 0 V)

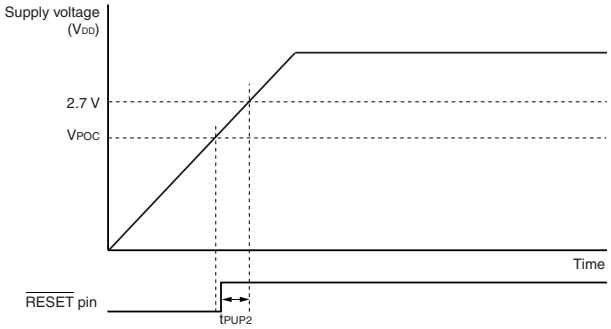
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 2.7 V (V_{DD} (MIN.)) (V_{DD}: 0 V → 2.7 V)	t_{PUP1}	POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 2.7 V (V_{DD} (MIN.)) (releasing $\overline{\text{RESET}}$ input → V_{DD}: 2.7 V)	t_{PUP2}	POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is used			1.9	ms

Supply Voltage Rise Time Timing

• When $\overline{\text{RESET}}$ pin input is not used



• When $\overline{\text{RESET}}$ pin input is used



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

A/D Converter Characteristics

(T_A = –40 to +125°C, 2.7 V ≤ AV_{REF} ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}					10	bit
Overall error[Notes 1, 2]	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V				±0.6	%FSR
Conversion time	t_{CONV}	Conventional-specification Products (μPD78F05xx(A2))	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		36.7	μs
			2.7 V ≤ AV_{REF} < 4.0 V	12.2		36.7	μs
		Expanded-specification Products (μPD78F05xxA (A2))	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		66.6	μs
			2.7 V ≤ AV_{REF} < 4.0 V	12.2		66.6	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V				±0.6	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V				±0.6	%FSR
Integral non-linearity error[Note 1]	I_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V				±4.5	LSB
Differential non-linearity error[Note 1]	D_{LE}	4.0 V ≤ AV_{REF} ≤ 5.5 V				±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V				±2.0	LSB
Analog input voltage	V_{AIN}			AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Table 35-1. Soldering Conditions of Conventional-specification Products (μPD78F05xx and 78F05xxD) (2/3)

(2) 30-pin plastic SSOP (7.62 mm (300))
μPD78F050xMC-5A4-A (x = 0 to 3), 78F0503DMC-5A4-A
44-pin plastic LQFP (10x10)
μPD78F051xGB-UES-A (x = 1 to 3), 78F0513DGB-UES-A
48-pin plastic LQFP (fine pitch) (7x7)
μPD78F051xGA-8EU-A (x = 1 to 5), 78F0515DGA-8EU-A
μPD78F051xGA(A)-GAM-AX (x = 1 to 5), 78F051xGA(A2)-GAM-AX (x = 1 to 5)
52-pin plastic LQFP (10x10)
μPD78F052xGB-UET-A (x = 1 to 7), 78F0527DGB-UET-A
64-pin plastic LQFP (fine pitch) (10x10)
μPD78F053xGB-UEU-A (x = 1 to 7), 78F0537DGB-UEU-A
μPD78F053xGB(A)-GAH-AX (x = 1 to 7), 78F053xGB(A2)-GAH-AX (x = 1 to 7)
64-pin plastic LQFP (14x14)
μPD78F053xGC-UBS-A (x = 1 to 7), 78F0537DGC-UBS-A
64-pin plastic LQFP (12x12)
μPD78F053xGK-UET-A (x = 1 to 7), 78F0537DGK-UET-A
64-pin plastic TQFP (fine pitch) (7x7)
μPD78F053xGA-9EV-A (x = 1 to 7), 78F0537DGA-9EV-A
80-pin plastic LQFP (14x14)
μPD78F054xGC-UBT-A (x = 4 to 7), 78F0547DGC-UBT-A
80-pin plastic LQFP (fine pitch) (12x12)
μPD78F054xGK-8EU-A (x = 4 to 7), 78F0547DGK-8EU-A
μPD78F054xGK(A)-GAK-AX (x = 4 to 7), 78F054xGK(A2)-GAK-AX (x = 4 to 7)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution The μPD78F05xxD has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Table 35-1. Soldering Conditions of Conventional-specification Products (μPD78F05xx and 78F05xxD) (3/3)

(3) 30-pin plastic SSOP (7.62 mm (300))

μPD78F050xMC(A)-CAB-AX (x = 0 to 3), 78F050xMC(A2)-CAB-AX (x = 0 to 3)

44-pin plastic LQFP (10x10)

μPD78F051xGB(A)-GAF-AX (x = 1 to 3), 78F051xGB(A2)-GAF-AX (x = 1 to 3)

52-pin plastic LQFP (10x10)

μPD78F052xGB(A)-GAG-AX (x = 1 to 7), 78F052xGB(A2)-GAG-AX (x = 1 to 7)

64-pin plastic LQFP (14x14)

μPD78F053xGC(A)-GAL-AX (x = 1 to 7), 78F053xGC(A2)-GAL-AX (x = 1 to 7)

64-pin plastic LQFP (12x12)

μPD78F053xGK(A)-GAJ-AX (x = 1 to 7), 78F053xGK(A2)-GAJ-AX (x = 1 to 7)

80-pin plastic LQFP (14x14)

μPD78F054xGC(A)-GAD-AX (x = 4 to 7), 78F054xGC(A2)-GAD-AX (x = 4 to 7)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	WS60-207-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

C.2 Register Index (In Alphabetical Order with Respect to Register Symbol)

(26/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 24	Soft	Power-on-clear circuit	In 2.7 V/1.59 V POC mode	A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the supply voltage reaches 1.59 V (TYP.). If the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) within 1.93 ms, the power supply oscillation stabilization time of 0 to 5.39 ms is automatically generated before reset processing.	p. 695 ☐
			Cautions for power-on-clear circuit	In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.	p. 696 ☐
Chapter 25	Soft	Low-voltage detector	LVIM: Low-voltage detection register	To stop LVI, follow either of the procedures below. • When using 8-bit memory manipulation instruction: Write 00H to LVIM. • When using 1-bit memory manipulation instruction: Clear LVION to 0.	p. 700 ☐
	Hard			Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.	p. 700 ☐
	Soft			When using LVI as an interrupt, if LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.	p. 701 ☐
			LVIM and LVIS	With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.	p. 701 ☐
			LVIS: Low-voltage detection level selection register	Be sure to clear bits 4 to 7 to "0".	p. 701 ☐
				Do not change the value of LVIS during LVI operation.	p. 701 ☐
				When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.	p. 701 ☐
				With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.	p. 701 ☐
			When used as reset (When detecting level of supply voltage (V_{DD}))	<1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <4>.	p. 703 ☐
				If supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.	p. 703 ☐
			When used as reset (When detecting level of input voltage from external input pin (EXLVI))	<1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.	p. 706 ☐
				If input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.)) when LVIMD is set to 1, an internal reset signal is not generated.	p. 706 ☐
	Hard			Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.	p. 706 ☐
			When used as interrupt (When detecting level of input voltage from external input pin (EXLVI))	Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.	p. 711 ☐
	Soft		Cautions for low-voltage detector	In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used. (1) When used as reset The system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking action (1) below. (2) When used as interrupt Interrupt requests may be frequently generated. Take (b) of action (2) below.	p. 713 ☐
Chapter 26	Soft	Option byte	0082H, 0083H/1082H, 1083H	Be sure to set 00H to 0082H and 0083H (0082H/1082H and 0083H/1083H when the boot swap function is used).	p. 716 ☐
			0080H/1080H	Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.	p. 716 ☐

APPENDIX E REVISION HISTORY

E.1 Major Revisions in This Edition

Page	Description	Classification
R01UH0008EJ0400 → R01UH0008EJ0401		
pp. 97, 396, 399, 722, 723	Deletion of **Note**	(c)
p. 93	Change of Recommended Connection of Unused Pins of FLMD0 pin in **Table 2-3. Pin I/O Circuit Types**	(a)
p. 135	Change of **Note 2** of **Table 3-8. Special Function Register List (5/5)**	(c)
U18598JJ3V0UD00 → R01UH0008EJ0400		
Throughout	Deletion of "**recommended**" from **Caution** "**Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: recommended).**"	(c)
CHAPTER 1 OUTLINE		
p. 41	Change of status of **64-pin plastic FBGA (4x4)** of **78K0/KE2** from under development to mass production	(b)
CHAPTER 2 PIN FUNCTIONS		
p. 69	Change of **2. 1. 3 78K0/KD2 (2) Non-port functions: 78K0/KD2**	(c)
pp. 72, 73	Change of **2. 1. 4 78K0/KE2 (2) Non-port functions: 78K0/KE2**	(c)
p. 93	Change of **Table 2-3. Pin I/O Circuit Types (3/3)**	(c)
CHAPTER 6 CLOCK GENERATOR		
p. 230	Change of **Caution 2** in **Figure 6-3. Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KB2)**	(a)
p. 231	Change of **Caution 2** in **Figure 6-4. Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)**	(a)
p. 259	Change of **Figure 6-18. CPU Clock Status Transition Diagram (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0), 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)**	(c)
CHAPTER 7 16-BIT TIMER/EVENT COUNTERS 00 AND 01		
p. 299	Change of **Caution** in **7.4.4 Operation in clear & start mode entered by TI00n pin valid edge input**	(c)
CHAPTER 18 SERIAL INTERFACE IIC0		
p. 553	Addition of **Caution** to **Figure 18-3. Format of IIC Shift Register 0 (IIC0)**	(c)
p. 553	Change of description of **18.2 (2) Slave address register 0 (SVA0)**	(c)
p. 557	Addition of **Note** to **Figure 18-5. Format of IIC Control Register 0 (IICC0) (1/4)** and change of **Caution**	(c)
p. 559	Change of **Figure 18-5. Format of IIC Control Register 0 (IICC0) (3/4)**	(c)
p. 560	Change of **Figure 18-5. Format of IIC Control Register 0 (IICC0) (4/4)**	(c)
p. 562	Change of **Figure 18-6. Format of IIC Status Register 0 (IICS0) (2/3)**	(c)
CHAPTER 20 INTERRUPT FUNCTIONS		
p. 634	Change of **(C) External maskable interrupt (INTKR)** in **Figure 20-1 Basic Configuration of Interrupt Function**	(c)
CHAPTER 22 STANDBY FUNCTION		
p. 673	Addition of **Note** to **Figure 22-4. HALT Mode Release by Reset**	(c)
p. 680	Addition of **Note** to **Figure 22-7. STOP Mode Release by Reset**	(c)
CHAPTER 27 FLASH MEMORY		
p. 730	Change of description of **27.6.5 REGC pin**	(c)
p. 755	Addition of **27.11 Creating ROM Code to Place Order for Previously Written Product**	(c)
APPENDIX E REVISION HISTORY		
p. 975	Addition of **C.2 Revision History of Preceding Editions**	(c)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents