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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFLGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0534afc-aa1-a

2.1.3 78K0/KD2

(1) Port functions (1/2): 78K0/KD2

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P02				–
P03				–
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0 to ANI7
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1
P31				INTP2/OCD1A[Note]
P32				INTP3/OCD1B[Note]
P33				TI51/TO51/INTP4
P40, P41	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P60	I/O	Port 6. 4-bit I/O port. Output is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P62				EXSCL0
P63				–
P70 to P77	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR7
P120	I/O	Port 12. 5-bit I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121				X1/OCD0A[Note]
P122				X2/EXCLK/ OCD0B[Note]
P123				XT1
P124				XT2/EXCLKS

Note μPD78F0527D and 78F0527DA (product with on-chip debug function) only

2.2.11 P140 to P145 (port 14)

P140 to P145 function as an I/O port. These pins also function as external interrupt request input, clock output, buzzer output, serial interface data I/O, clock I/O, busy input, and strobe output pins.

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P140/PCL/INTP6	–	√Note 1	√	√		√
P141/BUZ/BUSY0/INTP7	–	–	–	P141/BUZ/INTP7Note 2		√
P142/$\overline{\text{SCKA0}}$	–	–	–	–		√
P143/SIA0	–	–	–	–		√
P144/SOA0	–	–	–	–		√
P145/STB0	–	–	–	–		√

Notes 1. This is not mounted onto 38-pin and 44-pin products of the 78K0/KC2.

2. The 78K0/KE2 products are not provided with the BUSY0 input function.

Remark √: Mounted, –: Not mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P140 to P145 function as an I/O port. P140 to P145 can be set to input or output port in 1-bit units using port mode register 14 (PM14). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 14 (PU14).

(2) Control mode

P140 to P145 function as external interrupt request input, clock output, buzzer output, serial interface data I/O, clock I/O, busy input, and strobe output pins.

(a) INTP6, INTP7

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) PCL

This is a clock output pin.

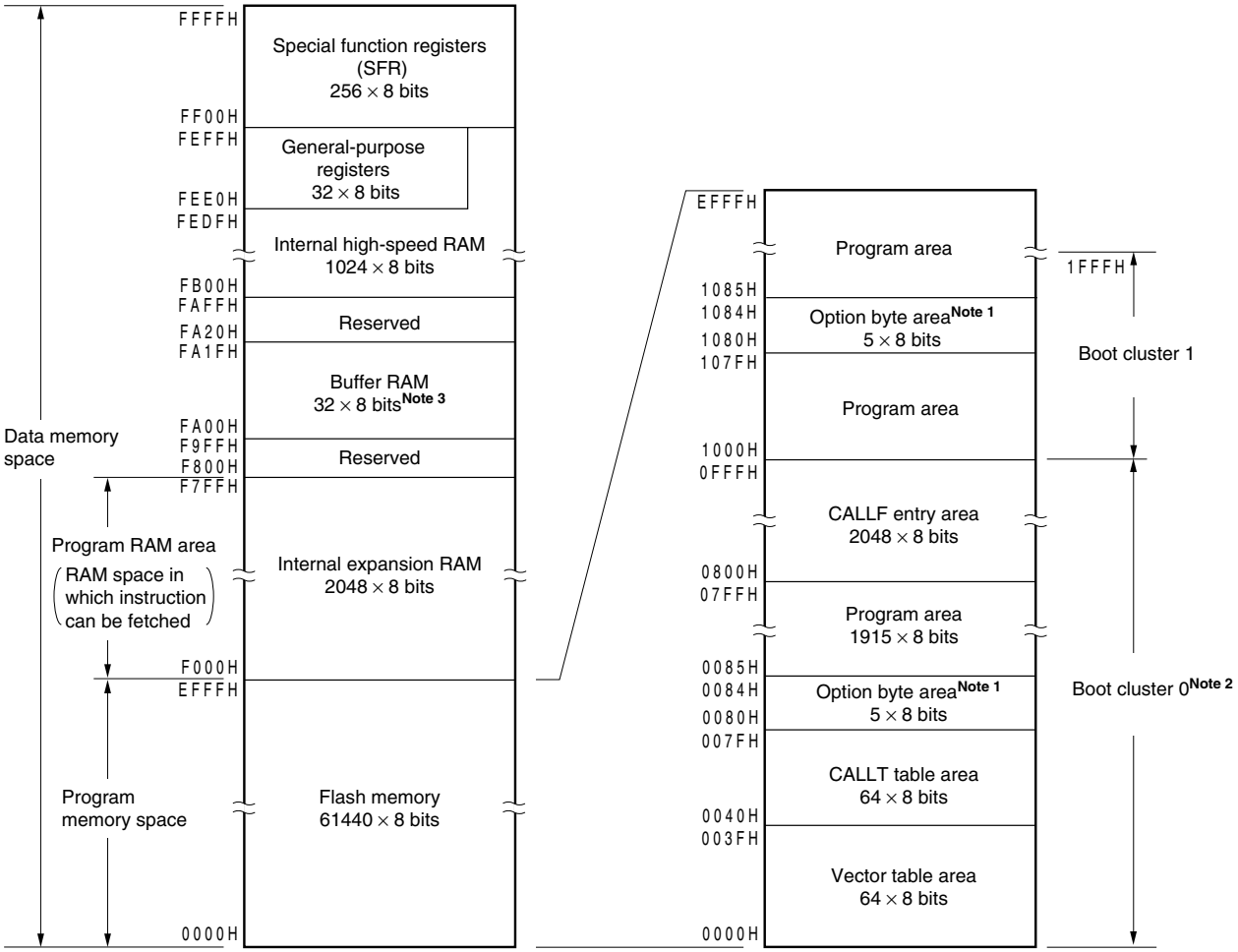
(c) BUZ

This is a buzzer output pin.

(d) BUSY0

This is a serial interface CSIA0 busy input pin.

Figure 3-7. Memory Map (μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, 78F0535A, 78F0545, and 78F0545A)

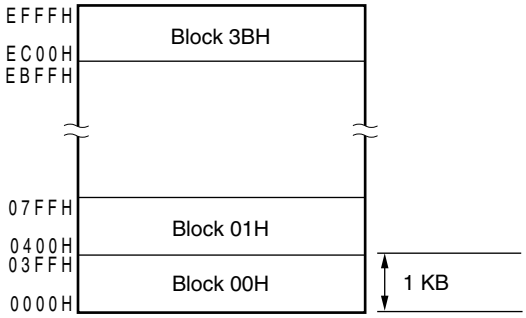


Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H.
When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

3. The buffer RAM is incorporated only in the μPD78F0545 and 78F0545A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, and 78F0535A.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.



3.2 Processor Registers

The 78K0/Kx2 microcontrollers incorporate the following processor registers.

3.2.1 Control registers

The control registers control the program sequence, statuses and stack memory. The control registers consist of a program counter (PC), a program status word (PSW) and a stack pointer (SP).

(1) Program counter (PC)

The program counter is a 16-bit register that holds the address information of the next program to be executed.

In normal operation, PC is automatically incremented according to the number of bytes of the instruction to be fetched.

When a branch instruction is executed, immediate data and register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-20. Format of Program Counter

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags set/reset by instruction execution.

Program status word contents are stored in the stack area upon vectored interrupt request acknowledgement or PUSH PSW instruction execution and are restored upon execution of the RETB, RETI and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 3-21. Format of Program Status Word

	7							0
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY

(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledge operations of the CPU.

When 0, the IE flag is set to the interrupt disabled (DI) state, and all maskable interrupt requests are disabled.

When 1, the IE flag is set to the interrupt enabled (EI) state and interrupt request acknowledgment is controlled with an in-service priority flag (ISP), an interrupt mask flag for various interrupt sources, and a priority specification flag.

The IE flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

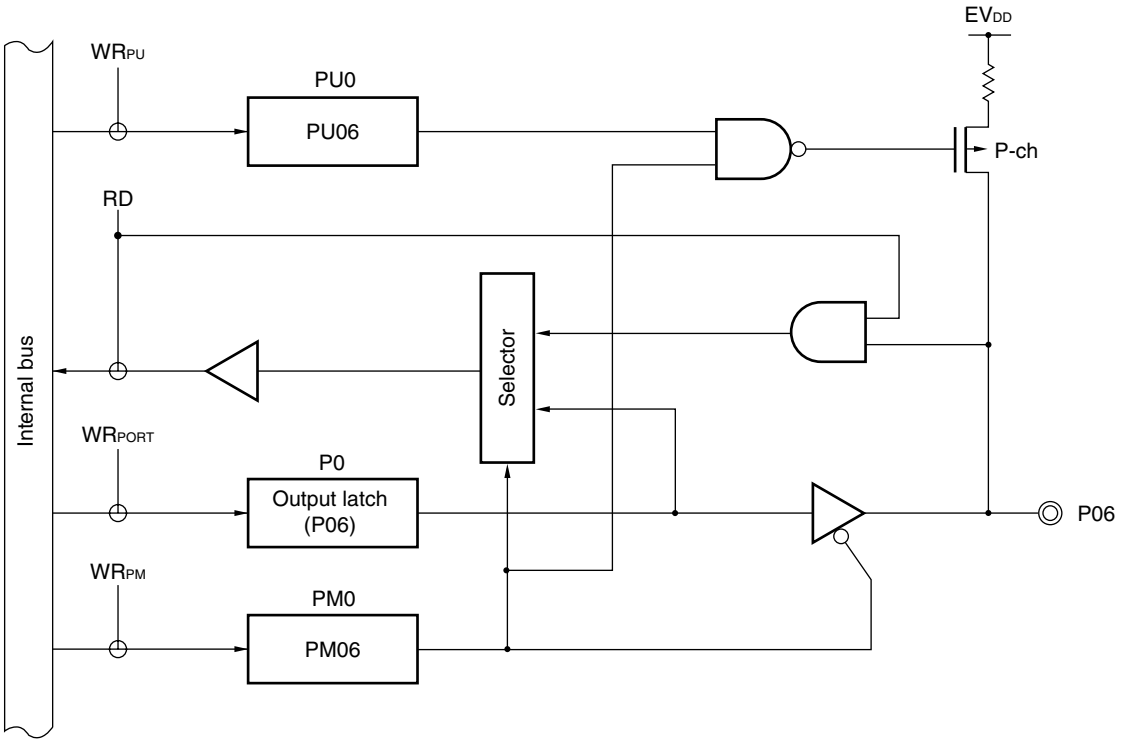
(c) Register bank select flags (RBS0 and RBS1)

These are 2-bit flags to select one of the four register banks.

In these flags, the 2-bit information that indicates the register bank selected by SEL RBn instruction execution is stored.

Figure 5-6. Block Diagram of P06 (1/2)

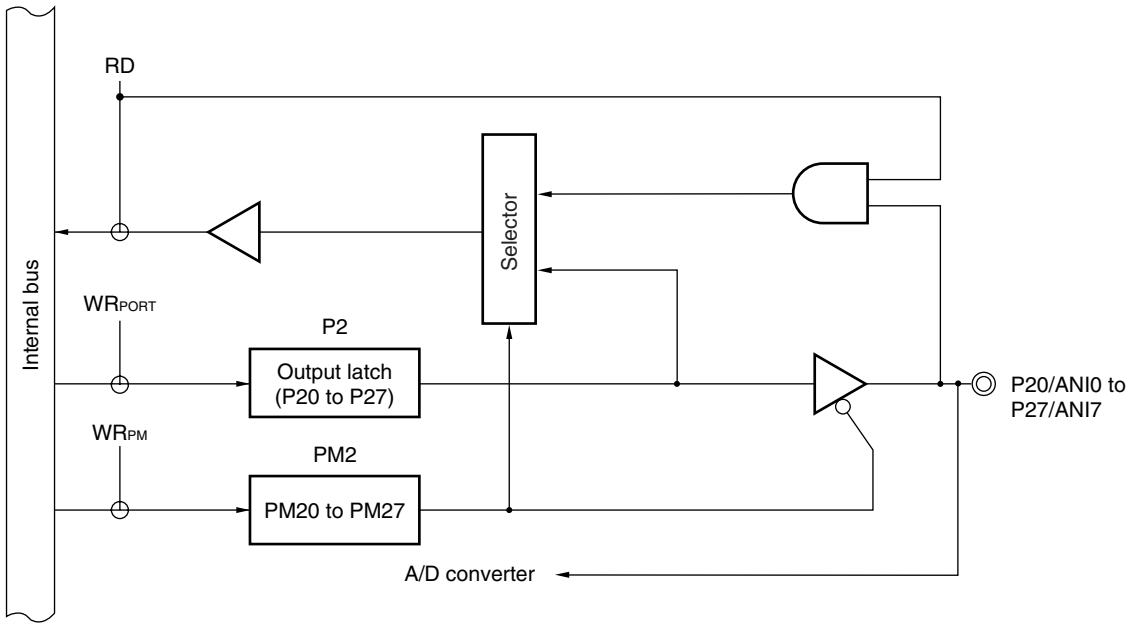
(1) 78K0/KE2 products whose flash memory is less than 32 KB



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

Figure 5-12. Block Diagram of P20 to P27

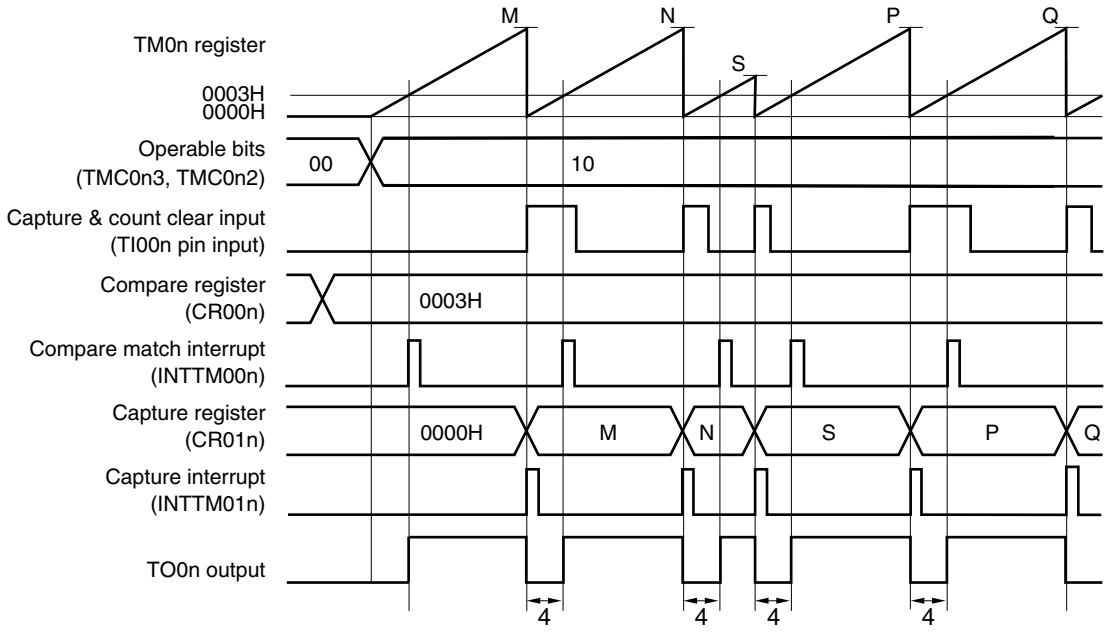


P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Caution For the 38-pin products of 78K0/KC2, be sure to set bits 6 and 7 of PM2 to "1", and bits 6 and 7 of P2 to "0".

Figure 7-30. Timing Example of Clear & Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Compare Register, CR01n: Capture Register) (2/2)

(b) TOC0n = 13H, PRM0n = 10H, CRC0n, = 04H, TMC0n = 0AH, CR00n = 0003H



This is an application example where the width set to CR00n (4 clocks in this example) is to be output from the TO0n pin when the count value has been captured & cleared.

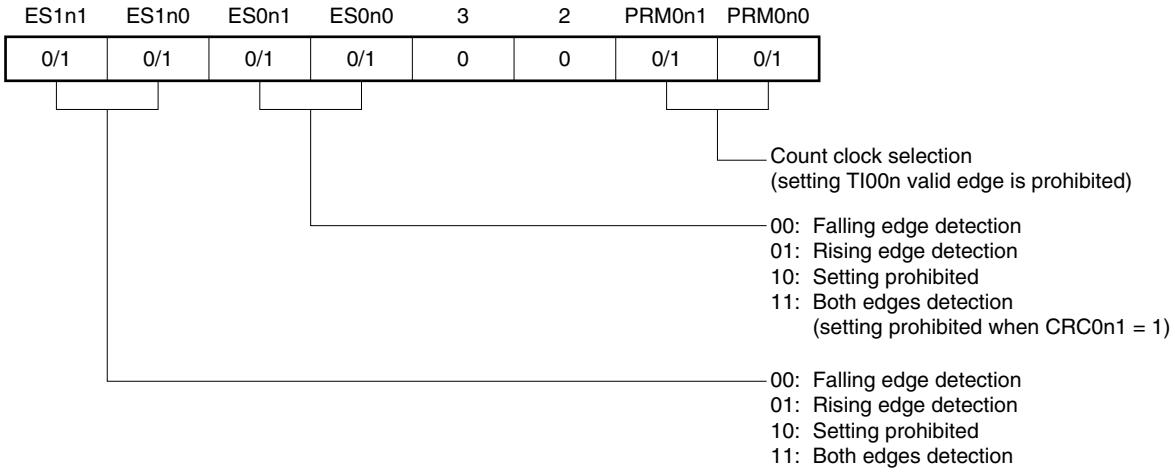
The count value is captured to CR01n, a capture interrupt signal (INTTM01n) is generated, TM0n is cleared (to 0000H), and the TO0n output level is inverted when the valid edge of the TI00n pin is detected. When the count value of TM0n is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM00n) is generated and the TO0n output level is inverted.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-43. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 0n (PRM0n)



(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM00n) is generated. The count value of TM0n is not cleared.

To use this register as a capture register, select either the TI00n or TI01n pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR00n.

(g) 16-bit capture/compare register 01n (CR01n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM01n) is generated. The count value of TM0n is not cleared.

When this register is used as a capture register, the TI00n pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR01n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Notes 2. Set the serial clock to satisfy the following conditions.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD) and Expanded-specification Products (μPD78F05xxA and 78F05xxDA)		
	Standard Products	(A) Grade Products	(A2) Grade Products
4.0 V ≤ V_{DD} ≤ 5.5 V	Serial clock ≤ 6.25 MHz	Serial clock ≤ 5 MHz	Serial clock ≤ 5 MHz
2.7 V ≤ V_{DD} < 4.0 V	Serial clock ≤ 4 MHz	Serial clock ≤ 2.5 MHz	Serial clock ≤ 2.5 MHz
1.8 V ≤ V_{DD} < 2.7 V	Serial clock ≤ 2 MHz	Serial clock ≤ 1.66 MHz	–

3. Do not start communication with the external clock from the $\overline{SCK11}$ pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. Do not write to CSIC11 while CSIE11 = 1 (operation enabled).

2. To use P02/SO11 and P04/$\overline{SCK11}$ as general-purpose ports, set CSIC11 in the default status (00H).

3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock frequency

(3) Port mode registers 0 and 1 (PM0, PM1)

These registers set port 0 and 1 input/output in 1-bit units.

When using P10/$\overline{SCK10}$ and P04/$\overline{SCK11}$ as the clock output pins of the serial interface, clear PM10 and PM04 to 0, and set the output latches of P10 and P04 to 1.

When using P12/SO10 and P02/SO11 as the data output pins of the serial interface, clear PM12, PM02, and the output latches of P12 and P02 to 0.

When using P10/$\overline{SCK10}$ and P04/$\overline{SCK11}$ as the clock input pins of the serial interface, P11/SI10/RxD0 and P03/SI11 as the data input pins, and P05/$\overline{SSI11}$/TI001 as the chip select input pin, set PM10, PM04, PM11, PM03, and PM05 to 1. At this time, the output latches of P10, P04, P11, P03, and P05 may be 0 or 1.

PM0 and PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 16-7. Format of Port Mode Register 0 (PM0)

Address: FF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

PM0n	P0n pin I/O mode selection (n = 0 to 6)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 0 of 78K0/KF2 products. For the format of port mode register 0 of other products, see **(1) Port mode registers (PMxx)** in **5.3 Registers Controlling Port Function**.

Figure 18-2 shows a serial bus configuration example.

Figure 18-2. Serial Bus Configuration Example Using I²C Bus

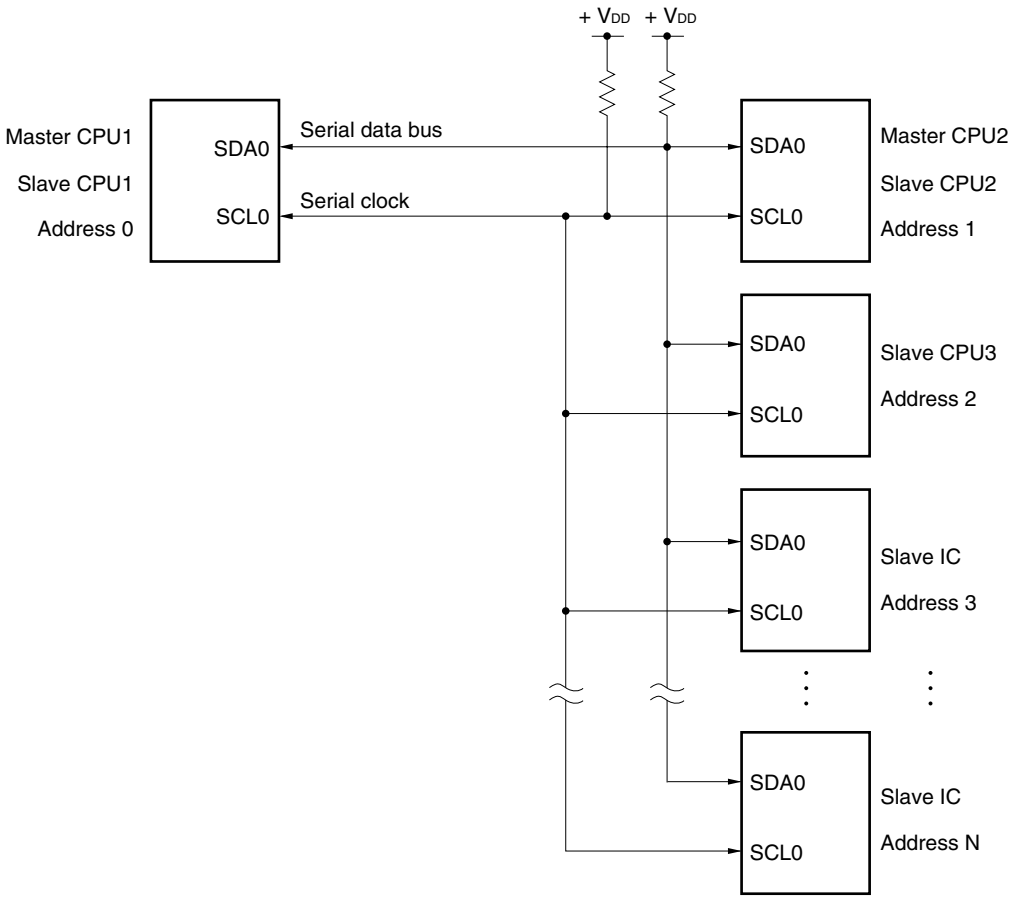


Figure 18-5. Format of IIC Control Register 0 (IICC0) (2/4)

SPIE0[Note 1]	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable

Condition for clearing (SPIE0 = 0)	Condition for setting (SPIE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

WTIM0[Note 1]	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and wait is set. Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.
An interrupt is generated at the falling edge of the ninth clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an acknowledge ($\overline{ACK}$) is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.	

Condition for clearing (WTIM0 = 0)	Condition for setting (WTIM0 = 1)
• Cleared by instruction • Reset	• Set by instruction

ACKE0[Notes 1, 2]	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDA0 line is set to low level.

Condition for clearing (ACKE0 = 0)	Condition for setting (ACKE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

Notes 1. This flag's signal is invalid when IICE0 = 0.

2. The set value is invalid during address transfer and if the code is not an extension code.
When the device serves as a slave and the addresses match, an acknowledge is generated regardless of the set value.

(4) IIC clock selection register 0 (IICCL0)

This register is used to set the transfer clock for the I^2C bus.

IICCL0 is set by a 1-bit or 8-bit memory manipulation instruction. However, the CLD0 and DAD0 bits are read-only.

The SMC0, CL01, and CL00 bits are set in combination with bit 0 (CLX0) of IIC function expansion register 0 (IICX0) (see **18.3 (6) I^2C transfer clock setting method**).

Set IICCL0 while bit 7 (IICE0) of IIC control register 0 (IICC0) is 0.

Reset signal generation clears IICCL0 to 00H.

Figure 18-8. Format of IIC Clock Selection Register 0 (IICCL0)

Address: FFA8H After reset: 00H R/W[Note]

Symbol	7	6	<5>	<4>	<3>	<2>	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

CLD0	Detection of SCL0 pin level (valid only when IICE0 = 1)
0	The SCL0 pin was detected at low level.
1	The SCL0 pin was detected at high level.

Condition for clearing (CLD0 = 0)	Condition for setting (CLD0 = 1)
• When the SCL0 pin is at low level • When IICE0 = 0 (operation stop) • Reset	• When the SCL0 pin is at high level

DAD0	Detection of SDA0 pin level (valid only when IICE0 = 1)
0	The SDA0 pin was detected at low level.
1	The SDA0 pin was detected at high level.

Condition for clearing (DAD0 = 0)	Condition for setting (DAD0 = 1)
• When the SDA0 pin is at low level • When IICE0 = 0 (operation stop) • Reset	• When the SDA0 pin is at high level

SMC0	Operation mode switching
0	Operates in standard mode.
1	Operates in high-speed mode.

DFC0	Digital filter operation control
0	Digital filter off.
1	Digital filter on.
Digital filter can be used only in high-speed mode. In high-speed mode, the transfer clock does not vary regardless of DFC0 bit set (1)/clear (0). The digital filter is used for noise elimination in high-speed mode.	

Note Bits 4 and 5 are read-only.

Remark IICE0: Bit 7 of IIC control register 0 (IICC0)

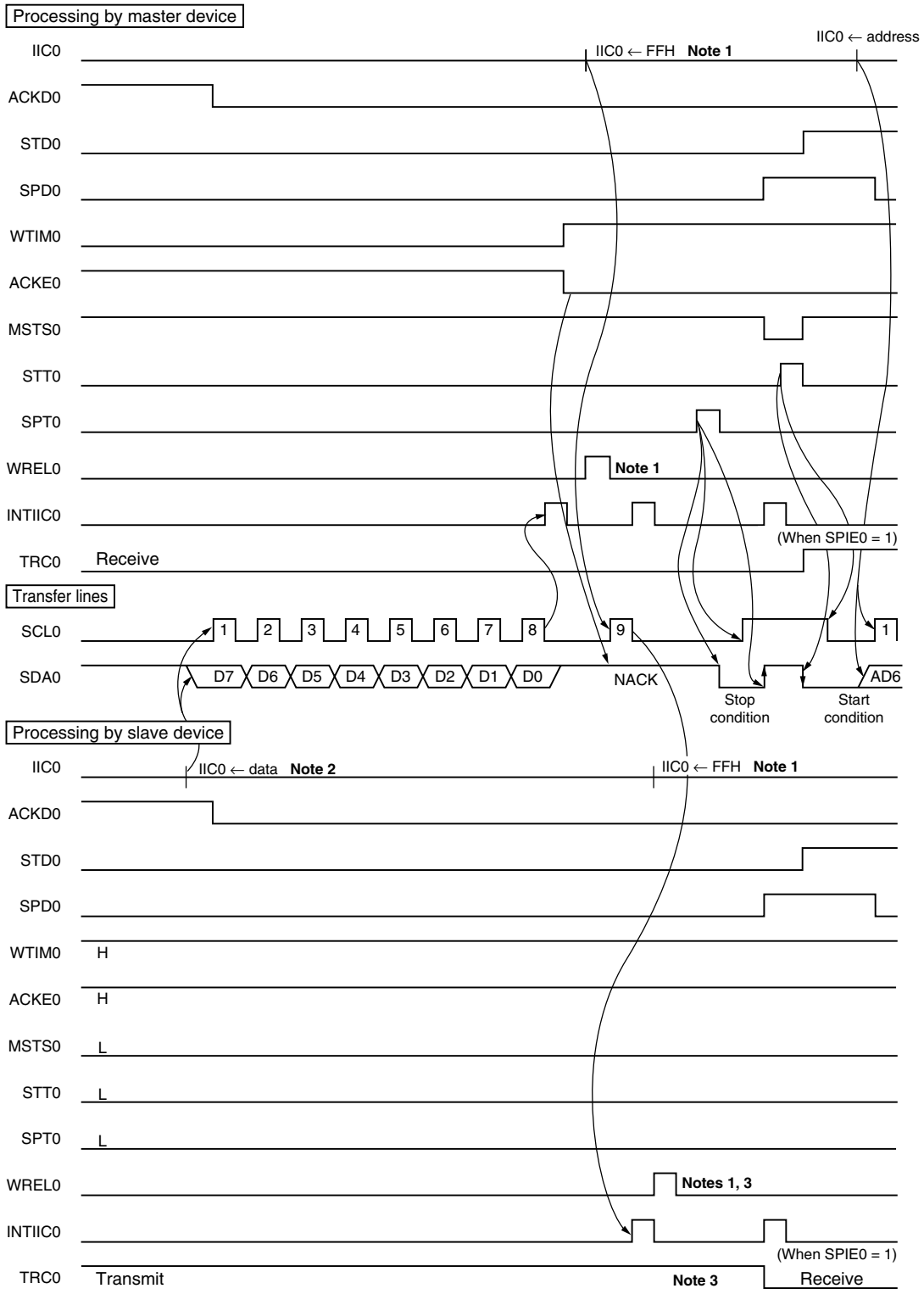
18.5.17 Timing of I²C interrupt request (INTIIC0) occurrence

The timing of transmitting or receiving data and generation of interrupt request signal INTIIC0, and the value of the IICS0 register when the INTIIC0 signal is generated are shown below.

Remark ST: Start condition
AD6 to AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7 to D0: Data
SP: Stop condition

Figure 18-28. Example of Slave to Master Communication
(When 8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Stop condition



Notes 1. To cancel wait, write “FFH” to IIC0 or set WREL0.

2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

3. If a wait state during slave transmission is canceled by setting WREL0, TRC0 will be cleared.

19.3 Register Controlling Multiplier/Divider

The multiplier/divider is controlled by multiplier/divider control register 0 (DMUC0).

(1) Multiplier/divider control register 0 (DMUC0)

DMUC0 is an 8-bit register that controls the operation of the multiplier/divider.

DMUC0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears DMUC0 to 00H.

Figure 19-5. Format of Multiplier/Divider Control Register 0 (DMUC0)

Address: FF68H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
DMUC0	DMUE	0	0	0	0	0	0	DMUSEL0

DMUE[Note]	Operation start/stop
0	Stops operation
1	Starts operation

DMUSEL0	Operation mode (multiplication/division) selection
0	Division mode
1	Multiplication mode

Note When DMUE is set to 1, the operation is started. DMUE is automatically cleared to 0 after the operation is complete.

Cautions 1. If DMUE is cleared to 0 during operation processing (when DMUE is 1), the operation result is not guaranteed. If the operation is completed while the clearing instruction is being executed, the operation result is guaranteed, provided that the interrupt flag is set.

2. Do not change the value of DMUSEL0 during operation processing (while DMUE is 1). If it is changed, undefined operation results are stored in multiplication/division data register A0 (MDA0) and remainder data register 0 (SDR0).

3. If DMUE is cleared to 0 during operation processing (while DMUE is 1), the operation processing is stopped. To execute the operation again, set multiplication/division data register A0 (MDA0), multiplication/division data register B0 (MDB0), and multiplier/divider control register 0 (DMUC0), and start the operation (by setting DMUE to 1).

19.4.2 Division operation

- Initial setting
  1. Set operation data to multiplication/division data register A0 (MDA0L and MDA0H) and multiplication/division data register B0 (MDB0).
  2. Set bits 0 (DMUSEL0) and 7 (DMUE) of multiplier/divider control register 0 (DMUC0) to 0 and 1, respectively. Operation will start.
- During operation
  3. The operation will be completed when 32 peripheral hardware clocks (f_{PRS}) have been issued after the start of the operation (intermediate data is stored in the MDA0L and MDA0H registers and remainder data register 0 (SDR0) during operation, and therefore the read values of these registers are not guaranteed).
- End of operation
  4. The result data is stored in the MDA0L, MDA0H, and SDR0 registers.
  5. DMUE is cleared to 0 (end of operation).
  6. After the operation, an interrupt request signal (INTDMU) is generated.
- Next operation
  7. To execute multiplication next, start from the initial setting in **19.4.1 Multiplication operation**.
  8. To execute division next, start from the initial setting in **19.4.2 Division operation**.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	−10	mA
		Total of all pins −80 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	−25	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P64 to P67, P70 to P77	−55	mA
		Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
		Per pin	P121 to P124	−1	mA
		Total of all pins		−4	mA
Output current, low	I_{OL}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P130, P140 to P145	30	mA
		Total of all pins 200 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	60	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P60 to P67, P70 to P77	140	mA
		Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
		Per pin	P121 to P124	4	mA
		Total of all pins		10	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Cautions 1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Non-port functions

Port		78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
		30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Power supply, ground		V_{DD}, EV_{DD}[Note 1], V_{SS}, EV_{SS}[Note 1], AV_{REF}, AV_{SS}	V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, V_{SS}, EV_{SS}, AV_{REF}, AV_{SS}	
Regulator		REGC						
Reset		$\overline{\text{RESET}}$						
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK, EXCLKS					
Writing to flash memory		FLMD0						
Interrupt		INTP0 to INTP5			INTP0 to INTP6		INTP0 to INTP7	
Key interrupt		–	KR0, KR1	KR0 to KR3		KR0 to KR7		
Timer	TM00	TI000, TI010, TO00						
	TM01	–					TI001[Note 2], TI011[Note 2], TO01[Note 2]	
	TM50	TI50, TO50						
	TM51	TI51, TO51						
	TMH0	TOH0						
	TMH1	TOH1						
Serial interface	UART0	RxD0, TxD0						
	UART6	RxD6, TxD6						
	IIC0	SCL0, SDA0	SCL0, SDA0, EXSCL0					
	CSI10	$\overline{\text{SCK10}}$, SI10, SO10						
	CSI11	–					$\overline{\text{SCK11}}$[Note 2], SI11[Note 2], SO11[Note 2], $\overline{\text{SSI11}}$[Note 2]	
	CSIA0	–						$\overline{\text{SCKA0}}$, SIA0, SOA0, BUSY0, STB0
A/D converter		ANI0 to ANI3	ANI0 to ANI5	ANI0 to ANI7				
Clock output		–			PCL			
Buzzer output		–					BUZ	
Low-voltage detector (LVI)		EXLVI						

Notes 1. This is not mounted onto 30-pin products.

2. This is not mounted onto the 78K0/KE2 products whose flash memory is less than 32 KB.

Table 36-2. RAM Accesses That Generate Wait and Number of CPU Wait Clocks (78K0/KF2 only)

Area	Access	Number of Wait Clocks
Buffer RAM	Write	1 to 81 clocks[Note]
<Calculating maximum number of wait clocks> • Maximum number of wait clocks = $\frac{5 f_{CPU}}{f_W} + 1$ * Fraction is truncated if the number of wait clocks multiplied by ($1/f_{CPU}$) is equal or lower than t_{CPUL} and rounded up if higher than t_{CPUL}. f_W: Frequency of base clock selected by CKS00 bit of CSIS0 register (CKS00 = 0: f_{PRS}, CKS00 = 1: $f_{PRS}/2$) f_{CPU}: CPU clock frequency t_{CPUL}: CPU clock low-level width f_{PRS}: Peripheral hardware clock frequency		

Note No waits are generated when five CSIA0 operating clocks or more are inserted between writing to the RAM from the CSIA0 and writing to the buffer RAM from the CPU.

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 6	Hard	Clock generator operation when power supply voltage is turned on	–	It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK and EXCLKS pins is used.	pp. 246, 247 ☐
				A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the power supply voltage reaches 1.59 V (TYP.). If the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) within 1.93 ms, the power supply oscillation stabilization time of 0 to 5.39 ms is automatically generated before reset processing.	p. 247 ☐
	Soft	Controlling high-speed system clock	X1/P121 and X2/EXCLK/P122	The X1/P121 and X2/EXCLK/P122 pins are in the I/O port mode after a reset release.	p. 248 ☐
			X1 clock	Do not change the value of EXCLK and OSCSEL while the X1 clock is operating.	p. 249 ☐
				Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS : T_A = • 40 to +125°C)).	p. 249 ☐
			External main system clock	Do not change the value of EXCLK and OSCSEL while the external main systerm clock is operating.	p. 249 ☐
				Set the external main system clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS : T_A = • 40 to +125°C)).	p. 249 ☐
			Main system clock	If the high-speed system clock is selected as the main system clock, a clock other than the high-speed system clock cannot be set as the peripheral hardware clock.	p. 250 ☐
			High-speed system clock	Be sure to confirm that MCS = 0 or CLS = 1 when setting MSTOP to 1. In addition, stop peripheral hardware that is operating on the high-speed system clock.	p. 251 ☐
			Internal high-speed oscillation clock	Be sure to confirm that MCS = 1 or CLS = 1 when setting RSTOP to 1. In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock.	p. 253 ☐
			XT1/P123, XT2/EXCLKS/ P124	The XT1/P123 and XT2/EXCLKS/P124 pins are in the I/O port mode after a reset release.	p. 254 ☐
			External clock from peripheral hardware pins	Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.	p. 254 ☐
			XT1 clock, external subsystem clock	Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.	p. 254 ☐
			Subsystem clock	Be sure to confirm that CLS = 0 when clearing OSCSELS to 0. In addition, stop the watch timer if it is operating on the subsystem clock.	p. 255 ☐
				The subsystem clock oscillation cannot be stopped using the STOP instruction.	p. 255 ☐
		Controlling internal low-speed oscillation clock	Internal low-speed oscillation clock	If “Internal low-speed oscillator cannot be stopped” is selected by the option byte, oscillation of the internal low-speed oscillation clock cannot be controlled.	p. 256 ☐