Renesas Electronics America Inc - UPD78F0534AGK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0534agk-gaj-ax

(2) Non-port functions (1/2): 78K0/KB2

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI3	Input	A/D converter analog input	Analog input	P20 to P23
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
FLMD0	–	Flash memory programming mode setting	–	–
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P30
INTP2				P31/OCD1A[Note]
INTP3				P32/OCD1B[Note]
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
REGC	–	Connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI10
RxD6	Input	Serial data input to UART6	Input port	P14
TxD0	Output	Serial data output from UART0	Input port	P10/$\overline{\text{SCK10}}$
TxD6	Output	Serial data output from UART6	Input port	P13
$\overline{\text{SCK10}}$	I/O	Clock input/output for CSI10	Input port	P10/TxD0
SI10	Input	Serial data input to CSI10		P11/RxD0
SO10	Output	Serial data output from CSI10		P12
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SDA0		Serial data I/O for I^2C		P61
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00
TI010	Input	Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00	Input port	P01/TO00
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TI010
TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50
TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
TOH0	Output	8-bit timer H0 output	Input port	P15
TOH1		8-bit timer H1 output		P16/INTP5
X1	–	Connecting resonator for main system clock	Input port	P121/OCD0A[Note]
X2	–		Input port	P122/EXCLK/OCD0B[Note]
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/OCD0B[Note]

Note μPD78F0503D and 78F0503DA (product with on-chip debug function) only

Table 5-3. Port Functions (2/3)

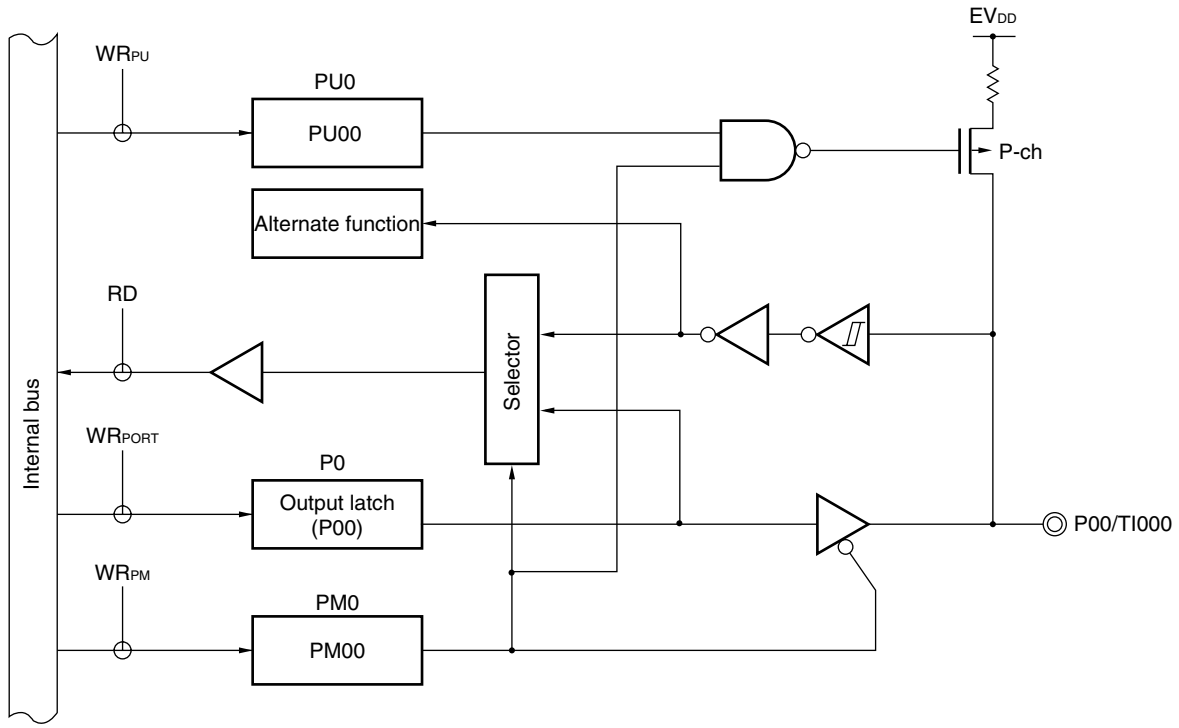
KB2	KC2	KD2	KES	KF2	Function Name	I/O	Function	After Reset	Alternate Function
–	Note 1	√	√	√	P40	I/O	Port 4. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
–	Note 1	√	√	√	P41				–
–	–	–	√	√	P42				–
–	–	–	√	√	P43				–
–	–	–	–	√	P44				–
–	–	–	–	√	P45				–
–	–	–	–	√	P46				–
–	–	–	–	√	P47				–
–	–	–	√	√	P50	I/O	Port 5. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
–	–	–	√	√	P51				–
–	–	–	√	√	P52				–
–	–	–	√	√	P53				–
–	–	–	–	√	P54				–
–	–	–	–	√	P55				–
–	–	–	–	√	P56				–
–	–	–	–	√	P57				–
√	√	√	√	√	P60	I/O	Port 6. I/O port. Output of P60 to P63 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units. Only for P64 to P67, use of an on-chip resistor can be specified by a software setting.	Input port	SCL0
√	√	√	√	√	P61				SDA0
–	√	√	√	√	P62				EXSCL0
–	√	√	√	√	P63				–
–	–	–	–	√	P64				–
–	–	–	–	√	P65				–
–	–	–	–	√	P66				–
–	–	–	–	√	P67				–
–	√	√	√	√	P70	I/O	Port 7. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0
–	√	√	√	√	P71				KR1
–	Note 1	√	√	√	P72				KR2
–	Note 1	√	√	√	P73				KR3
–	Note 2	√	√	√	P74				KR4
–	Note 2	√	√	√	P75				KR5
–	–	√	√	√	P76				KR6
–	–	√	√	√	P77				KR7

Notes 1. This is not mounted onto 38-pin products of the 78K0/KC2. For the 38-pin products, be sure to set bits 0 and 1 of PM4, bits 2 and 3 of PM7, bits 0 and 1 of P4, and bits 2 and 3 of P7 to “0”.

2. This is not mounted onto 38-pin and 44-pin products of the 78K0/KC2. The 48-pin products are only provided with port functions (P74 to P75) and not alternate functions.

Remark √: Mounted, –: Not mounted

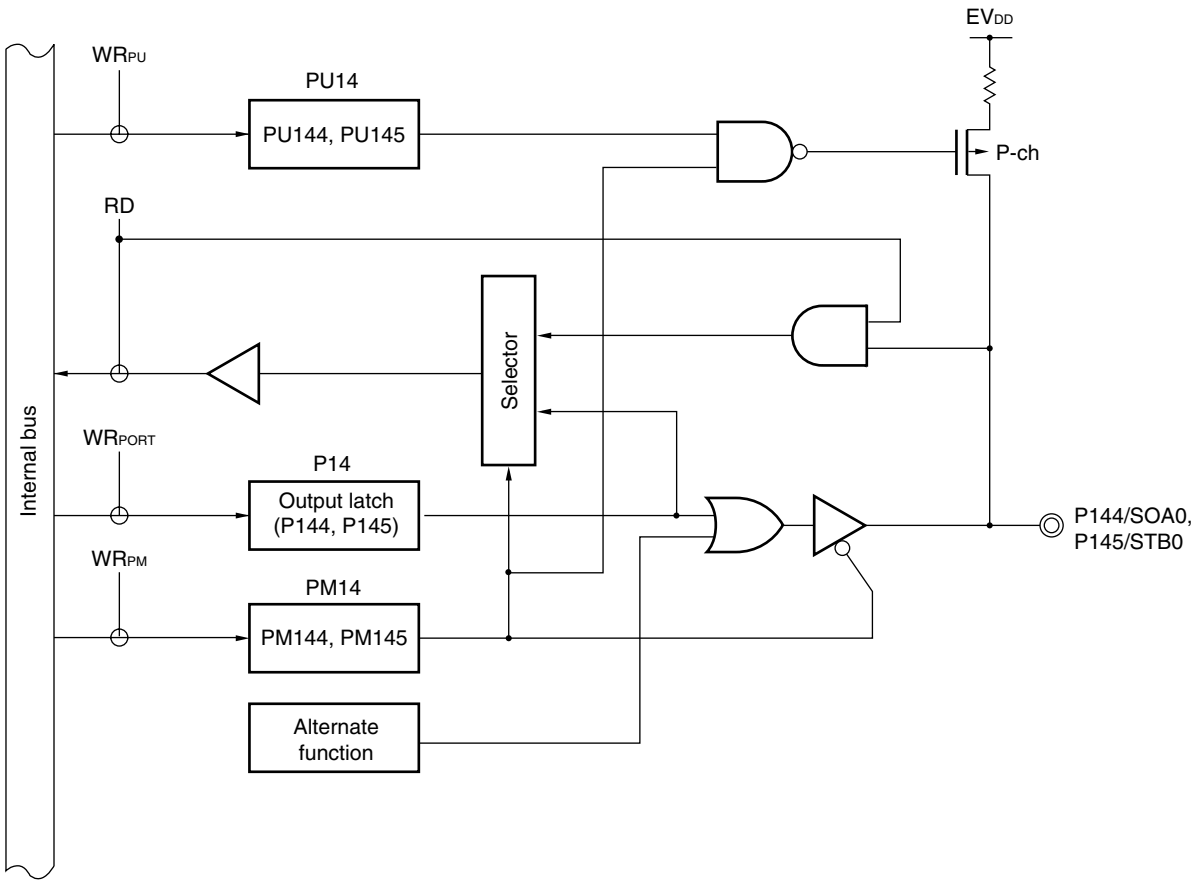
Figure 5-1. Block Diagram of P00



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-28. Block Diagram of P144 and P145



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

5.3 Registers Controlling Port Function

Port functions are controlled by the following four types of registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- A/D port configuration register (ADPC)

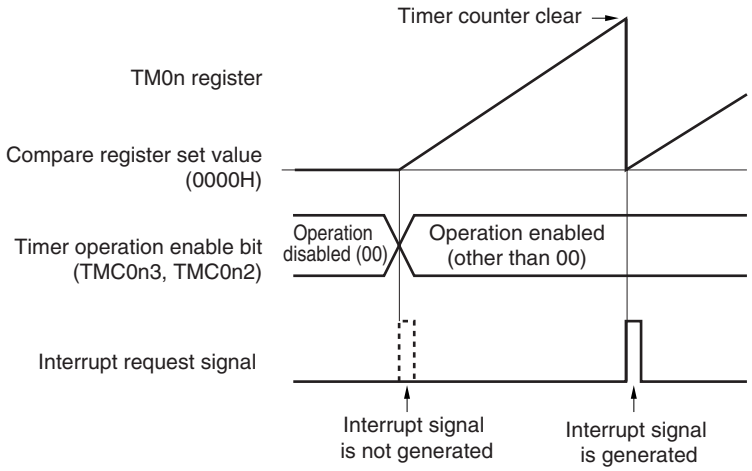
(iii) Setting range when CR00n or CR01n is used as a compare register

When CR00n or CR01n is used as a compare register, set it as shown below.

Operation	CR00n Register Setting Range	CR01n Register Setting Range
Operation as interval timer	0000H < N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH Normally, this setting is not used. Mask the match interrupt signal (INTTM01n).
Operation as square-wave output		
Operation as external event counter		
Operation in the clear & start mode entered by TI00n pin valid edge input	0000H[Note] ≤ N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH
Operation as free-running timer		
Operation as PPG output	M < N ≤ FFFFH	0000H[Note] ≤ M < N
Operation as one-shot pulse output	0000H[Note] ≤ N ≤ FFFFH (N ≠ M)	0000H[Note] ≤ M ≤ FFFFH (M ≠ N)

Note When 0000H is set, a match interrupt immediately after the timer operation does not occur and timer output is not changed, and the first match timing is as follows. A match interrupt occurs at the timing when the timer counter (TM0n register) is changed from 0000H to 0001H.

- When the timer counter is cleared due to overflow
- When the timer counter is cleared due to TI00n pin valid edge (when clear & start mode is entered by TI00n pin valid edge input)
- When the timer counter is cleared due to compare match (when clear & start mode is entered by match between TM0n and CR00n (CR00n = other than 0000H, CR01n = 0000H))



Remarks 1. N: CR00n register set value, M: CR01n register set value

2. For details of TMC0n3 and TMC0n2, see **7.3 (1) 16-bit timer mode control register 0n (TMC0n)**.

3. n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(5) Port mode register 0 (PM0)

This register sets port 0 input/output in 1-bit units.

When using the P01/TO00/TI010 and P06/TO01/TI011 pins for timer output, set PM01 and PM06 and the output latches of P01 and P06 to 0.

When using the P00/TI000, P01/TO00/TI010, P05/TI001/$\overline{\text{SSI11}}$, and P06/TO01/TI011 pins for timer input, set PM00, PM01, PM05, and PM06 to 1. At this time, the output latches of P00, P01, P05, and P06 may be 0 or 1.

PM0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM0 to FFH.

Figure 7-15. Format of Port Mode Register 0 (PM0)

Address: FF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

PM0n	P0n pin I/O mode selection (n = 0 to 6)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 0 of 78K0/KF2 products. For the format of port mode register 0 of other products, see **(1) Port mode registers (PMxx)** in **5.3 Registers Controlling Port Function**.

CHAPTER 8 8-BIT TIMER/EVENT COUNTERS 50 AND 51

8.1 Functions of 8-Bit Timer/Event Counters 50 and 51

8-bit timer/event counters 50 and 51 are mounted onto all 78K0/Kx2 microcontroller products.
8-bit timer/event counters 50 and 51 have the following functions.

- Interval timer
- External event counter
- Square-wave output
- PWM output

8.2 Configuration of 8-Bit Timer/Event Counters 50 and 51

8-bit timer/event counters 50 and 51 include the following hardware.

Table 8-1. Configuration of 8-Bit Timer/Event Counters 50 and 51

Item	Configuration
Timer register	8-bit timer counter 5n (TM5n)
Register	8-bit timer compare register 5n (CR5n)
Timer input	TI5n
Timer output	TO5n
Control registers	Timer clock selection register 5n (TCL5n) 8-bit timer mode control register 5n (TMC5n) Port mode register 1 (PM1) or port mode register 3 (PM3) Port register 1 (P1) or port register 3 (P3)

Figures 8-1 and 8-2 show the block diagrams of 8-bit timer/event counters 50 and 51.

Figure 9-5. Format of 8-Bit Timer H Mode Register 0 (TMHMD0)

Address: FF69H After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD0	TMHE0	CKS02	CKS01	CKS00	TMMD01	TMMD00	TOLEV0	TOEN0

TMHE0	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS02	CKS01	CKS00	Count clock selection[Note 1]				
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz	20 MHz[Note 3]
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
1	0	0	$f_{PRS}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.54 kHz
1	0	1	TM50 output[Note 4]				
Other than above			Setting prohibited				

TMMD01	TMMD00	Timer operation mode
0	0	Interval timer mode
1	0	PWM output mode
Other than above		Setting prohibited

TOLEV0	Timer output level control (in default mode)
0	Low level
1	High level

TOEN0	Timer output control
0	Disables output
1	Enables output

Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

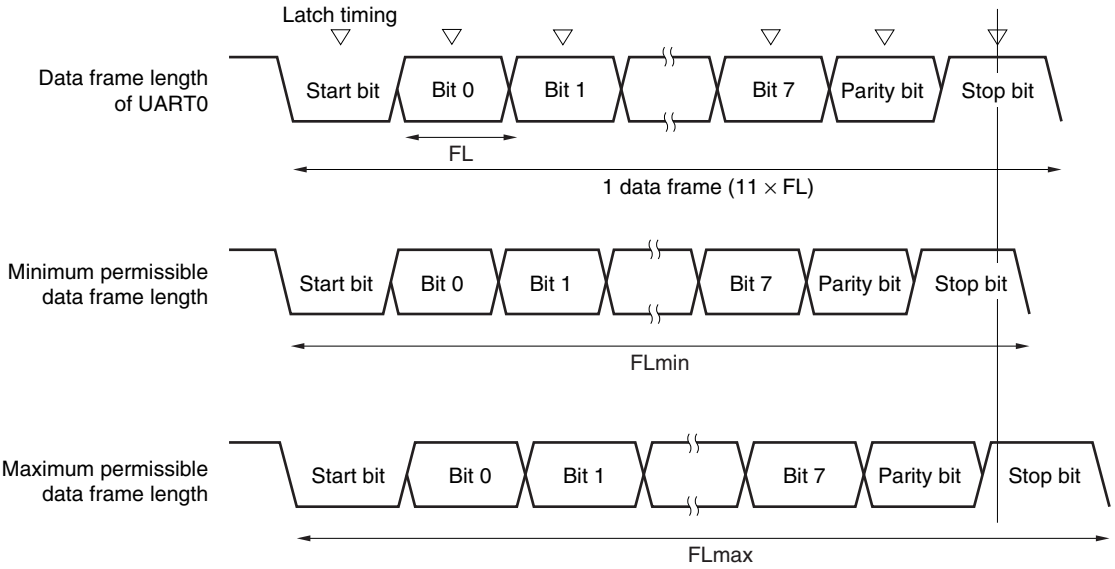
(The values shown in the table above are those when $f_{PRS} = f_{XH}$ (XSEL = 1).)

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 14-12. Permissible Baud Rate Range During Reception



As shown in Figure 14-12, the latch timing of the receive data is determined by the counter set by baud rate generator control register 0 (BRGC0) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.

Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART0
k: Set value of BRGC0
FL: 1-bit data length
Margin of latch timing: 2 clocks

(3) Automatic transmission/reception communication operation

(a) Automatic transmission/reception mode

Automatic transmission/reception can be performed using buffer RAM.

The data stored in the buffer RAM is output from the SOA0 pin via the SIOA0 register in synchronization with the $\overline{\text{SCKA0}}$ falling edge by performing **(2) Automatic transmit/receive data setting**.

The receive data is stored in the buffer RAM via the SIOA0 register in synchronization with the $\overline{\text{SCKA0}}$ rising edge.

Data transfer ends if bit 0 (TSF0) of serial status register 0 (CSIS0) is set to 1 when any of the following conditions is met.

- Communication stop: Reset by clearing bit 7 (CSIAE0) of the CSIMA0 register to 0
- Communication suspension: Transfer of 1 byte is complete by setting bit 1 (ATSTP0) of the CSIT0 register to 1
- Bit shift error: Transfer of 1 byte is complete when bit 1 (ERRF0) of the CSIS0 register becomes 1 while bit 2 (ERRE0) = 1
- Transfer of the range specified by the ADTP0 register is complete

At this time, an interrupt request signal (INTACSI) is generated except when the CSIAE0 bit = 0.

If a transfer is terminated in the middle, transfer starting from the remaining data is not possible. Read automatic data transfer address count register 0 (ADTC0) to confirm how much of the data has already been transferred and re-execute transfer by performing **(2) Automatic transmit/receive data setting**.

In addition, when busy control and strobe control are not performed, the BUSY0/BUZ/INTP7/P141 and STB0/P145 pins can be used as ordinary I/O port pins.

Figure 17-13 shows the example of the operation timing in automatic transmission/reception mode and Figure 17-14 shows the operation flowchart. Figures 17-15 and 17-16 show the operation of internal buffer RAM when 6 bytes of data are transmitted/received.

Figure 20-9. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KD2)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	SREMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK010	TMMK000	TMMK50	TMMKH0	TMMKH1	DUALMK0 CSIMK10 STMK0	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	1	PMK6	WTMK	KRMK	TMMK51	WTIMK	SRMK0	ADMK

Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	<0>
MK1H	1	1	1	1	1	1	1	IICMK0 DMUMK[Note]

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note Products whose flash memory is at least 48 KB only.

Caution Be sure to set bit 7 of MK1L and bits 1 to 7 of MK1H to 1.

(3) Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)

The priority specification flag registers are used to set the corresponding maskable interrupt priority order.

PR0L, PR0H, PR1L, and PR1H are set by a 1-bit or 8-bit memory manipulation instruction. If PR0L and PR0H, and PR1L and PR1H are combined to form 16-bit registers PR0 and PR1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 20-12. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KB2)

Address: FFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	DUALPR0 CSIPR10 STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	7	6	5	4	<3>	2	<1>	<0>
PR1L	1	1	1	1	TMPR51	1	SRPR0	ADPR

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	<0>
PR1H	1	1	1	1	1	1	1	IICPR0

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Caution Be sure to set bits 2, 4 to 7 of PR1L and bits 1 to 7 of PR1H to 1.

21.3 Register Controlling Key Interrupt

(1) Key return mode register (KRM)

This register controls the KRMn bit using the KRn signal.

KRM is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears KRM to 00H.

Figure 21-2. Format of Key Return Mode Register (KRM)

(1) 38-pin products of 78K0/KC2

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	0	0	KRM1	KRM0

(2) 44-pin and 48-pin products of 78K0/KC2

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	KRM3	KRM2	KRM1	KRM0

(3) 78K0/KD2, 78K0/KE2, 78K0/KF2

Address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

Cautions 1. If any of the KRMn bits used is set to 1, set bit n (PU7n) of the corresponding pull-up resistor register 7 (PU7) to 1.

2. If KRM is changed, the interrupt request flag may be set. Therefore, disable interrupts and then change the KRM register. Clear the interrupt request flag and enable interrupts.

3. The bits not used in the key interrupt mode can be used as normal ports.

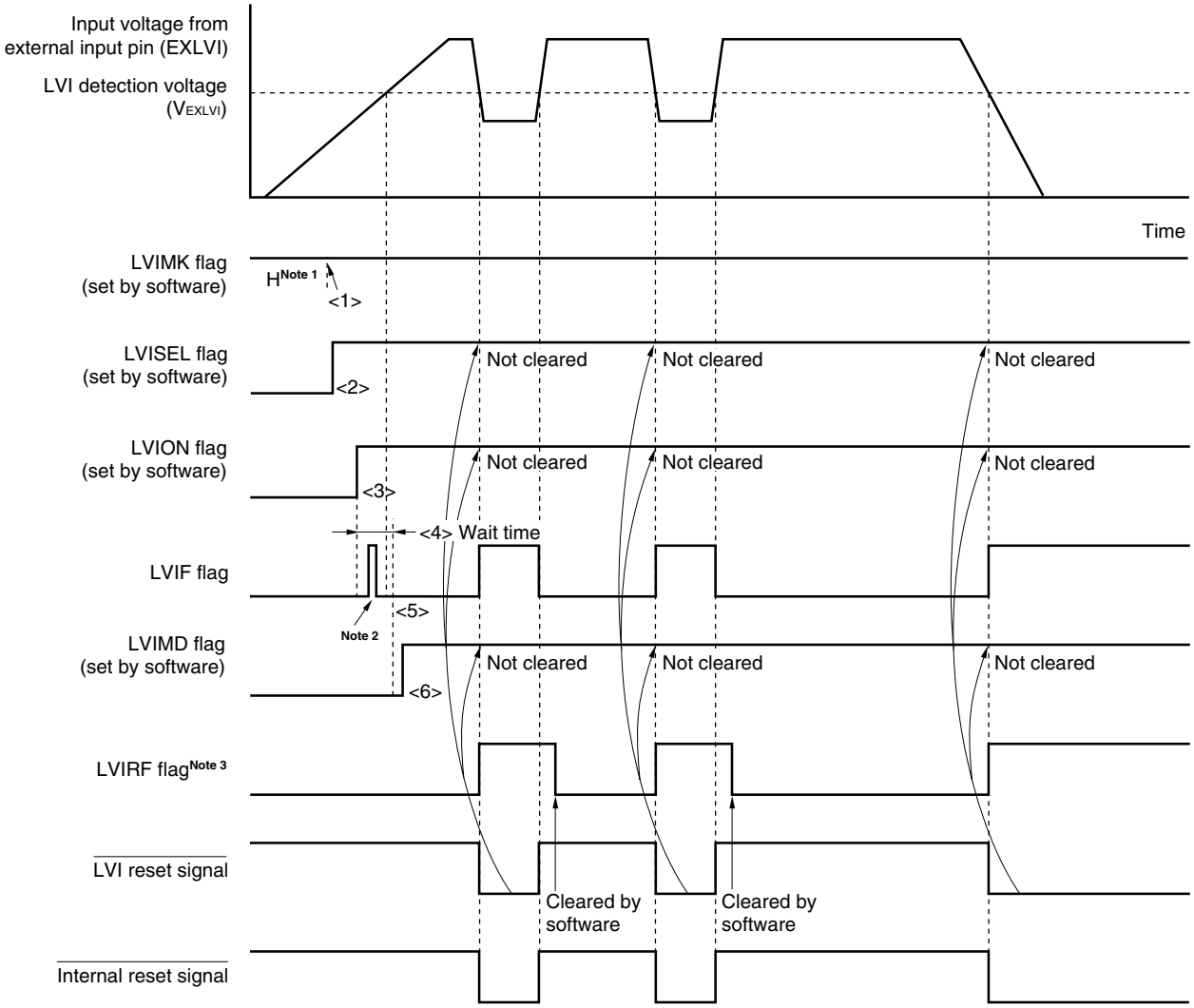
4. For the 38-pin products of 78K0/KC2, be sure to set bits 2 to 7 of KRM to "0". For the 44-pin and 48-pin products of 78K0/KC2, be sure to set bits 4 to 7 of KRM to "0".

Remark n = 0, 1: 38-pin products of 78K0/KC2

n = 0 to 3: 44-pin and 48-pin products of 78K0/KC2

n = 0 to 7: 78K0/KD2, 78K0/KE2, 78K0/KF2

Figure 25-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Detects Level of Input Voltage from External Input Pin (EXLVI))



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

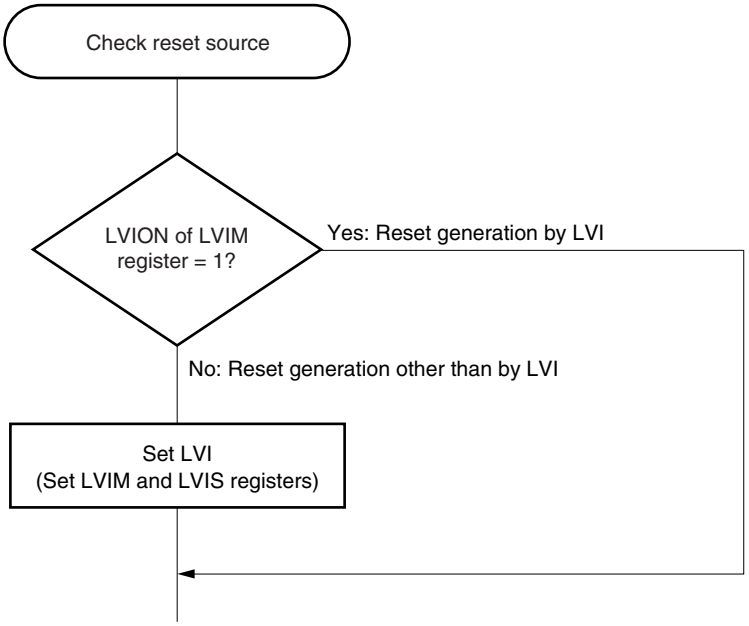
2. The LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 23 RESET FUNCTION**.

Remark <1> to <6> in Figure 25-6 above correspond to <1> to <6> in the description of "When starting operation" in **25.4.1 (2) When detecting level of input voltage from external input pin (EXLVI)**.

Figure 25-9. Example of Software Processing After Reset Release (2/2)

• Checking reset source



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	EV_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3[Note]	V
	AV_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}		−0.5 to +3.6 and −0.5 to V_{DD}	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P20 to P27, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120 to P124, P140 to P145, X1, X2, XT1, XT2, $\overline{\text{RESET}}$, FLMD0	−0.3 to V_{DD} + 0.3[Note]	V
	V_{I2}	P60 to P63 (N-ch open drain)	−0.3 to +6.5	V
Output voltage	V_O		−0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{AN}	ANI0 to ANI7	−0.3 to AV_{REF} + 0.3[Note] and −0.3 to V_{DD} + 0.3[Note]	V

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

DC Characteristics (4/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		3.2	5.5	mA
				Resonator connection		4.5	6.9	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		1.6	2.8	mA
				Resonator connection		2.3	3.9	mA
			f_{XH} = 10 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		1.5	2.7	mA
				Resonator connection		2.2	3.2	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.9	1.6	mA
				Resonator connection		1.3	2.0	mA
			f_{XH} = 5 MHz, V_{DD} = 2.0 V [Notes 2, 3]	Square wave input		0.7	1.4	mA
				Resonator connection		1.0	1.6	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			1.4	2.5	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		6	25	μA
				Resonator connection		15	30	μA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		0.8	2.6	mA
				Resonator connection		2.0	4.4	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		0.4	1.3	mA
				Resonator connection		1.0	2.4	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.2	0.65	mA
				Resonator connection		0.5	1.1	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			0.4	1.2	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		3.0	22	μA
				Resonator connection		12	25	μA
	I_{DD3}[Note 6]	STOP mode				1	20	μA
			T_A = −40 to +70 °C			1	10	μA
A/D converter operating current	I_{ADC}[Note 7]	2.3 V ≤ AV_{REF} ≤ V_{DD}, ADCS = 1				0.86	1.9	mA
Watchdog timer operating current	I_{WDT}[Note 8]	During 240 kHz internal low-speed oscillation clock operation				5	10	μA
LVI operating current	I_{LVI}[Note 9]					9	18	μA

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

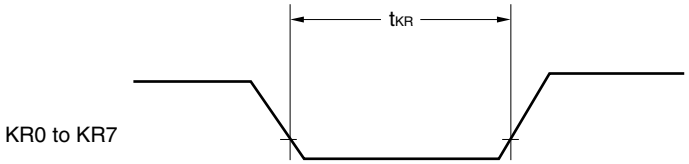
2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or external subsystem clock frequency)

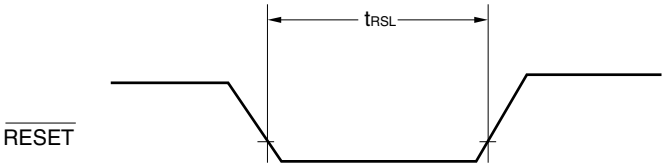
(Notes on next page)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



CHAPTER 32 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: T_A = –40 to +110°C)

Target Products	Conventional-specification Products	Expanded-specification Products
78K0/KB2	μPD78F0500(A2), 78F0501(A2), 78F0502(A2), 78F0503(A2)	μPD78F0500A(A2), 78F0501A(A2), 78F0502A(A2), 78F0503A(A2)
78K0/KC2	μPD78F0511(A2), 78F0512(A2), 78F0513(A2), 78F0514(A2), 78F0515(A2)	μPD78F0511A(A2), 78F0512A(A2), 78F0513A(A2), 78F0514A(A2), 78F0515A(A2)
78K0/KD2	μPD78F0521(A2), 78F0522(A2), 78F0523(A2), 78F0524(A2), 78F0525(A2), 78F0526(A2), 78F0527(A2)	μPD78F0521A(A2), 78F0522A(A2), 78F0523A(A2), 78F0524A(A2), 78F0525A(A2), 78F0526A(A2), 78F0527A(A2)
78K0/KE2	μPD78F0531(A2), 78F0532(A2), 78F0533(A2), 78F0534(A2), 78F0535(A2), 78F0536(A2), 78F0537(A2)	μPD78F0531A(A2), 78F0532A(A2), 78F0533A(A2), 78F0534A(A2), 78F0535A(A2), 78F0536A(A2), 78F0537A(A2)
78K0/KF2	μPD78F0544(A2), 78F0545(A2), 78F0546(A2), 78F0547(A2)	μPD78F0544A(A2), 78F0545A(A2), 78F0546A(A2), 78F0547A(A2)

The following items are described separately for conventional-specification products (μPD78F05xx(A2)) and expanded-specification products (μPD78F05xxA(A2)).

- X1 clock oscillation frequency (**X1 oscillator characteristics**)
- Instruction cycle, peripheral hardware clock frequency, external main system clock frequency, external main system clock input high-level width, and external main system clock input low-level width (**(1) Basic operation** in **AC characteristics**)
- A/D conversion time (**A/D Converter Characteristics**)
- Number of rewrites per chip (**Flash Memory Programming Characteristics**)

Caution The pins mounted depend on the product as follows.

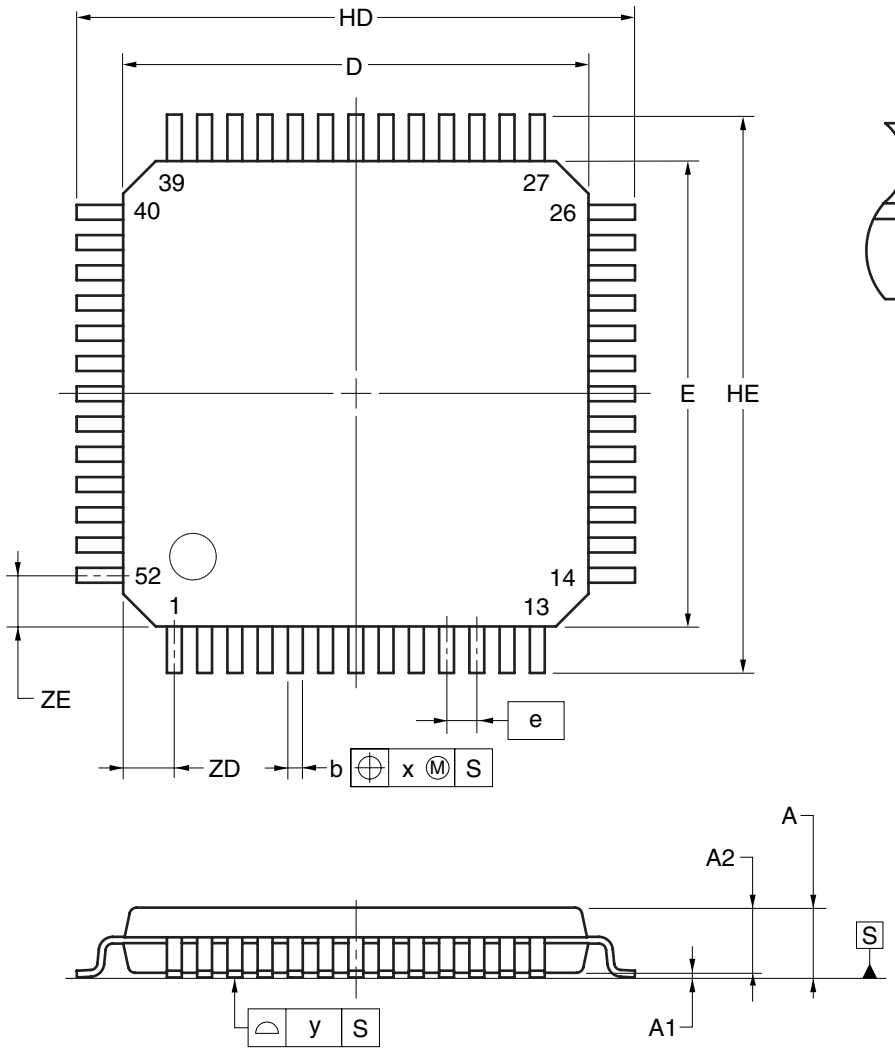
(1) Port functions

Port	78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
	30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Port 0	P00, P01				P00 to P03	P00 to P06	
Port 1	P10 to P17						
Port 2	P20 to P23	P20 to P25	P20 to P27				
Port 3	P30 to P33						
Port 4	–		P40, P41			P40 to P43	P40 to P47
Port 5	–					P50 to P53	P50 to P57
Port 6	P60, P61	P60 to P63					P60 to P67
Port 7	–	P70, P71	P70 to P73	P70 to P75	P70 to P77		
Port 12	P120 to P122	P120 to P124					
Port 13	–			P130			
Port 14	–			P140		P140, P141	P140 to P145

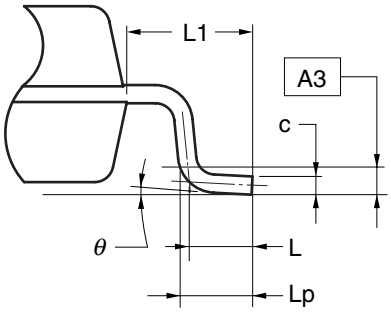
(The remaining table is on the next page.)

- μPD78F0521GB(A)-GAG-AX, 78F0522GB(A)-GAG-AX, 78F0523GB(A)-GAG-AX, 78F0524GB(A)-GAG-AX, 78F0525GB(A)-GAG-AX, 78F0526GB(A)-GAG-AX, 78F0527GB(A)-GAG-AX
- μPD78F0521GB(A2)-GAG-AX, 78F0522GB(A2)-GAG-AX, 78F0523GB(A2)-GAG-AX, 78F0524GB(A2)-GAG-AX, 78F0525GB(A2)-GAG-AX, 78F0526GB(A2)-GAG-AX, 78F0527GB(A2)-GAG-AX
- μPD78F0521AGB-GAG-AX, 78F0522AGB-GAG-AX, 78F0523AGB-GAG-AX, 78F0524AGB-GAG-AX, 78F0525AGB-GAG-AX, 78F0526AGB-GAG-AX, 78F0527AGB-GAG-AX, 78F0527DAGB-GAG-AX
- μPD78F0521AGBA-GAG-G, 78F0522AGBA-GAG-G, 78F0523AGBA-GAG-G, 78F0524AGBA-GAG-G, 78F0525AGBA-GAG-G, 78F0526AGBA-GAG-G, 78F0527AGBA-GAG-G
- μPD78F0521AGBA2-GAG-G, 78F0522AGBA2-GAG-G, 78F0523AGBA2-GAG-G, 78F0524AGBA2-GAG-G, 78F0525AGBA2-GAG-G, 78F0526AGBA2-GAG-G, 78F0527AGBA2-GAG-G

52-PIN PLASTIC LQFP (10x10)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.10
ZE	1.10

P52GB-65-GAG

NOTE
Each lead centerline is located within 0.13mm of its true position at maximum material condition.