Renesas Electronics America Inc - UPD78F0535AGK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0535agk-gaj-ax

2.2.4 P30 to P33 (port 3)

P30 to P33 function as an I/O port. These pins also function as pins for external interrupt request input and timer I/O.

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P30/INTP1	√					
P31/INTP2/ OCD1A[Note]	√					
P32/INTP3/ OCD1B[Note]	√					
P33/INTP4/TI51/ TO51	√					

Note OCD1A and OCD1B are provided to the products with an on-chip debug function (μPD78F05xxD and 78F05xxDA) only.

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as an I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as external interrupt request input and timer I/O.

(a) INTP1 to INTP4

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI51

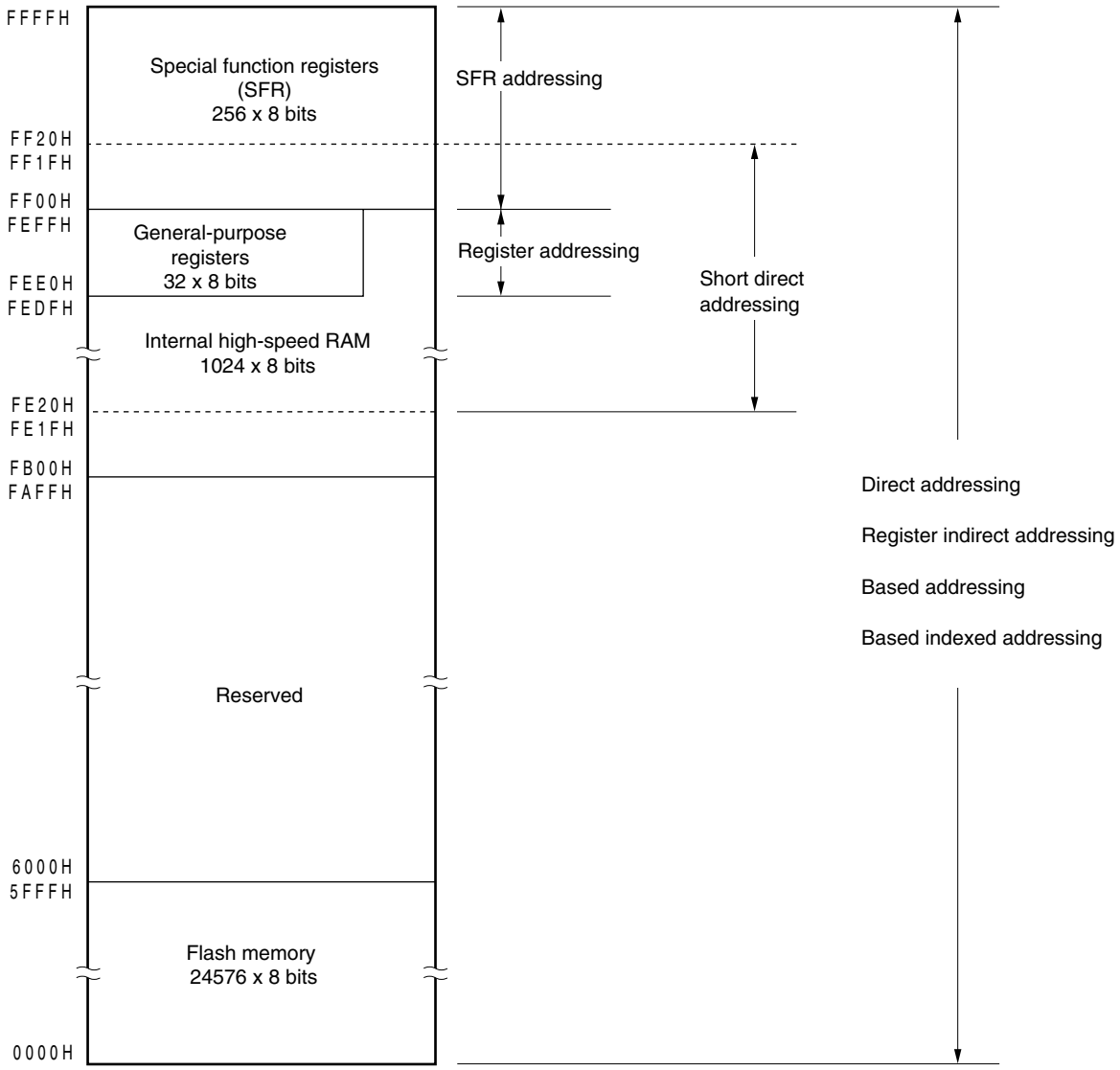
This is an external count clock input pin to 8-bit timer/event counter 51.

(c) TO51

This is a timer output pin from 8-bit timer/event counter 51.

Caution 1. In the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA), be sure to pull the P31/INTP2/OCD1A pin down before a reset release, to prevent malfunction.

Figure 3-14. Correspondence Between Data Memory and Addressing
(μPD78F0502, 78F0502A, 78F0512, 78F0512A, 78F0522, 78F0522A, 78F0532, and 78F0532A)



Caution 1. When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 6-12 and 6-13 to avoid an adverse effect from wiring capacitance.

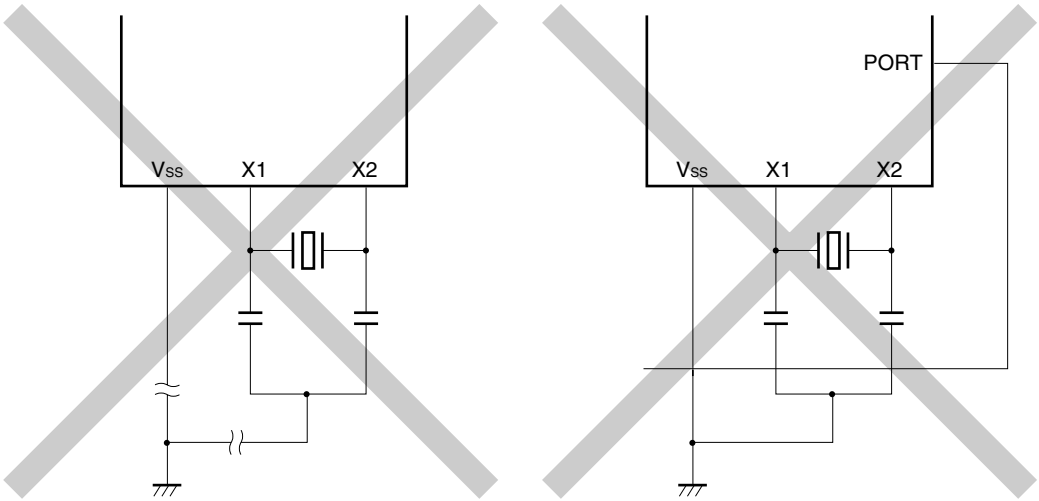
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Note that the XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption.

Figure 6-14 shows examples of incorrect resonator connection.

Figure 6-14. Examples of Incorrect Resonator Connection (1/2)

(a) Too long wiring **(b) Crossed signal line**



Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

<4> Waiting for the stabilization of the oscillation of X1 clock
Check the OSTC register and wait for the necessary time.
During the wait time, other software processing can be executed with the internal high-speed oscillation clock.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the X1 clock is operating.
2. Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: T_A = –40 to +125°C)).

(2) Example of setting procedure when using the external main system clock

<1> Setting frequency (OSCCTL register)
Using AMPH, set the frequency to be used.

AMPH[Note]	Operating Frequency Control
0	1 MHz ≤ f_{XH} ≤ 10 MHz
1	10 MHz < f_{XH} ≤ 20 MHz

Note Set AMPH before setting the peripheral functions after a reset release. The value of AMPH can be changed only once after a reset release. The clock supply to the CPU is stopped for the duration of 160 external clocks after AMPH is set to 1.

Remark f_{XH}: High-speed system clock oscillation frequency

<2> Setting P121/X1 and P122/X2/EXCLK pins and selecting operation mode (OSCCTL register)
When EXCLK and OSCSEL are set to 1, the mode is switched from port mode to external clock input mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
1	1	External clock input mode	I/O port	External clock input

<3> Controlling external main system clock input (MOC register)
When MSTOP is cleared to 0, the input of the external main system clock is enabled.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the external main system clock is operating.
2. Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) to CHAPTER 33 ELECTRICAL SPECIFICATIONS ((A2) GRADE PRODUCTS: T_A = –40 to +125°C)).

(3) Example of setting procedure when using high-speed system clock as CPU clock and peripheral hardware clock

<1> Setting high-speed system clock oscillation[Note]
(See **6.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when high-speed system clock is already operating.

6.6.9 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 6-11. Conditions Before the Clock Oscillation Is Stopped and Flag Settings (78K0/KB2)

Clock[Note]	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 (The CPU is operating on the high-speed system clock)	RSTOP = 1
X1 clock	MCS = 0 (The CPU is operating on the internal high-speed oscillation clock)	MSTOP = 1
External main system clock		

Note The 78K0/KB2 is not provided with a subsystem clock.

Table 6-12. Conditions Before the Clock Oscillation Is Stopped and Flag Settings (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the internal high-speed oscillation clock)	RSTOP = 1
X1 clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock)	MSTOP = 1
External main system clock		
XT1 clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock)	OSCSELS = 0
External subsystem clock		

Figure 7-18. Example of Register Settings for Interval Timer Operation

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	1	1	0	0

Clears and starts on match between TM0n and CR00n.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0	0	0

CR00n used as compare register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0	0	0	0

(d) Prescaler mode register 0n (PRM0n)

ES1n1	ES1n0	ES0n1	ES0n0	3	2	PRM0n1	PRM0n0
0	0	0	0	0	0	0/1	0/1

Selects count clock

(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

If M is set to CR00n, the interval time is as follows.

- Interval time = (M + 1) × Count clock cycle

Setting CR00n to 0000H is prohibited.

(g) 16-bit capture/compare register 01n (CR01n)

Usually, CR01n is not used for the interval timer function. However, a compare match interrupt (INTTM01n) is generated when the set value of CR01n matches the value of TM0n.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK01n).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 14-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (2/2)

PS01	PS00	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL0	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL0	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE0) of asynchronous serial interface reception error status register 0 (ASIS0) is not set and the error interrupt does not occur.

Cautions 1. To start the transmission, set POWER0 to 1 and then set TXE0 to 1. To stop the transmission, clear TXE0 to 0, and then clear POWER0 to 0.

2. To start the reception, set POWER0 to 1 and then set RXE0 to 1. To stop the reception, clear RXE0 to 0, and then clear POWER0 to 0.

3. Set POWER0 to 1 and then set RXE0 to 1 while a high level is input to the RxD0 pin. If POWER0 is set to 1 and RXE0 is set to 1 while a low level is input, reception is started.

4. TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.

5. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

6. Clear the TXE0 and RXE0 bits to 0 before rewriting the PS01, PS00, and CL0 bits.

7. Make sure that TXE0 = 0 when rewriting the SL0 bit. Reception is always performed with “number of stop bits = 1”, and therefore, is not affected by the set value of the SL0 bit.

8. Be sure to set bit 0 to 1.

15.4 Operation of Serial Interface UART6

Serial interface UART6 has the following two modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode

15.4.1 Operation stop mode

In this mode, serial communication cannot be executed; therefore, the power consumption can be reduced. In addition, the pins can be used as ordinary port pins in this mode. To set the operation stop mode, clear bits 7, 6, and 5 (POWER6, TXE6, and RXE6) of ASIM6 to 0.

(1) Register used

The operation stop mode is set by asynchronous serial interface operation mode register 6 (ASIM6).

ASIM6 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM6	POWER6	TXE6	RXE6	PS61	PS60	CL6	SL6	ISRM6

POWER6	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].

TXE6	Enables/disables transmission
0	Disables transmission operation (synchronously resets the transmission circuit).

RXE6	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).

Notes 1. If POWER6 = 0 is set while transmitting data, the output of the TxD6 pin will be fixed to high level (if TXDLV6 = 0). Furthermore, the input from the RxD6 pin will be fixed to high level.

2. Asynchronous serial interface reception error status register 6 (ASIS6), asynchronous serial interface transmission status register 6 (ASIF6), bit 7 (SBRF6) and bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6), and receive buffer register 6 (RXB6) are reset.

Caution Clear POWER6 to 0 after clearing TXE6 and RXE6 to 0 to stop the operation.
To start the communication, set POWER6 to 1, and then set TXE6 or RXE6 to 1.

Remark To use the RxD6/P14 and TxD6/P13 pins as general-purpose port pins, see **CHAPTER 5 PORT FUNCTIONS**.

(c) Normal transmission

When bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and bit 6 (TXE6) of ASIM6 is then set to 1, transmission is enabled. Transmission can be started by writing transmit data to transmit buffer register 6 (TXB6). The start bit, parity bit, and stop bit are automatically appended to the data.

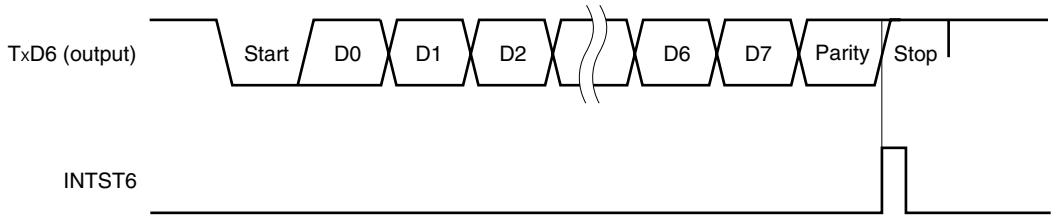
When transmission is started, the data in TXB6 is transferred to transmit shift register 6 (TXS6). After that, the transmit data is sequentially output from TXS6 to the TxD6 pin. When transmission is completed, the parity and stop bits set by ASIM6 are appended and a transmission completion interrupt request (INTST6) is generated.

Transmission is stopped until the data to be transmitted next is written to TXB6.

Figure 15-15 shows the timing of the transmission completion interrupt request (INTST6). This interrupt occurs as soon as the last stop bit has been output.

Figure 15-15. Normal Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2

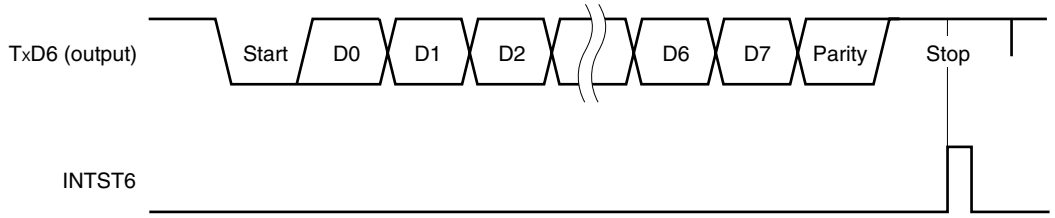


Figure 18-5. Format of IIC Control Register 0 (IICC0) (2/4)

SPIE0[Note 1]	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable

Condition for clearing (SPIE0 = 0)	Condition for setting (SPIE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

WTIM0[Note 1]	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and wait is set. Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.
An interrupt is generated at the falling edge of the ninth clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an acknowledge ($\overline{ACK}$) is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.	

Condition for clearing (WTIM0 = 0)	Condition for setting (WTIM0 = 1)
• Cleared by instruction • Reset	• Set by instruction

ACKE0[Notes 1, 2]	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDA0 line is set to low level.

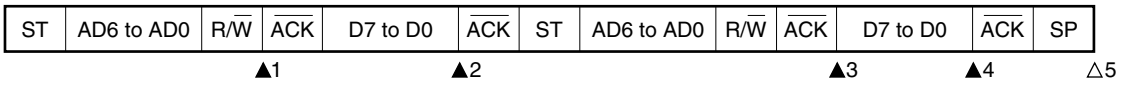
Condition for clearing (ACKE0 = 0)	Condition for setting (ACKE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

Notes 1. This flag's signal is invalid when IICE0 = 0.

2. The set value is invalid during address transfer and if the code is not an extension code.
When the device serves as a slave and the addresses match, an acknowledge is generated regardless of the set value.

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

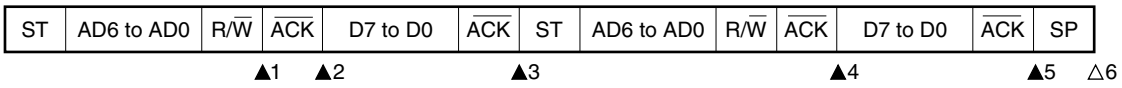
(i) When WTIM0 = 0 (after restart, matches SVA0)



▲1: IICS0 = 0010×010B
▲2: IICS0 = 0010×000B
▲3: IICS0 = 0001×110B
▲4: IICS0 = 0001×000B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, matches SVA0)



▲1: IICS0 = 0010×010B
▲2: IICS0 = 0010×110B
▲3: IICS0 = 0010××00B
▲4: IICS0 = 0001×110B
▲5: IICS0 = 0001××00B
△6: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 20-15. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KE2)

Address: FFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	DUALPR0 CSIPR10 STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR1L	PPR7	PPR6	WTPR	KRPR	TMPR51	WTIPR	SRPR0	ADPR

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR1H	1	1	1	1	TMPR011 Note	TMPR001 Note	CSIPR11 Note	IICPR0 DMUPR Note

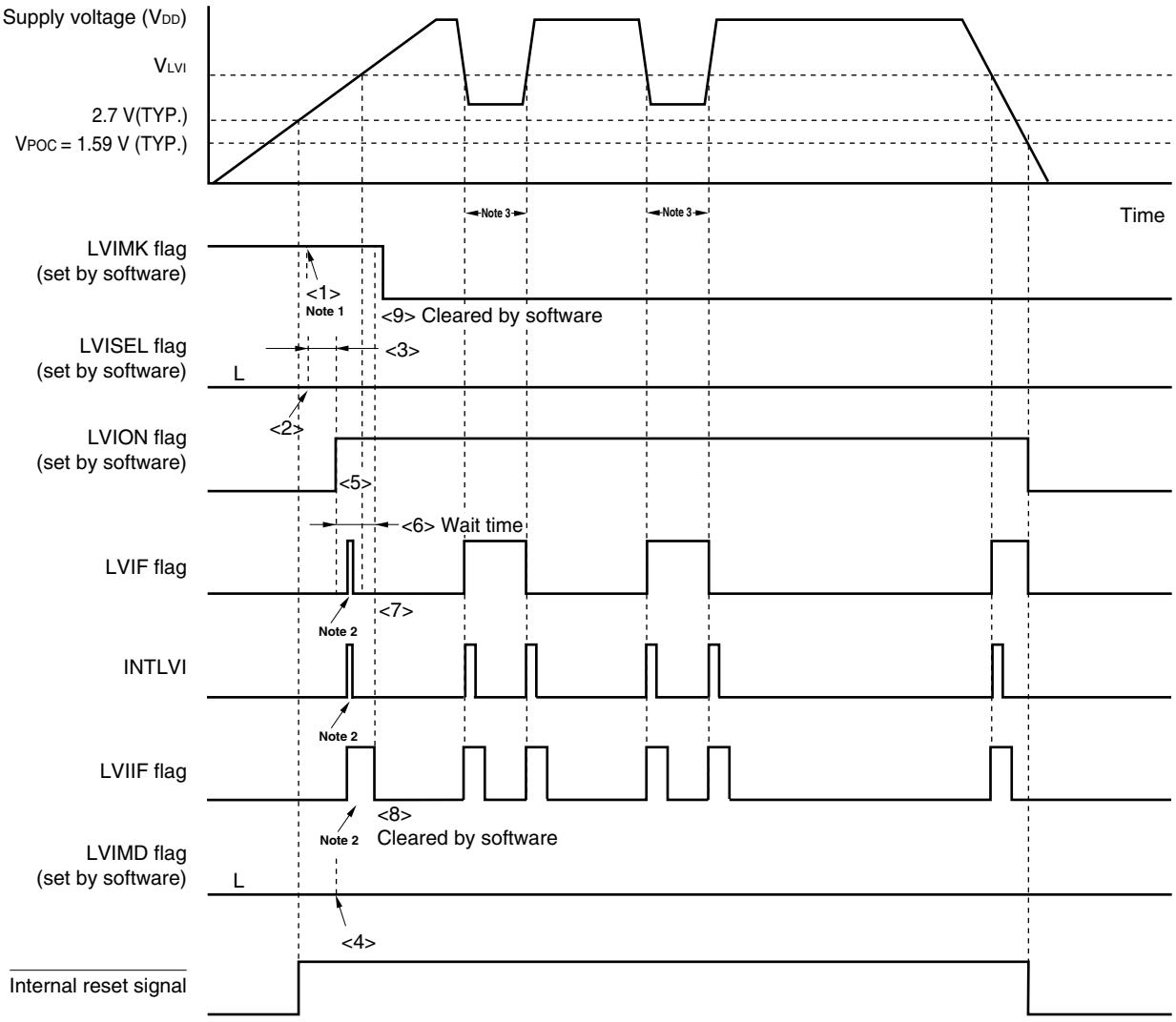
XXPRX	Priority level selection
0	High priority level
1	Low priority level

Note Products whose flash memory is at least 48 KB only.

Caution Be sure to set bits 1 to 7 of PR1H to 1 for the products whose flash memory is less than 32 KB. Be sure to set bits 4 to 7 of PR1H to 1 for the products whose flash memory is at least 48 KB.

Figure 25-7. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage (V_{DD})) (2/2)

(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

Remark <1> to <9> in Figure 25-7 above correspond to <1> to <9> in the description of "When starting operation" in **25.4.2 (1) When detecting level of supply voltage (V_{DD})**.

CHAPTER 26 OPTION BYTE

26.1 Functions of Option Bytes

The flash memory at 0080H to 0084H of the 78K0/Kx2 microcontrollers is an option byte area. When power is turned on or when the device is restarted from the reset status, the device automatically references the option bytes and sets specified functions. When using the product, be sure to set the following functions by using the option bytes.

When the boot swap operation is used during self-programming, 0080H to 0084H are switched to 1080H to 1084H. Therefore, set values that are the same as those of 0080H to 0084H to 1080H to 1084H in advance.

Caution Be sure to set 00H to 0082H and 0083H (0082H/1082H and 0083H/1083H when the boot swap function is used).

(1) 0080H/1080H

- Internal low-speed oscillator operation
  - Can be stopped by software
  - Cannot be stopped
- Watchdog timer overflow time setting
- Watchdog timer counter operation
  - Enabled counter operation
  - Disabled counter operation
- Watchdog timer window open period setting

Caution Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

(2) 0081H/1081H

- Selecting POC mode
  - During 2.7 V/1.59 V POC mode operation (POCMODE = 1)
    The device is in the reset state upon power application and until the supply voltage reaches 2.7 V (TYP.). It is released from the reset state when the voltage exceeds 2.7 V (TYP.). After that, POC is not detected at 2.7 V but is detected at 1.59 V (TYP.).
    With standard and (A) grade products, if the supply voltage rises to 1.8 V after power application at a rate slower than 0.5 V/ms (MIN.), use of the 2.7 V/1.59 V POC mode is recommended.
  - During 1.59 V POC mode operation (POCMODE = 0)
    The device is in the reset state upon power application and until the supply voltage reaches 1.59 V (TYP.). It is released from the reset state when the voltage exceeds 1.59 V (TYP.). After that, POC is detected at 1.59 V (TYP.), in the same manner as on power application.

Caution POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

Figure 26-1. Format of Option Byte (2/2)

Address: 0081H/1081H[Notes 1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	POCMODE

POCMODE	POC mode selection
0	1.59 V POC mode (default)
1	2.7 V/1.59 V POC mode

Notes 1. POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

2. To change the setting for the POC mode, set the value to 0081H again after batch erasure (chip erasure) of the flash memory. The setting cannot be changed after the memory of the specified block is erased.

Caution Be sure to clear bits 7 to 1 to "0".

Address: 0082H/1082H, 0083H/1083H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Note Be sure to set 00H to 0082H and 0083H, as these addresses are reserved areas. Also set 00H to 1082H and 1083H because 0082H and 0083H are switched with 1082H and 1083H when the boot swap operation is used.

Address: 0084H/1084H[Notes1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	OCDEN1	OCDEN0

OCDEN1	OCDEN0	On-chip debug operation control
0	0	Operation disabled
0	1	Setting prohibited
1	0	Operation enabled. Does not erase data of the flash memory in case authentication of the on-chip debug security ID fails.
1	1	Operation enabled. Erases data of the flash memory in case authentication of the on-chip debug security ID fails.

Notes 1. Be sure to set 00H (on-chip debug operation disabled) to 0084H for products not equipped with the on-chip debug function (μPD78F05xx and 78F05xxA). Also set 00H to 1084H because 0084H and 1084H are switched during the boot swap operation.

2. To use the on-chip debug function with a product equipped with the on-chip debug function (μPD78F05xxD and 78F05xxDA), set 02H or 03H to 0084H. Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot swap operation.

Remark For the on-chip debug security ID, see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD and 78F05xxDA ONLY)**.

Table 27-1. Internal Memory Size Switching Register Settings

78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2	IMS Setting
μPD78F0500, 78F0500A	–	–	–	–	42H
μPD78F0501, 78F0501A	μPD78F0511, 78F0511A	μPD78F0521, 78F0521A	μPD78F0531, 78F0531A	–	04H
μPD78F0502, 78F0502A	μPD78F0512, 78F0512A	μPD78F0522, 78F0522A	μPD78F0532, 78F0532A	–	C6H
μPD78F0503, 78F0503A, 78F0503D Note 1, 78F0503DA Note 1	μPD78F0513, 78F0513A, 78F0513D Note 1, 78F0513DA Note 1	μPD78F0523, 78F0523A	μPD78F0533, 78F0533A	–	C8H
–	μPD78F0514, 78F0514A	μPD78F0524, 78F0524A	μPD78F0534, 78F0534A	μPD78F0544, 78F0544A	CCH
–	μPD78F0515, 78F0515A, 78F0515D Note 1, 78F0515DA Note 1	μPD78F0525, 78F0525A	μPD78F0535, 78F0535A	μPD78F0545, 78F0545A	CFH
–	–	μPD78F0526, 78F0526A	μPD78F0536, 78F0536A	μPD78F0546, 78F0546A	CCH Note 2
–	–	μPD78F0527, 78F0527A, 78F0527D Note 1, 78F0527DA Note 1	μPD78F0537, 78F0537A, 78F0537D Note 1, 78F0537DA Note 1	μPD78F0547, 78F0547A, 78F0547D Note 1, 78F0547DA Note 1	CCH Note 2

Notes 1. The internal ROM capacity and internal high-speed RAM capacity of the products with the on-chip debug function can be debugged according to the debug target products. Set IMS according to the debug target products.

2. The μPD78F05x6 and 78F05x6A (x = 2 to 4) have internal ROMs of 96 KB, and the μPD78F05x7, 78F05x7A, 78F05x7D, and 78F05x7DA (x = 2 to 4) have those of 128 KB. However, the set value of IMS of these devices is the same as those of the 48 KB product because memory banks are used. For how to set the memory banks, see **4.3 Memory Bank Select Register (BANK)**.

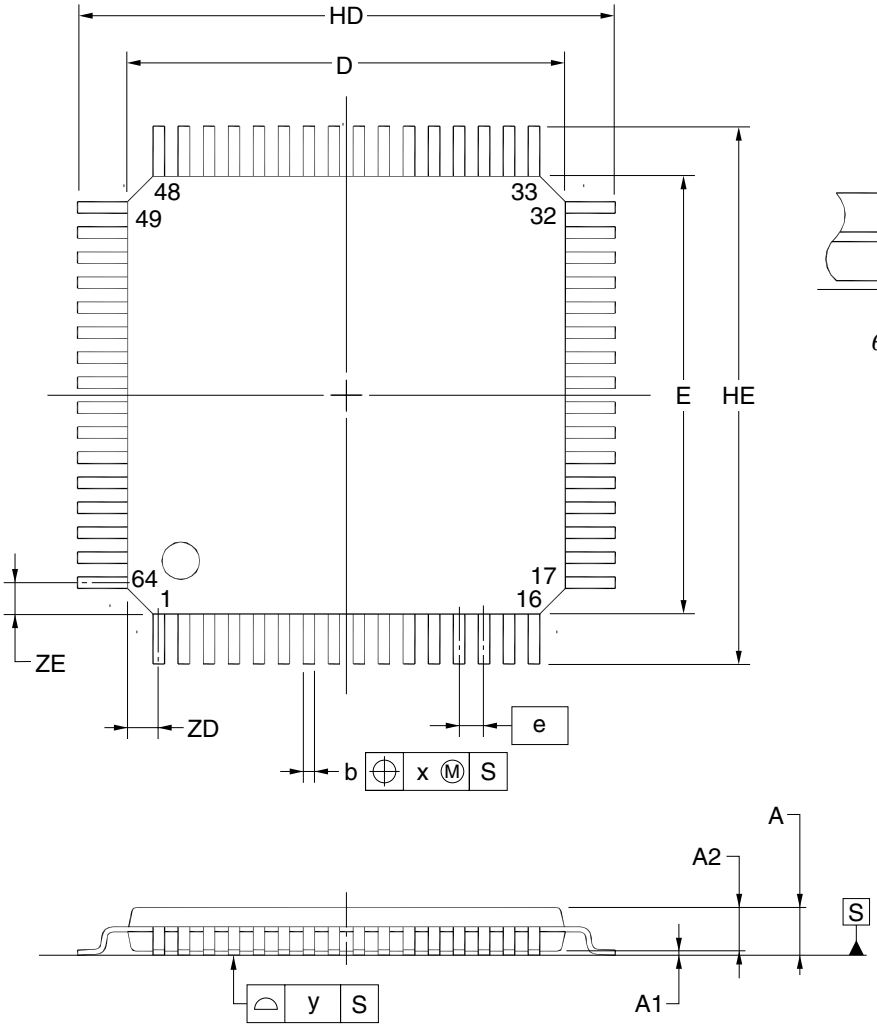
27.2 Internal Expansion RAM Size Switching Register

Select the internal expansion RAM capacity using the internal expansion RAM size switching register (IXS).
IXS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IXS to 0CH.

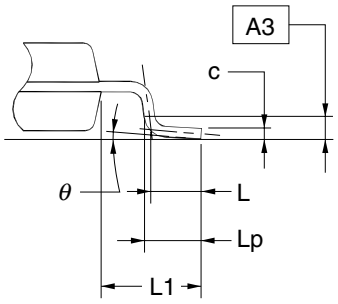
Caution Be sure to set each product to the values shown in Table 27-2 after a reset release.

- μPD78F0531GC-UBS-A, 78F0532GC-UBS-A, 78F0533GC-UBS-A, 78F0534GC-UBS-A, 78F0535GC-UBS-A, 78F0536GC-UBS-A, 78F0537GC-UBS-A, 78F0537DGC-UBS-A

64-PIN PLASTIC LQFP(14x14)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	17.20±0.20
HE	17.20±0.20
A	1.70 MAX.
A1	0.125±0.075
A2	1.40±0.05
A3	0.25
b	$0.37^{+0.08}_{-0.07}$
c	$0.17^{+0.03}_{-0.06}$
L	0.80
Lp	0.886±0.15
L1	1.60±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

P64GC-80-UBS

NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 7	Soft	16-bit timer/event counters 00, 01	ES0n0, ES0n1	Set the valid edge of the TI00n pin while the timer operation is stopped (TMC0n3 and TMC0n2 = 00). Set the valid edge by using ES0n0 and ES0n1.	p. 341 ☐
			Re-triggering one-shot pulse	Make sure that the trigger is not generated while an active level is being output in the one-shot pulse output mode. Be sure to input the next trigger after the current active level is output.	p. 341 ☐
			OVF0n	The OVF0n flag is set to 1 in the following case, as well as when TM0n overflows. Select the clear & start mode entered upon a match between TM0n and CR00n. →Set CR00n to FFFFH. →When TM0n matches CR00n and TM0n is cleared from FFFFH to 0000H	p. 342 ☐
				Even if the OVF0n flag is cleared to 0 after TM0n overflows and before the next count clock is counted (before the value of TM0n becomes 0001H), it is set to 1 again and clearing is invalid.	p. 342 ☐
			One-shot pulse output	One-shot pulse output operates correctly in the free-running timer mode or the clear & start mode entered by the TI00n pin valid edge. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM0n and CR00n.	p. 342 ☐
			TI00n	When the valid edge of TI00n is specified as the count clock, the capture register for which TI00n is specified as a trigger does not operate correctly.	p. 343 ☐
	Hard		TI00n, TI01n	To accurately capture the count value, the pulse input to the TI00n and TI01n pins as a capture trigger must be wider than two count clocks selected by PRM0n (see Figure 7-9).	p. 343 ☐
			INTTM00n, INTTM01n	The capture operation is performed at the falling edge of the count clock but the interrupt signals (INTTM00n and INTTM01n) are generated at the rising edge of the next count clock (see Figure 7-9).	p. 343 ☐
	Soft		CRC0n1 = 1	When the count value of the TM0n register is captured to the CR00n register in the phase reverse to the signal input to the TI00n pin, the interrupt signal (INTTM00n) is not generated after the count value is captured. If the valid edge is detected on the TI01n pin during this operation, the capture operation is not performed but the INTTM00n signal is generated as an external interrupt signal. Mask the INTTM00n signal when the external interrupt is not used.	p. 343 ☐
	Hard		Specifying valid edge after reset	If the operation of the 16-bit timer/event counter 0n is enabled after reset and while the TI00n or TI01n pin is at high level and when the rising edge or both the edges are specified as the valid edge of the TI00n or TI01n pin, then the high level of the TI00n or TI01n pin is detected as the rising edge. Note this when the TI00n or TI01n pin is pulled up. However, the rising edge is not detected when the operation is once stopped and then enabled again.	p. 343 ☐
			Sampling clock for eliminating noise	The sampling clock for eliminating noise differs depending on whether the valid edge of TI00n is used as the count clock or capture trigger. In the former case, the sampling clock is fixed to f_{PRS}. In the latter, the count clock selected by PRM0n is used for sampling. When the signal input to the TI00n pin is sampled and the valid level is detected two times in a row, the valid edge is detected. Therefore, noise having a short pulse width can be eliminated (see Figure 7-9).	p. 343 ☐
			TI00n/TI01n	The signal input to the TI00n/TI01n pin is not acknowledged while the timer is stopped, regardless of the operation mode of the CPU.	p. 343 ☐
			Reading of TM0n	TM0n can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.	p. 344 ☐
Chapter 8	Soft	8-bit timer/event counters 50, 51	CR5n: 8-bit timer compare register 5n	In the mode in which clear & start occurs on a match of TM5n and CR5n (TMC5n6 = 0), do not write other values to CR5n during operation.	p. 347 ☐
				In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.	p. 347 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 14	Soft	Serial interface UART0	POWER0, TXE0, RXE0: Bits 7, 6, 5 of ASIM0	Clear POWER0 to 0 after clearing TXE0 and RXE0 to 0 to set the operation stop mode. To start the communication, set POWER0 to 1, and then set TXE0 or RXE0 to 1.	p. 441 ☐
			UART mode	Take relationship with the other party of communication when setting the port mode register and port register.	p. 442 ☐
			UART transmission	After transmit data is written to TXS0, do not write the next transmit data before the transmission completion interrupt signal (INTST0) is generated.	p. 445 ☐
			UART reception	If a reception error occurs, read asynchronous serial interface reception error status register 0 (ASIS0) and then read receive buffer register 0 (RXB0) to clear the error flag. Otherwise, an overrun error will occur when the next data is received, and the reception error status will persist.	p. 446 ☐
				Reception is always performed with the “number of stop bits = 1”. The second stop bit is ignored.	p. 446 ☐
			Error of baud rate	Keep the baud rate error during transmission to within the permissible error range at the reception destination.	p. 450 ☐
				Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.	p. 450 ☐
			Permissible baud rate range during reception	Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.	p. 451 ☐
Chapter 15	Soft	Serial interface UART6	UART mode	The TxD6 output inversion function inverts only the transmission side and not the reception side. To use this function, the reception side must be ready for reception of inverted data.	p. 453 ☐
				If clock supply to serial interface UART6 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART6 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD6 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER6 = 0, RXE6 = 0, and TXE6 = 0.	p. 453 ☐
				Set POWER6 = 1 and then set TXE6 = 1 (transmission) or RXE6 = 1 (reception) to start communication.	p. 453 ☐
				TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.	p. 453 ☐
				Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.	p. 453 ☐
				If data is continuously transmitted, the communication timing from the stop bit to the next start bit is extended two operating clocks of the macro. However, this does not affect the result of communication because the reception side initializes the timing when it has detected a start bit. Do not use the continuous transmission function if the interface is used in LIN communication operation.	p. 453 ☐
			TXB6: Transmit buffer register 6	Do not write data to TXB6 when bit 1 (TXBF6) of asynchronous serial interface transmission status register 6 (ASIF6) is 1.	p. 459 ☐
				Do not refresh (write the same value to) TXB6 by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) are 1 or when bits 7 and 5 (POWER6, RXE6) of ASIM6 are 1).	p. 459 ☐
				Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.	p. 459 ☐

<R> E.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

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Edition	Description	Chapter
3nd Edition	Addition of the conventional-specification products (μPD78F05xx, 78F05xx(A), 78F05xx(A2))	Throughout
	Addition of the (A2) grade products of expanded-specification products (μPD78F05xxA(A2))	
	Addition of the 64-pin plastic FBGA (4x4) package	
	Addition of SM+ tor 78K0	
	Deletion of QB-78K0MINI, PG-FPL3, and FP-LITE3 (because of discontinued products)	
	Addition of **Differences Between Conventional-specification Products and Expanded-specification Products**	**INTRODUCTION**
	Modification of **Related Documents**	
	Addition of **1.1 Differences Between Conventional-specification Products (μPD78F05xx and 78F05xxD) and Expanded-specification Products (μPD78F05xxA and 78F05xxDA)**	**CHAPTER 1 OUTLINE**
	Modification of **1.4 Ordering Information**	
	Modification of **1.8 Outline of Functions**	
	Modification of **Table 3-1 Set Values of Internal Memory Size Switching Register (IMS) (78K0/KB2, and 38-pin products and 44-pin products of the 78K0/KC2)** and **Table 3-2 Set Values of Internal Memory Size Switching Register (IMS) and Internal Expansion RAM Size Switching Register (IXS) (48-pin products of the 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)**	**CHAPTER 3 CPU ARCHITECTURE**
	Addition of description in **3.2.1 (2) Program status word (PSW)**	
	Modification of **Notes 2 to 4** in **Table 3-8 Special Function Register List (5/5)**	
	Addition of **Caution 2** to **5.2.2 Port 1**	**CHAPTER 5 PORT FUNCTIONS**
	Modification of **Caution** in **Figure 5-17 Block Diagram of P60 and P61** and **Figure 5-18 Block Diagram of P62**	
	Addition of **Caution 2** to **Figure 6-3. Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KB2)** and **Figure 6-4 Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)**	**CHAPTER 6 CLOCK GENERATOR**
	Modification of **Note 1** in and addition of **Note 2** to **Figure 6-15 Clock Generator Operation When Power Supply Voltage Is Turned On (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0))**	
	Addition of **Note** to **Figure 6-17 CPU Clock Status Transition Diagram (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0), 78K0/KB2)** and **Figure 6-18 CPU Clock Status Transition Diagram (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0), 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)**	
	Modification of **Note 1** in and addition of **Note 3** to **Figure 7-13 Format of Prescaler Mode Register 00 (PRM00)** and **Figure 7-14 Format of Prescaler Mode Register 01 (PRM01)**	**CHAPTER 7 16-BIT TIMER/EVENT COUNTERS 00 AND 01**
	Modification of description in **(f) 16-bit capture/compare register 00n (CR00n)** in **Figure 7-46 Example of Register Settings for PPG Output Operation (2/2)**	