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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0535gc-ubs-a

(2) Expanded-specification products (μPD78F05xxA and 78F05xxDA) (2/3)

<3> When high-speed system clock (X1 oscillation or external clock input) is used and entry RAM is located outside short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		34/f_{CPU}			
Initialize library		55/f_{CPU} + 594			
Mode check library		36/f_{CPU} + 495		30/f_{CPU} + 495	
Block blank check library		179/f_{CPU} + 6429		136/f_{CPU} + 6429	
Block erase library		179/f_{CPU} + 19713	179/f_{CPU} + 268079	136/f_{CPU} + 19713	136/f_{CPU} + 268079
Word write library		333/f_{CPU} + 647 + 136 × w	333/f_{CPU} + 647 + 1647 × w	272/f_{CPU} + 647 + 136 × w	272/f_{CPU} + 647 + 1647 × w
Block verify library		179/f_{CPU} + 13284		136/f_{CPU} + 13284	
Self programming end library		34/f_{CPU}			
Get information library	Option value: 03H	180/f_{CPU} + 581		134f_{CPU} + 581	
	Option value: 04H	190/f_{CPU} + 574		144/f_{CPU} + 574	
	Option value: 05H	350/f_{CPU} + 535		304/f_{CPU} + 535	
Set information library		80/f_{CPU} + 43181	80/f_{CPU} + 572934	72/f_{CPU} + 43181	72/f_{CPU} + 572934
EEPROM write library		333/f_{CPU} + 729 + 209 × w	333/f_{CPU} + 729 + 1722 × w	268/f_{CPU} + 729 + 209 × w	268/f_{CPU} + 729 + 1722 × w

Remarks 1. The above processing times are those when a write start address structure is located in the internal high-speed RAM and during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

3. f_{CPU}: CPU operation clock frequency

4. w: Number of words in write data (1 word = 4 bytes)

2.1.4 78K0/KE2

(1) Port functions (1/2): 78K0/KE2

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P02				SO11[Note 1]
P03				SI11[Note 1]
P04				$\overline{\text{SCK11}}$[Note 1]
P05				TI001[Note 1]/ $\overline{\text{SSI11}}$[Note 1]
P06				TI011[Note 1]/ TO01[Note 1]
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0 to ANI7
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1
P31				INTP2/OCD1A[Note 2]
P32				INTP3/OCD1B[Note 2]
P33				TI51/TO51/INTP4
P40 to P43	I/O	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	−
P50 to P53	I/O	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	−
P60	I/O	Port 6. 4-bit I/O port. Output of P60 to P63 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P62				EXSCL0
P63				−

Notes 1. Available only in the products whose flash memory is at least 48 KB.

2. μPD78F0537D and 78F0537DA (product with on-chip debug function) only

2.2.6 P50 to P57 (port 5)

P50 to P57 function as an I/O port. P50 to P57 can be set to input or output port in 1-bit units using port mode register 5 (PM5). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 5 (PU5).

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P50	–			√		√
P51	–			√		√
P52	–			√		√
P53	–			√		√
P54	–			–		√
P55	–			–		√
P56	–			–		√
P57	–			–		√

Remark √: Mounted, –: Not mounted

2.2.7 P60 to P67 (port 6)

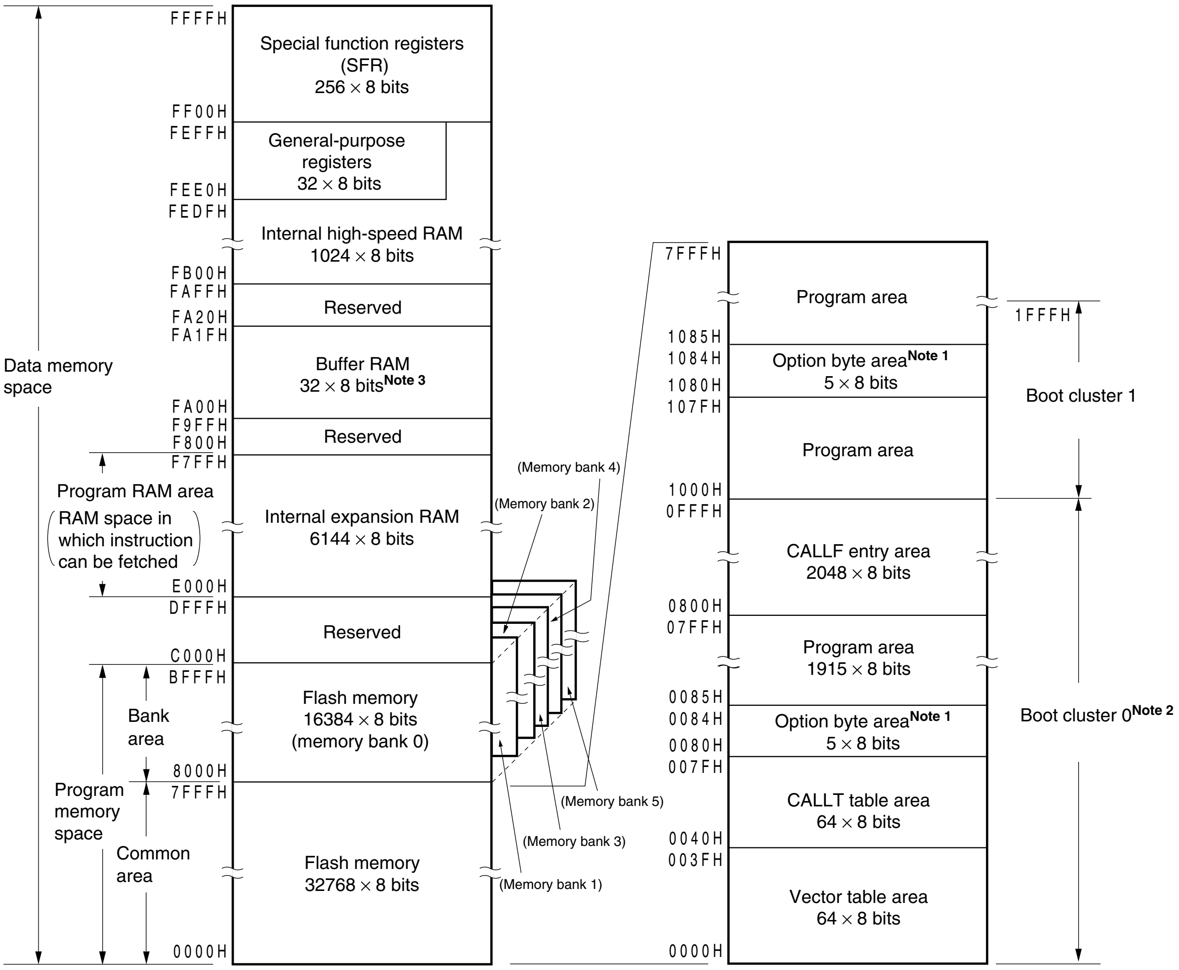
P60 to P67 function as an I/O port. These pins also function as pins for serial interface data I/O, clock I/O, and external clock input.

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P60/SCL0	√	√				√
P61/SDA0	√	√				√
P62/EXSCL0	–	√				√
P63	–	√				√
P64	–	–				√
P65	–	–				√
P66	–	–				√
P67	–	–				√

Remark √: Mounted, –: Not mounted

The following operation modes can be specified in 1-bit units.

Figure 3-10. Memory Map (μPD78F0527, 78F0527A, 78F0537, 78F0537A, 78F0547, and 78F0547A)

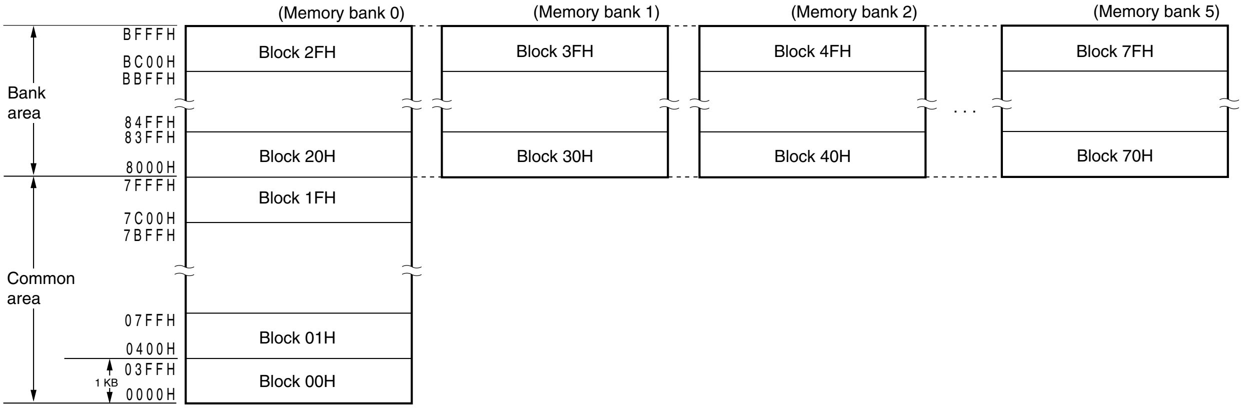

FFFFH
Special function registers (SFR) 256 × 8 bits
FF00H
FEFFH
General-purpose registers 32 × 8 bits
FEE0H
FEDFH
Internal high-speed RAM 1024 × 8 bits
FB00H
FAFFH
Reserved
FA20H
FA1FH
Buffer RAM 32 × 8 bitsNote 3
FA00H
F9FFH
Reserved
F800H
F7FFH
Internal expansion RAM 6144 × 8 bits
E000H
DFFFH
Reserved
C000H
BFFFH
Flash memory 16384 × 8 bits (memory bank 0)
8000H
7FFFH
Flash memory 32768 × 8 bits
0000H
Data memory space
Program RAM area
RAM space in which instruction can be fetched
Bank area
Program memory space
Common area
(Memory bank 4)
(Memory bank 2)
(Memory bank 5)
(Memory bank 3)
(Memory bank 1)
7FFFH
Program area
1085H
1084H
Option byte areaNote 1 5 × 8 bits
1080H
107FH
Program area
1000H
0FFFH
CALLF entry area 2048 × 8 bits
0800H
07FFH
Program area 1915 × 8 bits
0085H
0084H
Option byte areaNote 1 5 × 8 bits
0080H
007FH
CALLT table area 64 × 8 bits
0040H
003FH
Vector table area 64 × 8 bits
0000H
1FFFH
Boot cluster 1
Boot cluster 0Note 2

Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H.
When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

3. The buffer RAM is incorporated only in the μPD78F0547 and 78F0547A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0527, 78F0527A, 78F0537 and 78F0537A.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.



(2) CALLT instruction table area

The 64-byte area 0040H to 007FH can store the subroutine entry address of a 1-byte call instruction (CALLT).

(3) Option byte area

A 5-byte area of 0080H to 0084H and 1080H to 1084H can be used as an option byte area. Set the option byte at 0080H to 0084H when the boot swap is not used, and at 0080H to 0084H and 1080H to 1084H when the boot swap is used. For details, see **CHAPTER 26 OPTION BYTE**.

(4) CALLF instruction entry area

The area 0800H to 0FFFH can perform a direct subroutine call with a 2-byte call instruction (CALLF).

(5) On-chip debug security ID setting area (μPD78F05xxD and 78F05xxDA only)

A 10-byte area of 0085H to 008EH and 1085H to 108EH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 0085H to 008EH when the boot swap is not used and at 0085H to 008EH and 1085H to 108EH when the boot swap is used. For details, see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD and 78F05xxDA ONLY)**.

3.1.2 Memory bank (products whose flash memory is at least 96 KB only)

The 16 KB area 8000H to BFFFH is assigned to memory banks 0 to 3 in the μPD78F05x6 and 78F05x6A (x = 2 to 4), and assigned to memory banks 0 to 5 in the μPD78F05x7, 78F05x7A, 78F05x7D and 78F05x7DA (x = 2 to 4).

The banks are selected by using a memory bank select register (BANK). For details, see **CHAPTER 4 MEMORY BANK SELECT FUNCTION (PRODUCTS WHOSE FLASH MEMORY IS AT LEAST 96 KB ONLY)**.

Cautions 1. Instructions cannot be fetched between different memory banks.

2. Branch and access cannot be directly executed between different memory banks. Execute branch or access between different memory banks via the common area.

3. Allocate interrupt servicing in the common area.

4. An instruction that extends from 7FFFH to 8000H can only be executed in memory bank 0.

Figure 5-33. Format of Port Mode Register (78K0/KF2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FF24H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FF27H	FFH	R/W
PM12	1	1	1	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W
PM14	1	1	PM145	PM144	PM143	PM142	PM141	PM140	FF2EH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 7, 12, 14; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bit 7 of PM0, bits 4 to 7 of PM3, bits 5 to 7 of PM12, and bits 6 and 7 of PM14 to “1”.

Table 5-6. Settings of Port Mode Register and Output Latch When Using Alternate Function (2/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P30 to P32	INTP1 to INTP3	Input	1	×
P33	INTP4	Input	1	×
	TI51	Input	1	×
	TO51	Output	0	0
P60	SCL0	I/O	0	0
P61	SDA0	I/O	0	0
P62	EXSCL0	Input	1	×
P70 to P77	KR0 to KR7	Input	1	×
P120	INTP0	Input	1	×
	EXLVI	Input	1	×
P121	X1[Note]	–	×	×
P122	X2[Note]	–	×	×
	EXCLK[Note]	Input	×	×
P123	XT1[Note]	–	×	×
P124	XT2[Note]	–	×	×
	EXCLKS[Note]	Input	×	×
P140	PCL	Output	0	0
	INTP6	Input	1	×
P141	BUZ	Output	0	0
	INTP7	Input	1	×
	BUSY0	Input	1	×
P142	$\overline{\text{SCKA0}}$	Input	1	×
		Output	0	1
P143	SIA0	Input	1	×
P144	SOA0	Output	0	0
P145	STB0	Output	0	0

Note When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK) or subsystem clock (EXCLKS), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **6.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are I/O port pins). At this time, setting of PM121 to PM124 and P121 to P124 is not necessary.

Remarks 1. ×: Don’t care
PM××: Port mode register
P××: Port output latch

2. X1, X2, P31, and P32 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A, OCD0B, OCD1A, and OCD1B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD AND 78F05xxDA ONLY).**

7.2 Configuration of 16-Bit Timer/Event Counters 00 and 01

16-bit timer/event counters 00 and 01 include the following hardware.

Table 7-1. Configuration of 16-Bit Timer/Event Counters 00 and 01

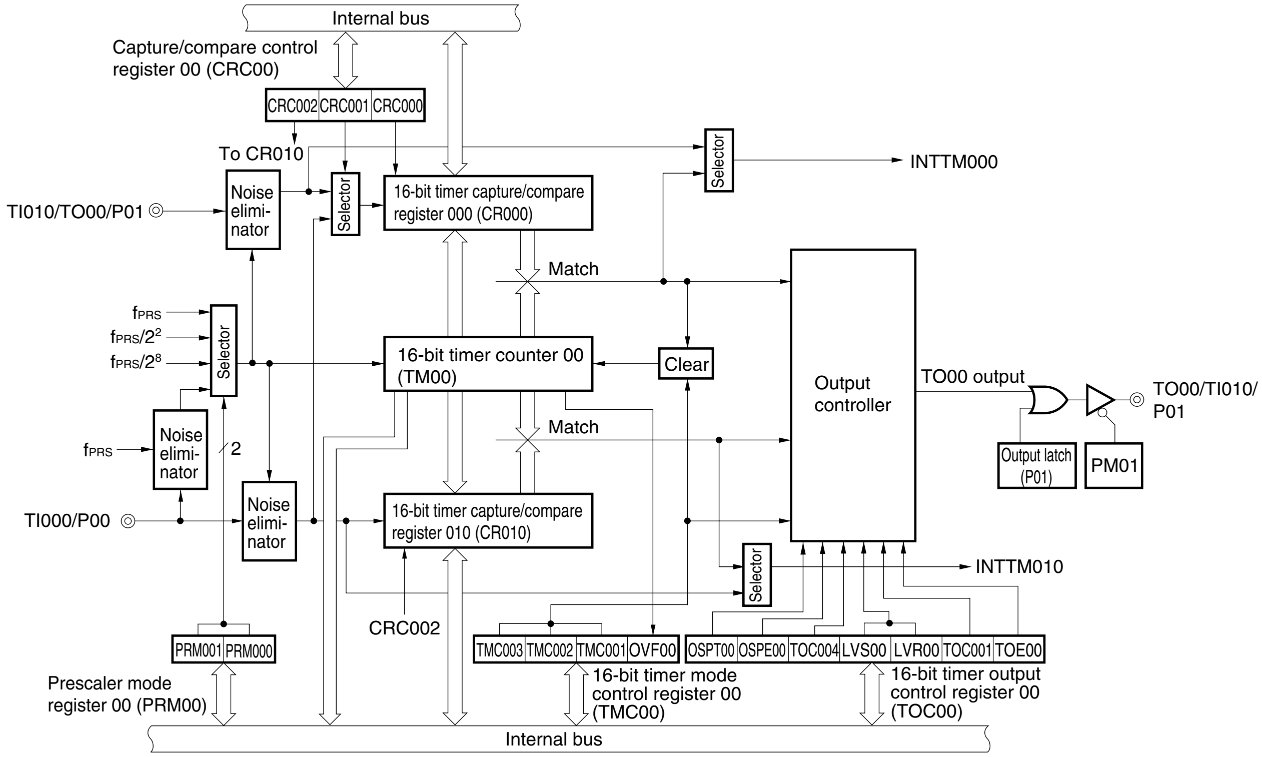
Item	Configuration
Time/counter	16-bit timer counter 0n (TM0n)
Register	16-bit timer capture/compare registers 00n, 01n (CR00n, CR01n)
Timer input	TI00n, TI01n pins
Timer output	TO0n pin, output controller
Control registers	16-bit timer mode control register 0n (TMC0n) 16-bit timer capture/compare control register 0n (CRC0n) 16-bit timer output control register 0n (TOC0n) Prescaler mode register 0n (PRM0n) Port mode register 0 (PM0) Port register 0 (P0)

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figures 7-1 and 7-2 show the block diagrams.

Figure 7-1. Block Diagram of 16-Bit Timer/Event Counter 00


Internal bus
Capture/compare control register 00 (CRC00)
CRC002 CRC001 CRC000
To CR010
TI010/TO00/P01
Noise elimi-nator
Selector
16-bit timer capture/compare register 000 (CR000)
Selector
INTTM000
Match
fPRS
fPRS/2^2
fPRS/2^8
Selector
16-bit timer counter 00 (TM00)
Clear
Output controller
TO00 output
TO00/TI010/P01
fPRS
Noise elimi-nator
2
Match
Output latch (P01)
PM01
TI000/P00
Noise elimi-nator
16-bit timer capture/compare register 010 (CR010)
Selector
INTTM010
CRC002
PRM001 PRM000
TMC003 TMC002 TMC001 OVF00
OSPT00 OSPE00 TOC004 LVS00 LVR00 TOC001 TOE00
Prescaler mode register 00 (PRM00)
16-bit timer mode control register 00 (TMC00)
16-bit timer output control register 00 (TOC00)
Internal bus

(Cautions 1 to 3 are listed on the next page.)

Figure 7-56. Example of Register Settings for Pulse Width Measurement (1/2)

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	0/1	0/1	0	0

01: Free running timer mode
10: Clear and start mode entered by valid edge of TI00n pin.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	1	0/1	1

1: CR00n used as capture register

0: TI01n pin is used as capture trigger of CR00n.
1: Reverse phase of TI00n pin is used as capture trigger of CR00n.

1: CR01n used as capture register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0	0	0	0

(d) Prescaler mode register 0n (PRM0n)

ES1n1	ES1n0	ES0n1	ES0n0	3	2	PRM0n1	PRM0n0
0/1	0/1	0/1	0/1	0	0	0/1	0/1

Selects count clock
(setting valid edge of TI00n is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection
(setting when CRC0n1 = 1 is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Remark If the overflow time is set to $2^{11}/f_{RL}$, the window close time and open time are as follows.

(when 2.7 V $\leq$ V_{DD} $\leq$ 5.5 V)

	Setting of Window Open Period			
	25%	50%	75%	100%
Window close time	0 to 7.11 ms	0 to 4.74 ms	0 to 2.37 ms	None
Window open time	7.11 to 7.76 ms	4.74 to 7.76 ms	2.37 to 7.76 ms	0 to 7.76 ms

<When window open period is 25%>

- Overflow time:
  $2^{11}/f_{RL}$ (MAX.) = $2^{11}/264$ kHz (MAX.) = 7.76 ms
- Window close time:
  0 to $2^{11}/f_{RL}$ (MIN.) $\times$ (1 $-$ 0.25) = 0 to $2^{11}/216$ kHz (MIN.) $\times$ 0.75 = 0 to 7.11 ms
- Window open time:
  $2^{11}/f_{RL}$ (MIN.) $\times$ (1 $-$ 0.25) to $2^{11}/f_{RL}$ (MAX.) = $2^{11}/216$ kHz (MIN.) $\times$ 0.75 to $2^{11}/264$ kHz (MAX.) = 7.11 to 7.76 ms

(3) Asynchronous serial interface transmission status register 6 (ASIF6)

This register indicates the status of transmission by serial interface UART6. It includes two status flag bits (TXBF6 and TXSF6).

Transmission can be continued without disruption even during an interrupt period, by writing the next data to the TXB6 register after data has been transferred from the TXB6 register to the TXS6 register.

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER6) or bit 6 (TXE6) of ASIM6 to 0 clears this register to 00H.

Figure 15-7. Format of Asynchronous Serial Interface Transmission Status Register 6 (ASIF6)

Address: FF55H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIF6	0	0	0	0	0	0	TXBF6	TXSF6

TXBF6	Transmit buffer data flag
0	If POWER6 = 0 or TXE6 = 0, or if data is transferred to transmit shift register 6 (TXS6)
1	If data is written to transmit buffer register 6 (TXB6) (if data exists in TXB6)

TXSF6	Transmit shift register data flag
0	If POWER6 = 0 or TXE6 = 0, or if the next data is not transferred from transmit buffer register 6 (TXB6) after completion of transfer
1	If data is transferred from transmit buffer register 6 (TXB6) (if data transmission is in progress)

Cautions 1. To transmit data continuously, write the first transmit data (first byte) to the TXB6 register. Be sure to check that the TXBF6 flag is “0”. If so, write the next transmit data (second byte) to the TXB6 register. If data is written to the TXB6 register while the TXBF6 flag is “1”, the transmit data cannot be guaranteed.

2. To initialize the transmission unit upon completion of continuous transmission, be sure to check that the TXSF6 flag is “0” after generation of the transmission completion interrupt, and then execute initialization. If initialization is executed while the TXSF6 flag is “1”, the transmit data cannot be guaranteed.

(4) Clock selection register 6 (CKSR6)

This register selects the base clock of serial interface UART6.

CKSR6 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Remark CKSR6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

(c) Bit shift detection by busy signal

During automatic transmission/reception, a bit shift of the serial clock of the slave device may occur because noise is superimposed on the serial clock signal output by the master device. Unless the strobe control option is used at this time, the bit shift affects transmission of the next byte. In this case, the master can detect the bit shift by checking the busy signal during transmission by using the busy control option.

A bit shift is detected by using the busy signal as follows:

The slave outputs the busy signal after the rising of the eighth serial clock during data transmission/reception (to not keep transmission/reception waiting by the busy signal at this time, make the busy signal inactive within 2 clocks).

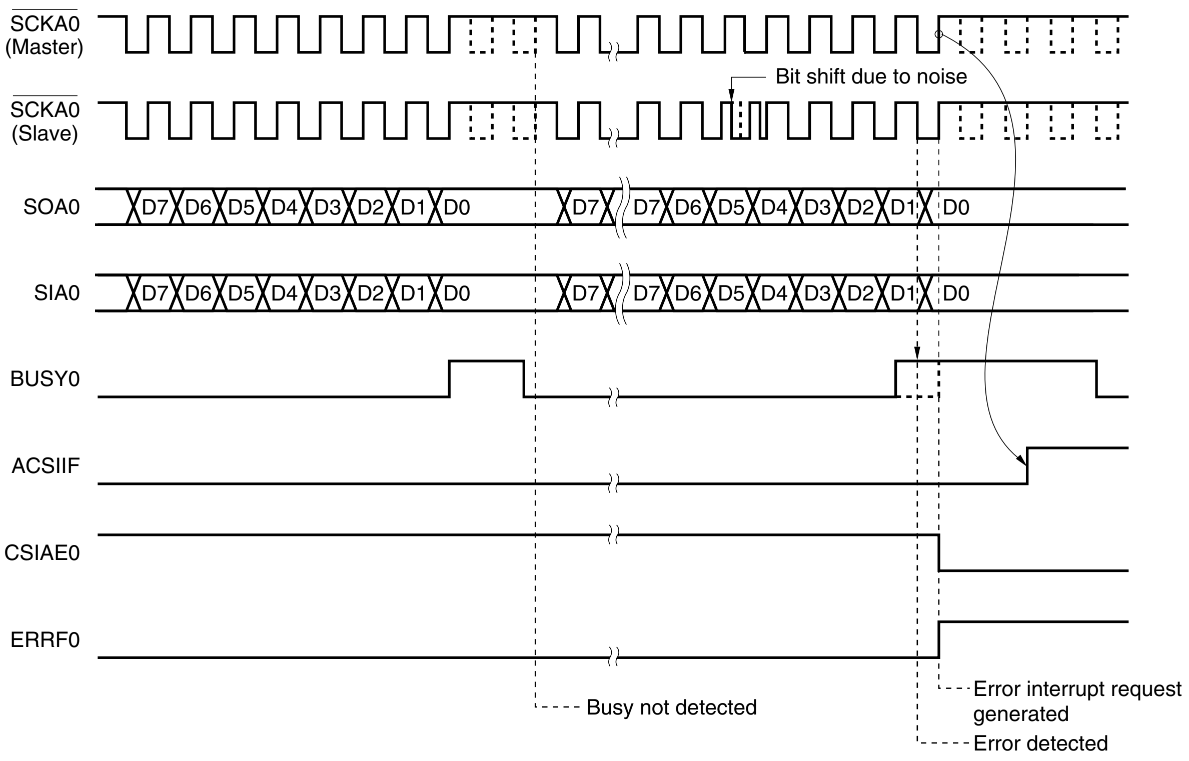
The master samples the busy signal in synchronization with the falling edge of the serial clock if bit 2 (ERRE0) of serial status register 0 (CSIS0) is set to 1. If a bit shift does not occur, all the eight serial clocks that have been sampled are inactive. If the sampled serial clocks are active, it is assumed that a bit shift has occurred, error processing is executed (by setting bit 1 (ERRF0) of serial status register 0 (CSIS0) to 1, and communication is suspended and an interrupt request signal (INTACSI) is output).

Although communication is suspended after completion of 1-byte data communication, slave signal output, wait due to the busy signal, and wait due to the interval time specified by ADTI0 are not executed.

If ERRE0 = 0, ERRF0 cannot become 1 even if a bit shift occurs.

Figure 17-27 shows the example of the operation timing of the bit shift detection function by the busy signal.

Figure 17-27. Example of Operation Timing of Bit Shift Detection Function by Busy Signal (When BUSYLV0 = 1)


$\overline{\text{SCKA0}}$
(Master)
Bit shift due to noise
$\overline{\text{SCKA0}}$
(Slave)
SOA0
D7 D6 D5 D4 D3 D2 D1 D0 D7 D7 D6 D5 D4 D3 D2 D1 D0
SIA0
D7 D6 D5 D4 D3 D2 D1 D0 D7 D7 D6 D5 D4 D3 D2 D1 D0
BUSY0
ACSIIF
CSIAE0
ERRF0
Busy not detected
Error interrupt request generated
Error detected

ACSIIF: Interrupt request flag

CSIAE0: Bit 7 of serial operation mode specification register 0 (CSIMA0)

ERRF0: Bit 1 of serial status register 0 (CSIS0)

18.5.4 Acknowledge ($\overline{\text{ACK}}$)

$\overline{\text{ACK}}$ is used to check the status of serial data at the transmission and reception sides.

The reception side returns $\overline{\text{ACK}}$ each time it has received 8-bit data.

The transmission side usually receives $\overline{\text{ACK}}$ after transmitting 8-bit data. When $\overline{\text{ACK}}$ is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether $\overline{\text{ACK}}$ has been detected can be checked by using bit 2 (ACKD0) of IIC status register 0 (IICS0).

When the master receives the last data item, it does not return $\overline{\text{ACK}}$ and instead generates a stop condition. If a slave does not return $\overline{\text{ACK}}$ after receiving data, the master outputs a stop condition or restart condition and stops transmission. If $\overline{\text{ACK}}$ is not returned, the possible causes are as follows.

<1> Reception was not performed normally.
<2> The final data item was received.
<3> The reception side specified by the address does not exist.

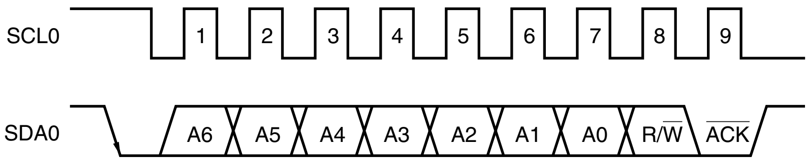
To generate $\overline{\text{ACK}}$, the reception side makes the SDA0 line low at the ninth clock (indicating normal reception).

Automatic generation of $\overline{\text{ACK}}$ is enabled by setting bit 2 (ACKE0) of IIC control register 0 (IICC0) to 1. Bit 3 (TRC0) of the IICS0 register is set by the data of the eighth bit that follows 7-bit address information. Usually, set ACKE0 bit to 1 for reception (TRC0 = 0).

If a slave can receive no more data during reception (TRC0 = 0) or does not require the next data item, then the slave must inform the master, by clearing ACKE0 bit to 0, that it will not receive any more data.

When the master does not require the next data item during reception (TRC0 = 0), it must clear ACKE0 bit to 0 so that $\overline{\text{ACK}}$ is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

Figure 18-16. $\overline{\text{ACK}}$



When the local address is received, $\overline{\text{ACK}}$ is automatically generated, regardless of the value of ACKE0 bit. When an address other than that of the local address is received, $\overline{\text{ACK}}$ is not generated (NACK).

When an extension code is received, $\overline{\text{ACK}}$ is generated if ACKE0 bit is set to 1 in advance.

How $\overline{\text{ACK}}$ is generated when data is received differs as follows depending on the setting of the wait timing.

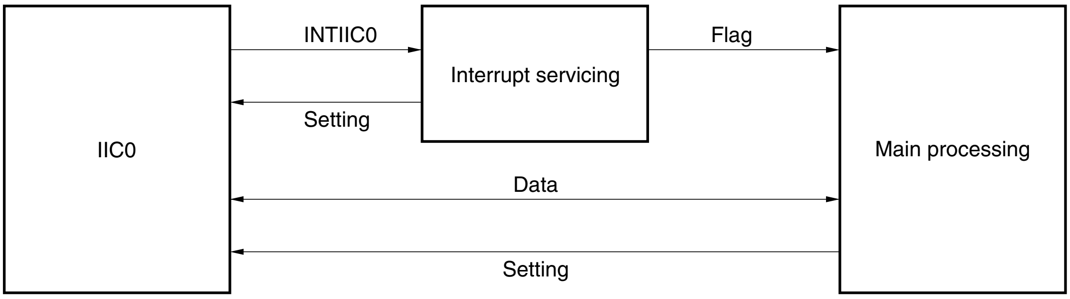
- When 8-clock wait state is selected (bit 3 (WTIM0) of IICC0 register = 0):
  By setting ACKE0 bit to 1 before releasing the wait state, $\overline{\text{ACK}}$ is generated at the falling edge of the eighth clock of the SCL0 pin.
- When 9-clock wait state is selected (bit 3 (WTIM0) of IICC0 register = 1):
  $\overline{\text{ACK}}$ is generated by setting ACKE0 bit to 1 in advance.

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIIC0 interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIIC0 interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIIC0.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

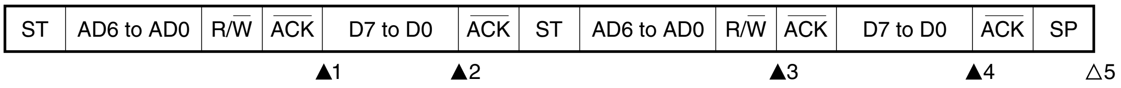
This flag indicates that data communication is enabled. Its function is the same as the INTIIC0 interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as TRC0.

(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= extension code))



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

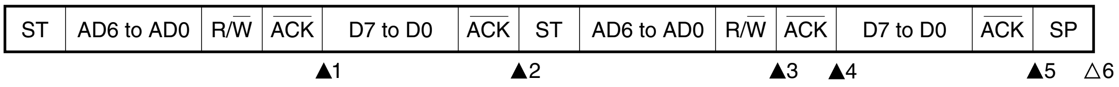
▲3: IICS0 = 0010×010B

▲4: IICS0 = 0010×000B

△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don’t care

(ii) When WTIM0 = 1 (after restart, does not match address (= extension code))



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001××00B

▲3: IICS0 = 0010×010B

▲4: IICS0 = 0010×110B

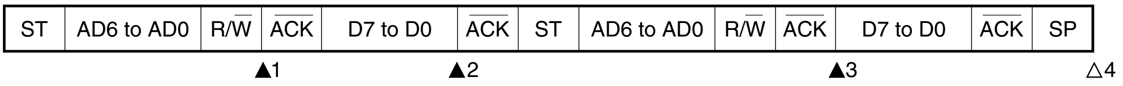
▲5: IICS0 = 0010××00B

△6: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don’t care

(d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))



▲1: IICS0 = 00100010B

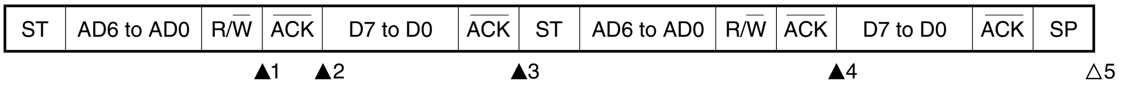
▲2: IICS0 = 00100000B

▲3: IICS0 = 00000110B

△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don’t care

(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))



▲1: IICS0 = 00100010B

▲2: IICS0 = 00100110B

▲3: IICS0 = 00100×00B

▲4: IICS0 = 00000110B

△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don’t care

Cautions 3. When using LVI as an interrupt, if LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

4. With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.

(2) Low-voltage detection level selection register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 25-3. Format of Low-Voltage Detection Level Selection Register (LVIS)

Address: FFBFH After reset: 00H[Note 1] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.24 V ±0.1 V)
0	0	0	1	V_{LVI1} (4.09 V ±0.1 V)
0	0	1	0	V_{LVI2} (3.93 V ±0.1 V)
0	0	1	1	V_{LVI3} (3.78 V ±0.1 V)
0	1	0	0	V_{LVI4} (3.62 V ±0.1 V)
0	1	0	1	V_{LVI5} (3.47 V ±0.1 V)
0	1	1	0	V_{LVI6} (3.32 V ±0.1 V)
0	1	1	1	V_{LVI7} (3.16 V ±0.1 V)
1	0	0	0	V_{LVI8} (3.01 V ±0.1 V)
1	0	0	1	V_{LVI9} (2.85 V ±0.1 V)
1	0	1	0	V_{LVI10} (2.70 V ±0.1 V) [Note 2]
1	0	1	1	V_{LVI11} (2.55 V ±0.1 V) [Note 2]
1	1	0	0	V_{LVI12} (2.39 V ±0.1 V) [Note 2]
1	1	0	1	V_{LVI13} (2.24 V ±0.1 V) [Note 2]
1	1	1	0	V_{LVI14} (2.08 V ±0.1 V) [Note 2]
1	1	1	1	V_{LVI15} (1.93 V ±0.1 V) [Note 2]

Notes 1. The value of LVIS is not reset but retained as is, upon a reset by LVI. It is cleared to 00H upon other resets.

2. Do not set V_{LVI10} to V_{LVI15} for (A2) grade products.

Cautions 1. Be sure to clear bits 4 to 7 to “0”.

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.

4. With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Bit manipulate	**AND1**	CY, saddr.bit	3	6	7	CY ← CY ∧ (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← CY ∧ sfr.bit			×
		CY, A.bit	2	4	–	CY ← CY ∧ A.bit			×
		CY, PSW.bit	3	–	7	CY ← CY ∧ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ∧ (HL).bit			×
	OR1	CY, saddr.bit	3	6	7	CY ← CY ∨ (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← CY ∨ sfr.bit			×
		CY, A.bit	2	4	–	CY ← CY ∨ A.bit			×
		CY, PSW.bit	3	–	7	CY ← CY ∨ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ∨ (HL).bit			×
	XOR1	CY, saddr.bit	3	6	7	CY ← CY ⊻ (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← CY ⊻ sfr.bit			×
		CY, A.bit	2	4	–	CY ← CY ⊻ A.bit			×
		CY, PSW. bit	3	–	7	CY ← CY ⊻ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ⊻ (HL).bit			×
	SET1	saddr.bit	2	4	6	(saddr.bit) ← 1			
		sfr.bit	3	–	8	sfr.bit ← 1			
		A.bit	2	4	–	A.bit ← 1			
		PSW.bit	2	–	6	PSW.bit ← 1	×	×	×
		[HL].bit	2	6	8	(HL).bit ← 1			
	CLR1	saddr.bit	2	4	6	(saddr.bit) ← 0			
		sfr.bit	3	–	8	sfr.bit ← 0			
		A.bit	2	4	–	A.bit ← 0			
		PSW.bit	2	–	6	PSW.bit ← 0	×	×	×
		[HL].bit	2	6	8	(HL).bit ← 0			
	SET1	CY	1	2	–	CY ← 1			1
	CLR1	CY	1	2	–	CY ← 0			0
	NOT1	CY	1	2	–	CY ← $\overline{\text{CY}}$			×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

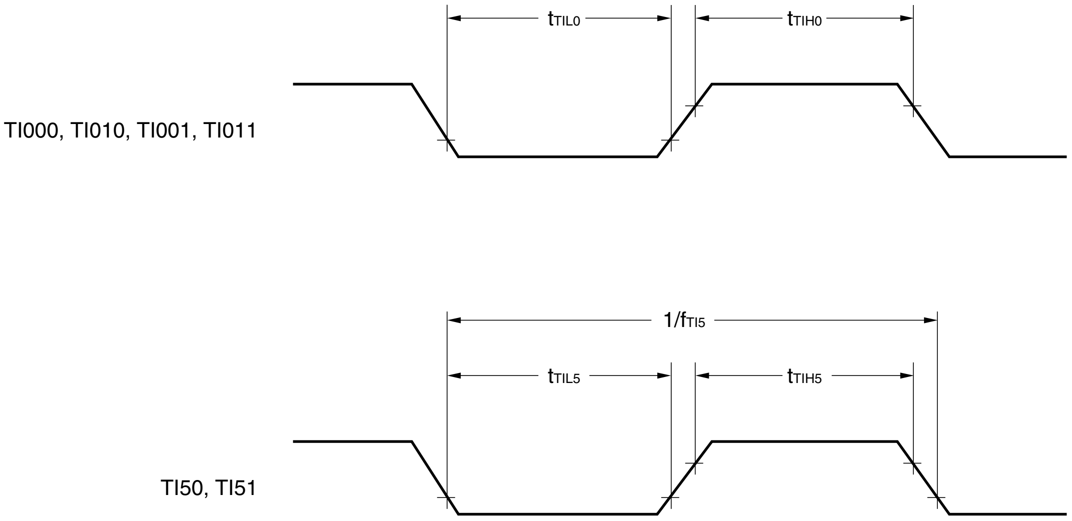
2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

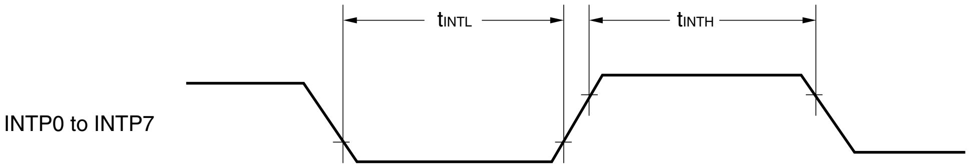
2. This clock cycle applies to the internal ROM program.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

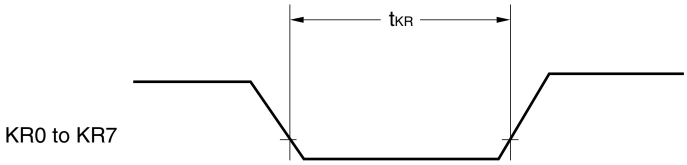
TI Timing



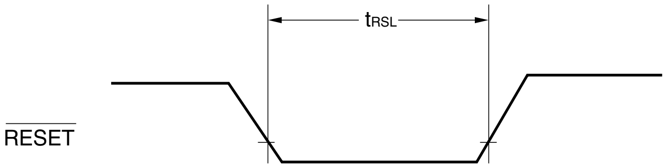
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 7	Soft	16-bit timer/event counters 00, 01	PRM0n: Prescaler mode register 0n	Do not apply the following setting when setting the PRM0n1 and PRM0n0 bits to 11 (to specify the valid edge of the TI00n pin as a count clock). • Clear & start mode entered by the TI00n pin valid edge • Setting the TI00n pin as a capture trigger	p. 285 □
				If the operation of the 16-bit timer/event counter 0n is enabled when the TI00n or TI01n pin is at high level and when the valid edge of the TI00n or TI01n pin is specified to be the rising edge or both edges, the high level of the TI00n or TI01n pin is detected as a rising edge. Note this when the TI00n or TI01n pin is pulled up. However, the rising edge is not detected when the timer operation has been once stopped and then is enabled again.	p. 285 □
	Hard			The valid edge of TI010 and timer output (TO00) cannot be used for the P01 pin at the same time, and the valid edge of TI011 and timer output (TO01) cannot be used for the P06 pin at the same time. Select either of the functions.	p. 285 □
	Soft		Clear & start mode entered by TI00n pin valid edge input	Do not set the count clock as the valid edge of the TI00n pin (PRM0n1 and PRM0n0 = 11). When PRM0n1 and PRM0n0 = 11, TM0n may be cleared.	p. 299 □
			PPG output	To change the duty factor (value of CR01n) during operation, see 7.5.1 Rewriting CR01n during TM0n operation.	p. 321 □
				Set values to CR00n and CR01n such that the condition 0000H ≤ CR01n < CR00n ≤ FFFFH is satisfied.	p. 323 □
			One-shot pulse output	Do not input the trigger again (setting OSPT0n to 1 or detecting the valid edge of the TI00n pin) while the one-shot pulse is output. To output the one-shot pulse again, generate the trigger after the current one-shot pulse output has completed.	p. 325 □
				To use only the setting of OSPT0n to 1 as the trigger of one-shot pulse output, do not change the level of the TI00n pin or its alternate function port pin. Otherwise, the pulse will be unexpectedly output.	p. 325 □
				Do not set the same value to CR00n and CR01n.	p. 327 □
			LVS0n, LVRn0	Be sure to set LVS0n and LVR0n following steps <1>, <2>, and <3> above. Step <2> can be performed after <1> and before <3>.	p. 339 □
			–	Table 7-3 shows the restrictions for each channel.	p. 340 □
	Hard		Timer start errors	An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM0n is started asynchronously to the count pulse.	p. 340 □
	Soft		CR00n, CR01n: 16-bit timer capture/compare registers 00n, 01n	Set a value other than 0000H to CR00n and CR01n in clear & start mode entered upon a match between TM0n and CR00n (TM0n cannot count one pulse when it is used as an external event counter).	p. 340 □
				When the valid edge is input to the TI00n/TI01n pin and the reverse phase of the TI00n pin is detected while CR00n/CR01n is read, CR01n performs a capture operation but the read value of CR00n/CR01n is not guaranteed. At this time, an interrupt signal (INTTM00n/INTTM01n) is generated when the valid edge of the TI00n/TI01n pin is detected (the interrupt signal is not generated when the reverse-phase edge of the TI00n pin is detected). When the count value is captured because the valid edge of the TI00n/TI01n pin was detected, read the value of CR00n/CR01n after INTTM00n/INTTM01n is generated.	p. 341 □
				The values of CR00n and CR01n are not guaranteed after 16-bit timer/event counter 0n stops.	p. 341 □