Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFLGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0536afc-aa1-a

CHAPTER 15 SERIAL INTERFACE UART6 453

15.1 Functions of Serial Interface UART6 453
15.2 Configuration of Serial Interface UART6 457
15.3 Registers Controlling Serial Interface UART6 460
15.4 Operation of Serial Interface UART6 469
15.4.1 Operation stop mode 469
15.4.2 Asynchronous serial interface (UART) mode 470
15.4.3 Dedicated baud rate generator 483
15.4.4 Calculation of baud rate 484

CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11 490

16.1 Functions of Serial Interfaces CSI10 and CSI11 490
16.2 Configuration of Serial Interfaces CSI10 and CSI11 491
16.3 Registers Controlling Serial Interfaces CSI10 and CSI11 493
16.4 Operation of Serial Interfaces CSI10 and CSI11 499
16.4.1 Operation stop mode 499
16.4.2 3-wire serial I/O mode 500

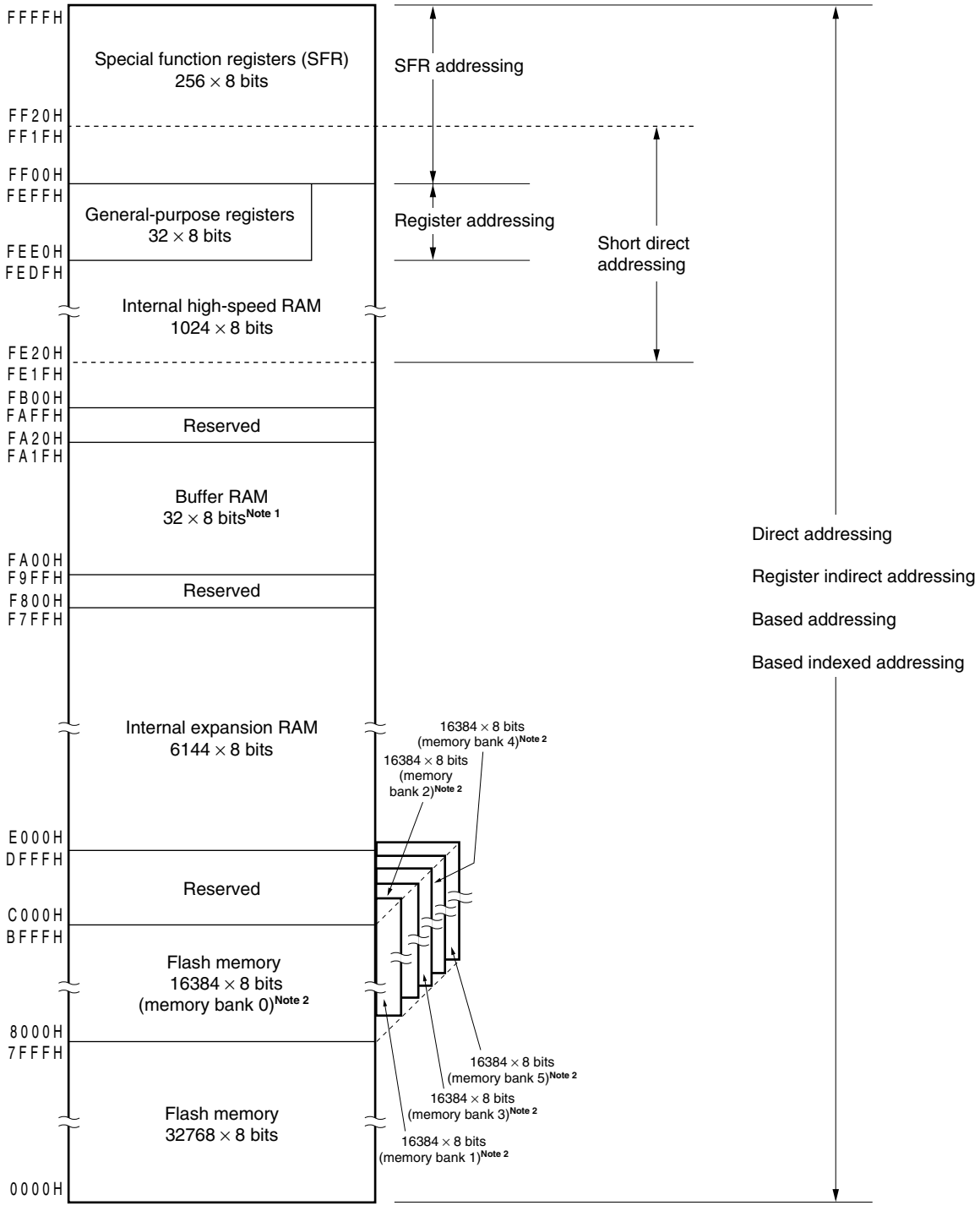
CHAPTER 17 SERIAL INTERFACE CSIA0 512

17.1 Functions of Serial Interface CSIA0 512
17.2 Configuration of Serial Interface CSIA0 513
17.3 Registers Controlling Serial Interface CSIA0 515
17.4 Operation of Serial Interface CSIA0 524
17.4.1 Operation stop mode 524
17.4.2 3-wire serial I/O mode 525
17.4.3 3-wire serial I/O mode with automatic transmit/receive function 530

CHAPTER 18 SERIAL INTERFACE IIC0 550

18.1 Functions of Serial Interface IIC0 550
18.2 Configuration of Serial Interface IIC0 553
18.3 Registers to Control Serial Interface IIC0 556
18.4 I^2C Bus Mode Functions 569
18.4.1 Pin configuration 569
18.5 I^2C Bus Definitions and Control Methods 570
18.5.1 Start conditions 570
18.5.2 Addresses 571
18.5.3 Transfer direction specification 571
18.5.4 Acknowledge ($\overline{ACK}$) 572
18.5.5 Stop condition 573
18.5.6 Wait 574
18.5.7 Canceling wait 576
18.5.8 Interrupt request (INTIIC0) generation timing and wait control 576
18.5.9 Address match detection method 577
18.5.10 Error detection 577
18.5.11 Extension code 578
18.5.12 Arbitration 579
18.5.13 Wakeup function 580
18.5.14 Communication reservation 581

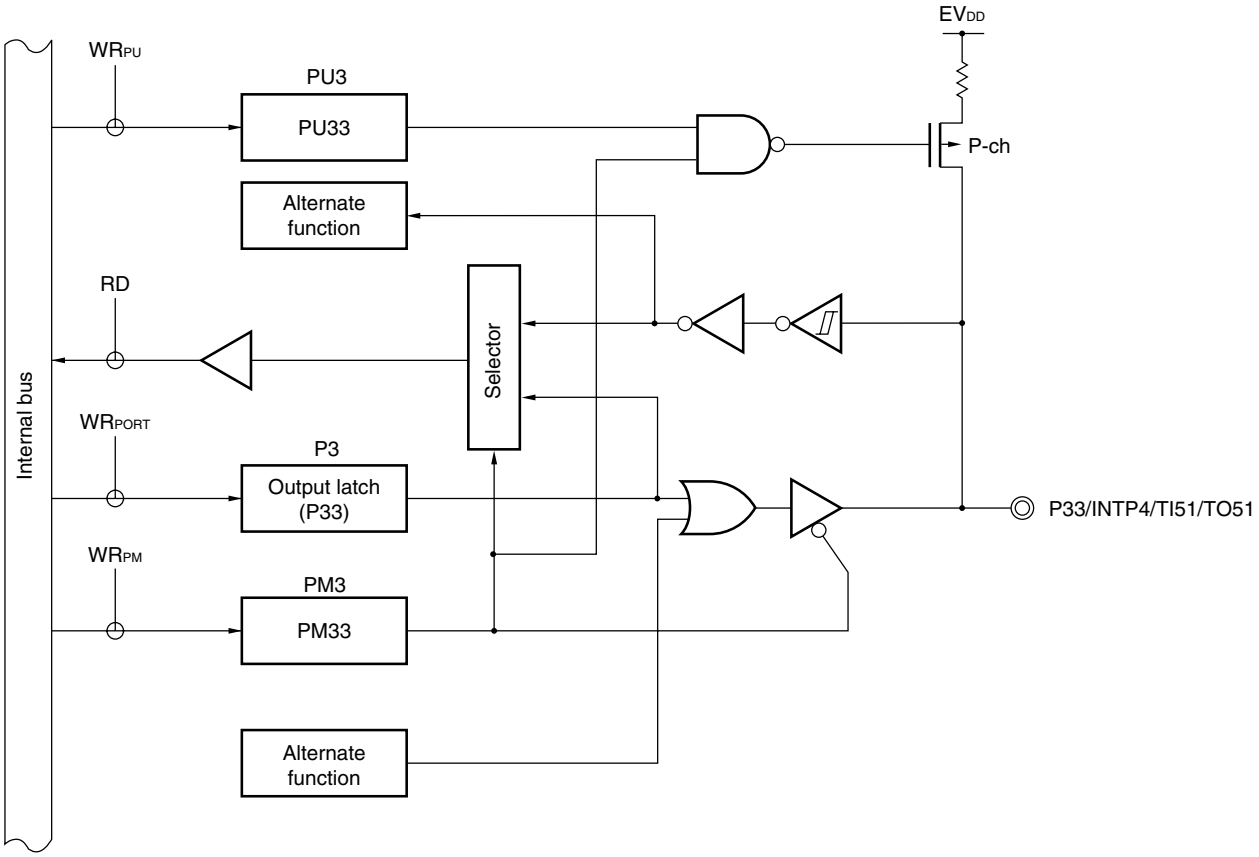
Figure 3-19. Correspondence Between Data Memory and Addressing
(μPD78F0527, 78F0527A, 78F0537, 78F0537A, 78F0547, 78F0547A, 78F0527D, 78F0527DA, 78F0537D, 78F0537DA, 78F0547D and 78F0547DA)



Notes 1. The buffer RAM is incorporated only in the μPD78F0547, 78F0547A, 78F0547D and 78F0547DA (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0527, 78F0527A, 78F0537, 78F0537A, 78F0527D, 78F0527DA, 78F0537D and 78F0537DA.

2. To branch to or address a memory bank that is not set by the memory bank select register (BANK), change the setting of the memory bank by using BANK.

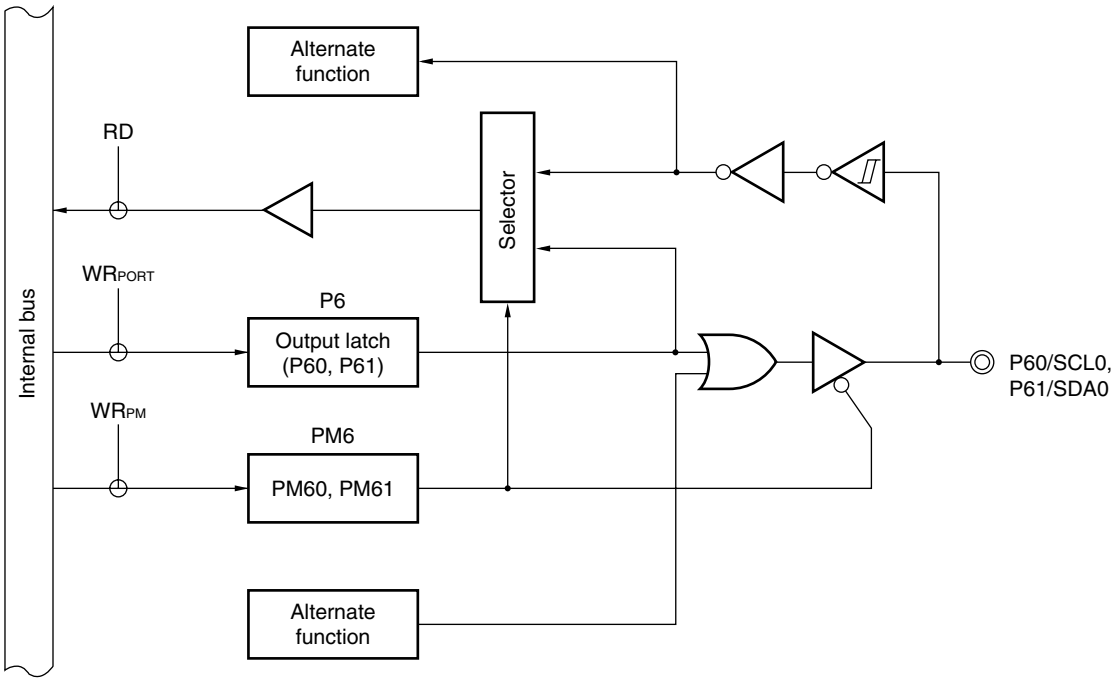
Figure 5-14. Block Diagram of P33



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-17. Block Diagram of P60 and P61

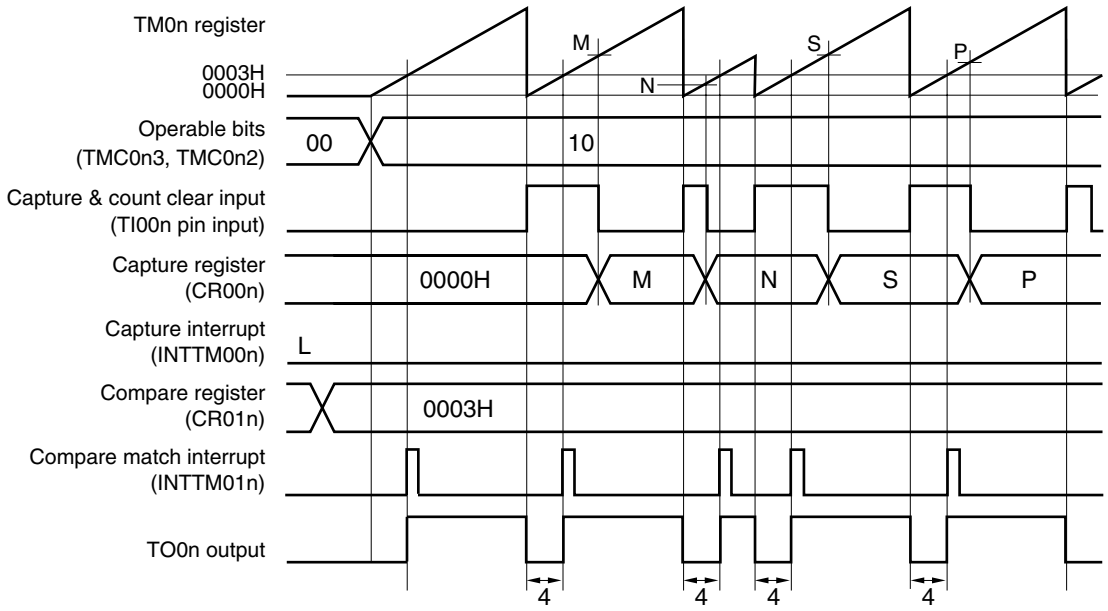


P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

Caution A through current flows through P60 and P61 if an intermediate potential is input to these pins, because the input buffer is also turned on when P60 and P61 are in output mode. Consequently, do not input an intermediate potential when P60 and P61 are in output mode.

Figure 7-32. Timing Example of Clear & Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register, CR01n: Compare Register) (2/2)

(b) TOC0n = 13H, PRM0n = 10H, CRC0n, = 03H, TMC0n = 0AH, CR01n = 0003H



This is an application example where the width set to CR01n (4 clocks in this example) is to be output from the TO0n pin when the count value has been captured & cleared.

TM0n is cleared (to 0000H) at the rising edge detection of the TI00n pin and captured to CR00n at the falling edge detection of the TI00n pin. The TO0n output level is inverted when TM0n is cleared (to 0000H) because the rising edge of the TI00n pin has been detected or when the value of TM0n matches that of a compare register (CR01n).

When bit 1 (CRC0n1) of capture/compare control register 0n (CRC0n) is 1, the count value of TM0n is captured to CR00n in the phase reverse to that of the input signal of the TI00n pin, but the capture interrupt signal (INTTM00n) is not generated. However, the INTTM00n interrupt is generated when the valid edge of the TI01n pin is detected. Mask the INTTM00n signal when it is not used.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(3) Port mode registers 1 and 3 (PM1, PM3)

These registers set port 1 and 3 input/output in 1-bit units.

When using the P17/TO50/TI50 and P33/TO51/TI51/INTP4 pins for timer output, clear PM17 and PM33 and the output latches of P17 and P33 to 0.

When using the P17/TO50/TI50 and P33/TO51/TI51/INTP4 pins for timer input, set PM17 and PM33 to 1. The output latches of P17 and P33 at this time may be 0 or 1.

PM1 and PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 8-9. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 8-10. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

12.4 Operations of Clock Output/Buzzer Output Controller

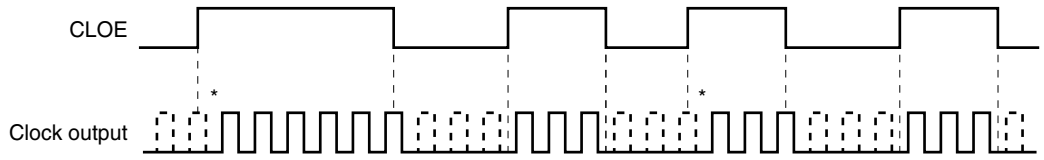
12.4.1 Operation as clock output

The clock pulse is output as the following procedure.

<1> Select the clock pulse output frequency with bits 0 to 3 (CCS0 to CCS3) of the clock output selection register (CKS) (clock pulse output in disabled status).
<2> Set bit 4 (CLOE) of CKS to 1 to enable clock output.

Remark The clock output controller is designed not to output pulses with a small width during output enable/disable switching of the clock output. As shown in Figure 12-6, be sure to start output from the low period of the clock (marked with * in the figure). When stopping output, do so after the high-level period of the clock.

Figure 12-6. Remote Control Output Application Example



12.4.2 Operation as buzzer output

The buzzer frequency is output as the following procedure.

<1> Select the buzzer output frequency with bits 5 and 6 (BCS0, BCS1) of the clock output selection register (CKS) (buzzer output in disabled status).
<2> Set bit 7 (BZOE) of CKS to 1 to enable buzzer output.

13.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$1LSB = 1/2^{10} = 1/1024$
$= 0.098\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 13-14. Overall Error

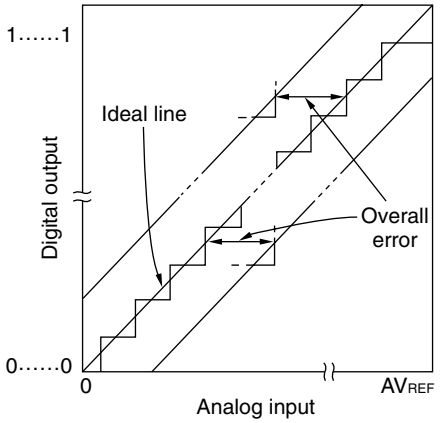
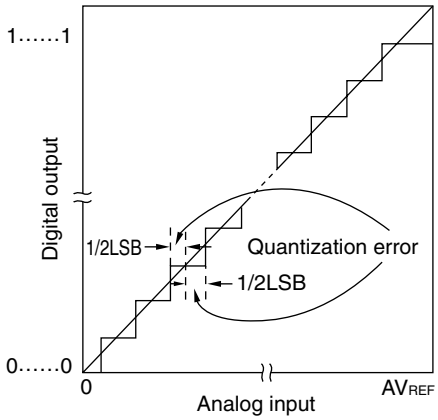


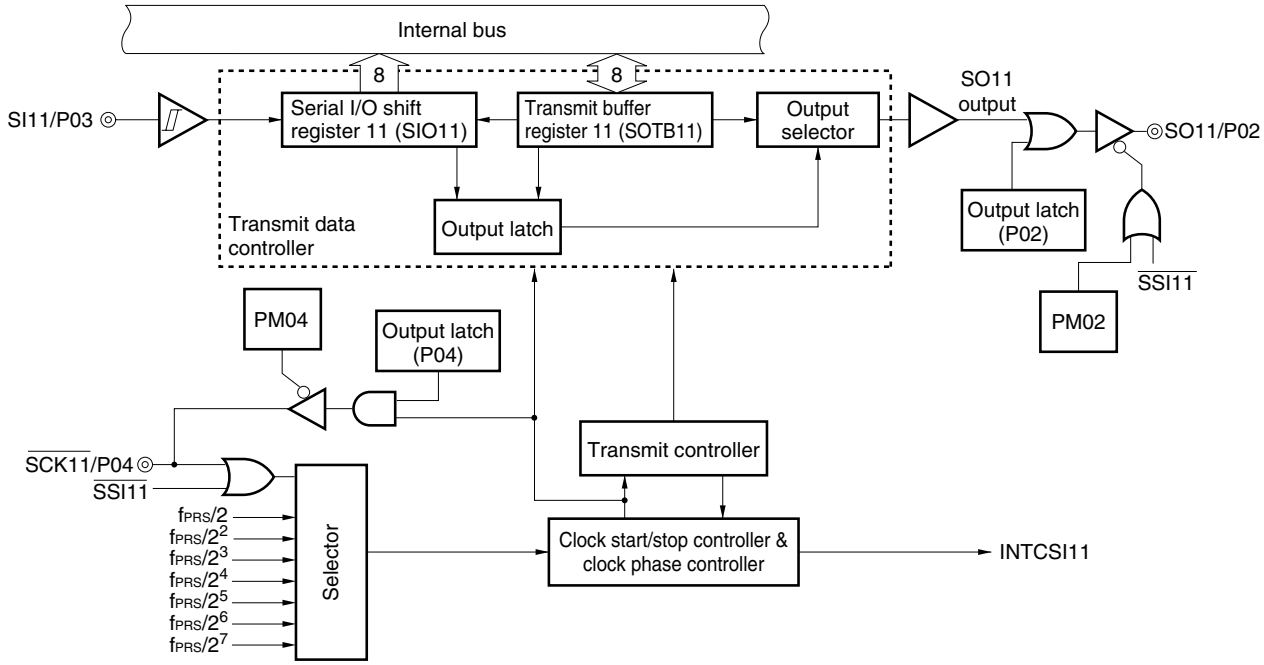
Figure 13-15. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.
If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

Figure 16-2. Block Diagram of Serial Interface CSI11



(1) Transmit buffer register 1n (SOTB1n)

This register sets the transmit data.

Transmission/reception is started by writing data to SOTB1n when bit 7 (CSIE1n) and bit 6 (TRMD1n) of serial operation mode register 1n (CSIM1n) is 1.

The data written to SOTB1n is converted from parallel data into serial data by serial I/O shift register 1n, and output to the serial output pin (SO1n).

SOTB1n can be written or read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Cautions 1. Do not access SOTB1n when CSOT1n = 1 (during serial communication).

2. In the slave mode, transmission/reception is started when data is written to SOTB11 with a low level input to the $\overline{\text{SSI11}}$ pin. For details on the transmission/reception operation, see 16.4.2 (2) Communication operation.

(2) Serial I/O shift register 1n (SIO1n)

This is an 8-bit register that converts data from parallel data into serial data and vice versa.

This register can be read by an 8-bit memory manipulation instruction.

Reception is started by reading data from SIO1n if bit 6 (TRMD1n) of serial operation mode register 1n (CSIM1n) is 0.

During reception, the data is read from the serial input pin (SI1n) to SIO1n.

Reset signal generation clears this register to 00H.

Cautions 1. Do not access SIO1n when CSOT1n = 1 (during serial communication).

2. In the slave mode, reception is started when data is read from SIO11 with a low level input to the $\overline{\text{SSI11}}$ pin. For details on the reception operation, see 16.4.2 (2) Communication operation.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(4) Divisor selection register 0 (BRGCA0)

This is an 8-bit register used to select the base clock divisor of CSIA0.

This register can be set by an 8-bit memory manipulation instruction. However, when bit 0 (TSF0) of serial status register 0 (CSIS0) is 1, rewriting BRGCA0 is prohibited.

Reset signal generation sets this register to 03H.

Figure 17-5. Format of Divisor Selection Register 0 (BRGCA0)

Address: FF93H After reset: 03H R/W

Symbol	7	6	5	4	3	2	1	0
BRGCA0	0	0	0	0	0	0	BRGCA01	BRGCA00

BRGCA01	BRGCA00	Selection of base clock (f_W) divisor of CSIA0[Note]						
			f_W = 1 MHz	f_W = 2 MHz	f_W = 2.5 MHz	f_W = 5 MHz	f_W = 10 MHz	f_W = 20 MHz
0	0	$f_W/6$	166.67 kHz	333.3 kHz	416.67 kHz	833.33 kHz	1.67 MHz	Setting prohibited
0	1	$f_W/2^3$	125 kHz	250 kHz	312.5 kHz	625 kHz	1.25 MHz	Setting prohibited
1	0	$f_W/2^4$	62.5 kHz	125 kHz	156.25 kHz	312.5 kHz	625 kHz	1.25 MHz
1	1	$f_W/2^5$	31.25 kHz	62.5 kHz	78.125 kHz	156.25 kHz	312.5 kHz	625 kHz

Note Set the transfer clock so as to satisfy the following conditions.

- When 4.0 V ≤ V_{DD} ≤ 5.5 V: transfer clock ≤ 1.67 MHz
- When 2.7 V ≤ V_{DD} < 4.0 V: transfer clock ≤ 833.33 kHz
- When 1.8 V ≤ V_{DD} < 2.7 V: transfer clock ≤ 555.56 kHz (Standard products and (A) grade products only)

Remark f_W: Base clock frequency selected by CKS00 bit of CSIS0 register (f_{PRS} or $f_{PRS}/2$)

f_{PRS}: Peripheral hardware clock frequency

(3) SO latch

The SO latch is used to retain the SDA0 pin's output level.

(4) Wake-up controller

This circuit generates an interrupt request (INTIIC0) when the address received by this register matches the address value set to slave address register 0 (SVA0) or when an extension code is received.

(5) Prescaler

This selects the sampling clock to be used.

(6) Serial clock counter

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

(7) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIIC0).

An I^2C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by WTIM0 bit)
- Interrupt request generated when a stop condition is detected (set by SPIE0 bit)

Remark WTIM0 bit: Bit 3 of IIC control register 0 (IICC0)
SPIE0 bit: Bit 4 of IIC control register 0 (IICC0)

(8) Serial clock controller

In master mode, this circuit generates the clock output via the SCL0 pin from a sampling clock.

(9) Serial clock wait controller

This circuit controls the wait timing.

(10) ACK generator, stop condition detector, start condition detector, and ACK detector

These circuits generate and detect each status.

(11) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(12) Start condition generator

This circuit generates a start condition when the STT0 bit is set to 1.

However, in the communication reservation disabled status (IICRSV bit = 1), when the bus is not released (IICBSY bit = 1), start condition requests are ignored and the STCF bit is set to 1.

(13) Stop condition generator

This circuit generates a stop condition when the SPT0 bit is set to 1.

18.5.4 Acknowledge ($\overline{\text{ACK}}$)

$\overline{\text{ACK}}$ is used to check the status of serial data at the transmission and reception sides.

The reception side returns $\overline{\text{ACK}}$ each time it has received 8-bit data.

The transmission side usually receives $\overline{\text{ACK}}$ after transmitting 8-bit data. When $\overline{\text{ACK}}$ is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether $\overline{\text{ACK}}$ has been detected can be checked by using bit 2 (ACKD0) of IIC status register 0 (IICS0).

When the master receives the last data item, it does not return $\overline{\text{ACK}}$ and instead generates a stop condition. If a slave does not return $\overline{\text{ACK}}$ after receiving data, the master outputs a stop condition or restart condition and stops transmission. If $\overline{\text{ACK}}$ is not returned, the possible causes are as follows.

<1> Reception was not performed normally.
<2> The final data item was received.
<3> The reception side specified by the address does not exist.

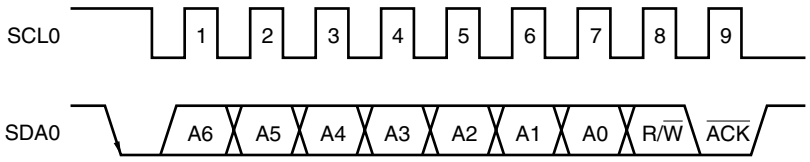
To generate $\overline{\text{ACK}}$, the reception side makes the SDA0 line low at the ninth clock (indicating normal reception).

Automatic generation of $\overline{\text{ACK}}$ is enabled by setting bit 2 (ACKE0) of IIC control register 0 (IICC0) to 1. Bit 3 (TRC0) of the IICS0 register is set by the data of the eighth bit that follows 7-bit address information. Usually, set ACKE0 bit to 1 for reception (TRC0 = 0).

If a slave can receive no more data during reception (TRC0 = 0) or does not require the next data item, then the slave must inform the master, by clearing ACKE0 bit to 0, that it will not receive any more data.

When the master does not require the next data item during reception (TRC0 = 0), it must clear ACKE0 bit to 0 so that $\overline{\text{ACK}}$ is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

Figure 18-16. $\overline{\text{ACK}}$



When the local address is received, $\overline{\text{ACK}}$ is automatically generated, regardless of the value of ACKE0 bit. When an address other than that of the local address is received, $\overline{\text{ACK}}$ is not generated (NACK).

When an extension code is received, $\overline{\text{ACK}}$ is generated if ACKE0 bit is set to 1 in advance.

How $\overline{\text{ACK}}$ is generated when data is received differs as follows depending on the setting of the wait timing.

- When 8-clock wait state is selected (bit 3 (WTIM0) of IICC0 register = 0):
  By setting ACKE0 bit to 1 before releasing the wait state, $\overline{\text{ACK}}$ is generated at the falling edge of the eighth clock of the SCL0 pin.
- When 9-clock wait state is selected (bit 3 (WTIM0) of IICC0 register = 1):
  $\overline{\text{ACK}}$ is generated by setting ACKE0 bit to 1 in advance.

(3) 0084H/1084H

○ On-chip debug operation control

- Disabling on-chip debug operation
- Enabling on-chip debug operation and erasing data of the flash memory in case authentication of the on-chip debug security ID fails
- Enabling on-chip debug operation and not erasing data of the flash memory even in case authentication of the on-chip debug security ID fails

Cautions 1. Be sure to set 00H (disabling on-chip debug operation) to 0084H for products not equipped with the on-chip debug function (μPD78F05xx and 78F05xxA). Also set 00H to 1084H because 0084H and 1084H are switched during the boot operation.

2. To use the on-chip debug function with a product equipped with the on-chip debug function (μPD78F05xxD and 78F05xxDA), set 02H or 03H to 0084H. Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot operation.

26.2 Format of Option Byte

The format of the option byte is shown below.

Figure 26-1. Format of Option Byte (2/2)

Address: 0081H/1081H[Notes 1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	POCMODE

POCMODE	POC mode selection
0	1.59 V POC mode (default)
1	2.7 V/1.59 V POC mode

Notes 1. POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

2. To change the setting for the POC mode, set the value to 0081H again after batch erasure (chip erasure) of the flash memory. The setting cannot be changed after the memory of the specified block is erased.

Caution Be sure to clear bits 7 to 1 to "0".

Address: 0082H/1082H, 0083H/1083H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Note Be sure to set 00H to 0082H and 0083H, as these addresses are reserved areas. Also set 00H to 1082H and 1083H because 0082H and 0083H are switched with 1082H and 1083H when the boot swap operation is used.

Address: 0084H/1084H[Notes1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	OCDEN1	OCDEN0

OCDEN1	OCDEN0	On-chip debug operation control
0	0	Operation disabled
0	1	Setting prohibited
1	0	Operation enabled. Does not erase data of the flash memory in case authentication of the on-chip debug security ID fails.
1	1	Operation enabled. Erases data of the flash memory in case authentication of the on-chip debug security ID fails.

Notes 1. Be sure to set 00H (on-chip debug operation disabled) to 0084H for products not equipped with the on-chip debug function (μPD78F05xx and 78F05xxA). Also set 00H to 1084H because 0084H and 1084H are switched during the boot swap operation.

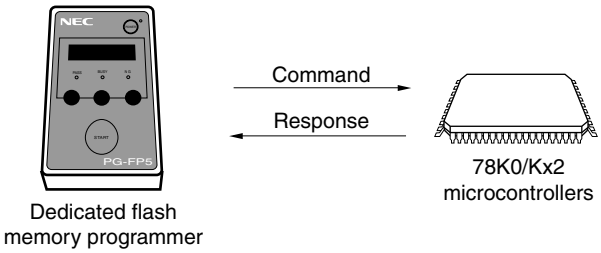
2. To use the on-chip debug function with a product equipped with the on-chip debug function (μPD78F05xxD and 78F05xxDA), set 02H or 03H to 0084H. Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot swap operation.

Remark For the on-chip debug security ID, see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD and 78F05xxDA ONLY)**.

27.7.4 Communication commands

The 78K0/Kx2 microcontrollers communicate with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0/Kx2 microcontrollers are called commands, and the signals sent from the 78K0/Kx2 microcontrollers to the dedicated flash memory programmer are called response.

Figure 27-12. Communication Commands



The flash memory control commands of the 78K0/Kx2 microcontrollers are listed in the table below. All these commands are issued from the programmer and the 78K0/Kx2 microcontrollers perform processing corresponding to the respective commands.

Table 27-8. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Chip Erase	Erases the entire flash memory.
	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Status	Gets the current operating status (status data).
	Silicon Signature	Gets 78K0/Kx2 information (such as the part number and flash memory configuration).
	Version Get	Gets the 78K0/Kx2 version and firmware version.
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
Others	Reset	Used to detect synchronization status of communication.
	Oscillating Frequency Set	Specifies an oscillation frequency.

The 78K0/Kx2 microcontrollers return a response for the command issued by the dedicated flash memory programmer. The response names sent from the 78K0/Kx2 microcontrollers are listed below.

Table 27-9. Response Names

Response Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

Table 27-14. Processing Time for Self Programming Library
(Expanded-specification Products (μPD78F05xxA and 78F05xxDA)) (1/3)

(1) When internal high-speed oscillation clock is used and entry RAM is located outside short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		4.0	4.5	4.0	4.5
Initialize library		1105.9	1106.6	1105.9	1106.6
Mode check library		905.7	906.1	904.9	905.3
Block blank check library		12776.1	12778.3	12770.9	12772.6
Block erase library		26050.4	349971.3	26045.3	349965.6
Word write library		1180.1 + 203 × w	1184.3 + 2241 × w	1172.9 + 203 × w	1176.3 + 2241 × w
Block verify library		25337.9	25340.2	25332.8	25334.5
Self programming end library		4.0	4.5	4.0	4.5
Get information library	Option value: 03H	1072.9	1075.2	1067.5	1069.1
	Option value: 04H	1060.2	1062.6	1054.8	1056.6
	Option value: 05H	1023.8	1028.2	1018.3	1022.1
Set information library		70265.9	759995.0	70264.9	759994.0
EEPROM write library		1316.8 + 347 × w	1320.9 + 2385 × w	1309.0 + 347 × w	1312.4 + 2385 × w

(2) When internal high-speed oscillation clock is used and entry RAM is located in short direct addressing range

Library Name		Processing Time (μs)			
		Normal Model of C Compiler		Static Model of C Compiler/Assembler	
		Min.	Max.	Min.	Max.
Self programming start library		4.0	4.5	4.0	4.5
Initialize library		449.5	450.2	449.5	450.2
Mode check library		249.3	249.7	248.6	248.9
Block blank check library		12119.7	12121.9	12114.6	12116.3
Block erase library		25344.7	349266.4	25339.6	349260.8
Word write library		445.8 + 203 × w	449.9 + 2241 × w	438.5 + 203 × w	441.9 + 2241 × w
Block verify library		24682.7	24684.9	24677.6	24679.3
Self programming end library		4.0	4.5	4.0	4.5
Get information library	Option value: 03H	417.6	419.8	412.1	413.8
	Option value: 04H	405.0	407.4	399.5	401.3
	Option value: 05H	367.4	371.8	361.9	365.8
Set information library		69569.3	759297.3	69568.3	759296.2
EEPROM write library		795.1 + 347 × w	799.3 + 2385 × w	787.4 + 347 × w	790.8 + 2385 × w

Remarks 1. The above processing times are those when a write start address structure is located in the internal high-speed RAM and during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

3. w: Number of words in write data (1 word = 4 bytes)

Table 27-15. Interrupt Response Time for Self Programming Library (Conventional-specification Products (μPD78F05xx and 78F05xxD)) (1/2)

(1) When internal high-speed oscillation clock is used

Library Name	Interrupt Response Time (μs (Max.))			
	Normal Model of C Compiler		Static Model of C Compiler/Assembler	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	933.6	668.6	927.9	662.9
Block erase library	1026.6	763.6	1020.9	757.9
Word write library	2505.8	1942.8	2497.8	1934.8
Block verify library	958.6	693.6	952.9	687.9
Set information library	476.5	211.5	475.5	210.5
EEPROM write library	2760.8	2168.8	2759.5	2167.5

Remarks 1. The above interrupt response times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

(2) When high-speed system clock is used (normal model of C compiler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	179/f_{CPU} + 507	179/f_{CPU} + 407	179/f_{CPU} + 1650	179/f_{CPU} + 714
Block erase library	179/f_{CPU} + 559	179/f_{CPU} + 460	179/f_{CPU} + 1702	179/f_{CPU} + 767
Word write library	333/f_{CPU} + 1589	333/f_{CPU} + 1298	333/f_{CPU} + 2732	333/f_{CPU} + 1605
Block verify library	179/f_{CPU} + 518	179/f_{CPU} + 418	179/f_{CPU} + 1661	179/f_{CPU} + 725
Set information library	80/f_{CPU} + 370	80/f_{CPU} + 165	80/f_{CPU} + 1513	80/f_{CPU} + 472
EEPROM write library[Note]	29/f_{CPU} + 1759	29/f_{CPU} + 1468	29/f_{CPU} + 1759	29/f_{CPU} + 1468
	333/f_{CPU} + 834	333/f_{CPU} + 512	333/f_{CPU} + 2061	333/f_{CPU} + 873

Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

AC Characteristics

(1) Basic operation (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	Conventional-specification Products (μPD78F05xx (A))	4.0 V ≤ V_{DD} ≤ 5.5 V	0.1		32	μs
				2.7 V ≤ V_{DD} < 4.0 V	0.2		32	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.4 Note 1		32	μs
			Expanded-specification Products (μPD78F05xxA (A))	2.7 V ≤ V_{DD} ≤ 5.5 V	0.1		32	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.4 Note 1		32	μs
		Subsystem clock (f_{SUB}) operation Note 2			114	122	125	μs
Peripheral hardware clock frequency	f_{PRS}	f_{PRS} = f_{XH} (XSEL = 1)	Conventional-specification Products (μPD78F05xx (A))	4.0 V ≤ V_{DD} ≤ 5.5 V			20	MHz
				2.7 V ≤ V_{DD} < 4.0 V			10	MHz
				1.8 V ≤ V_{DD} < 2.7 V			5	MHz
			Expanded-specification Products (μPD78F05xxA (A))	4.0 V ≤ V_{DD} ≤ 5.5 V			20	MHz
				2.7 V ≤ V_{DD} < 4.0 V Note 3			20	MHz
				1.8 V ≤ V_{DD} < 2.7 V			5	MHz
		f_{PRS} = f_{RH} (XSEL = 0)		2.7 V ≤ V_{DD} ≤ 5.5 V	7.6		8.4	MHz
				1.8 V ≤ V_{DD} < 2.7 V Note 4	7.6		10.4	MHz
External main system clock frequency	f_{EXCLK}	Conventional-specification Products (μPD78F05xx(A))		4.0 V ≤ V_{DD} ≤ 5.5 V	1.0 Note 5		20.0	MHz
				2.7 V ≤ V_{DD} < 4.0 V	1.0 Note 5		10.0	MHz
				1.8 V ≤ V_{DD} < 2.7 V	1.0		5.0	MHz
		Expanded-specification Products (μPD78F05xxA(A))		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0 Note 5		20.0	MHz
				1.8 V ≤ V_{DD} < 2.7 V	1.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXCLKH}, t_{EXCLKL}	Conventional-specification Products (μPD78F05xx(A))		4.0 V ≤ V_{DD} ≤ 5.5 V	24			ns
				2.7 V ≤ V_{DD} < 4.0 V	48			ns
				1.8 V ≤ V_{DD} < 2.7 V	96			ns
		Expanded-specification Products (μPD78F05xxA(A))		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns
				1.8 V ≤ V_{DD} < 2.7 V	96			ns

Notes 1. 0.38 μs when operating with the 8 MHz internal oscillator.

2. The 78K0/KB2 is not provided with a subsystem clock.

3. Characteristics of the main system clock frequency. Set the division clock to be set by a peripheral function to f_{XH}/2 (10 MHz) or less. The multiplier/divider, however, can operate on f_{XH} (20 MHz).

4. Characteristics of the main system clock frequency. Set the division clock to be set by a peripheral function to f_{RH}/2 or less.

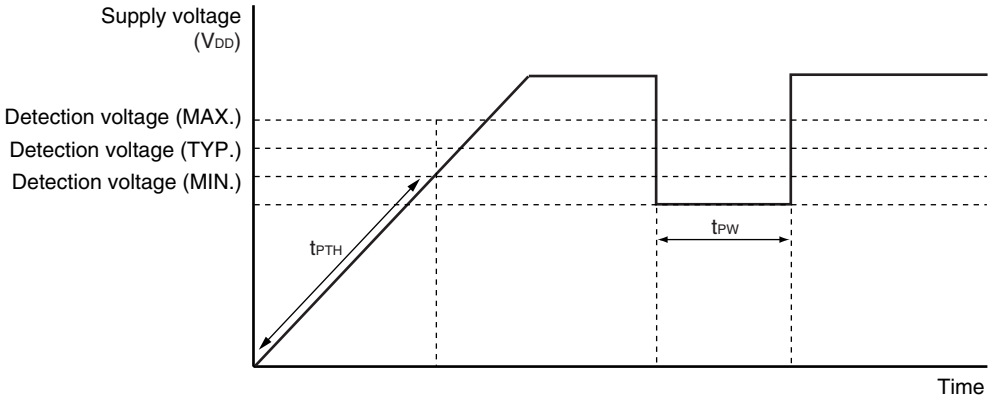
5. 2.0 MHz (MIN.) when using UART6 during on-board programming.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

1.59 V POC Circuit Characteristics (T_A = –40 to +125°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		1.44	1.59	1.74	V
Power supply voltage rise inclination	t_{PTH}	V_{DD}: 0 V → change inclination of V_{POC}	0.5			V/ms
Minimum pulse width	t_{PW}		200			μs

1.59 V POC Circuit Timing



(18/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 15	Soft	Serial interface UART6	ASICL6: Asynchronous serial interface control register 6	The read value of the SBRT6 bit is always 0. SBRT6 is automatically cleared to 0 after SBF reception has been correctly completed.	p. 467 ☐
				Before setting the SBTT6 bit to 1, make sure that bit 7 (POWER6) and bit 6 (TXE6) of ASIM6 = 1. After setting the SBTT6 bit to 1, do not clear it to 0 before SBF transmission is completed (before an interrupt request signal is generated).	p. 467 ☐
				The read value of the SBTT6 bit is always 0. SBTT6 is automatically cleared to 0 at the end of SBF transmission	p. 467 ☐
				Do not set the SBRT6 bit to 1 during reception, and do not set the SBTT6 bit to 1 during transmission.	p. 467 ☐
				When the TXDLV6 bit is set to 1 (inverted TxD6 output), the TxD6/SCLA0/P60 pin cannot be used as a general-purpose port, regardless of the settings of POWER6 and TXE6. When using the TxD6/SCLA0/P60 pin as a general-purpose port, clear the TXDLV6 bit to 0 (normal TxD6 output).	p. 467 ☐
				Before rewriting the DIR6 and TXDLV6 bits, clear the TXE6 and RXE6 bits to 0.	p. 467 ☐
			POWER6, TXE6, RXE6: Bits 7, 6, 5 of ASIM6	Clear POWER6 to 0 after clearing TXE6 and RXE6 to 0 to stop the operation. To start the communication, set POWER6 to 1, and then set TXE6 or RXE6 to 1.	p. 469 ☐
			UART mode	Take relationship with the other party of communication when setting the port mode register and port register.	p. 470 ☐
			Parity types and operation	Fix the PS61 and PS60 bits to 0 when the device is used in LIN communication operation.	p. 473 ☐
			Continuous transmission	The TXBF6 and TXSF6 flags of the ASIF6 register change from “10” to “11”, and to “01” during continuous transmission. To check the status, therefore, do not use a combination of the TXBF6 and TXSF6 flags for judgment. Read only the TXBF6 flag when executing continuous transmission.	p. 475 ☐
				When the device is use in LIN communication operation, the continuous transmission function cannot be used. Make sure that asynchronous serial interface transmission status register 6 (ASIF6) is 00H before writing transmit data to transmit buffer register 6 (TXB6).	p. 475 ☐
				To transmit data continuously, write the first transmit data (first byte) to the TXB6 register. Be sure to check that the TXBF6 flag is “0”. If so, write the next transmit data (second byte) to the TXB6 register. If data is written to the TXB6 register while the TXBF6 flag is “1”, the transmit data cannot be guaranteed.	p. 475 ☐
				To initialize the transmission unit upon completion of continuous transmission, be sure to check that the TXSF6 flag is “0” after generation of the transmission completion interrupt, and then execute initialization. If initialization is executed while the TXSF6 flag is “1”, the transmit data cannot be guaranteed.	p. 475 ☐
				During continuous transmission, the next transmission may complete before execution of INTST6 interrupt servicing after transmission of one data frame. As a countermeasure, detection can be performed by developing a program that can count the number of transmit data and by referencing the TXSF6 flag.	p. 475 ☐
			Normal reception	If a reception error occurs, read ASIS6 and then RXB6 to clear the error flag. Otherwise, an overrun error will occur when the next data is received, and the reception error status will persist.	p. 479 ☐
				Reception is always performed with the “number of stop bits = 1”. The second stop bit is ignored.	p. 479 ☐
				Be sure to read asynchronous serial interface reception error status register 6 (ASIS6) before reading RXB6.	p. 479 ☐
			Error of baud rate	Keep the baud rate error during transmission to within the permissible error range at the reception destination.	p. 486 ☐
				Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.	p. 486 ☐
			Permissible baud rate range during reception	Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.	p. 487 ☐