Renesas Electronics America Inc - UPD78F0536AGB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0536agb-gah-ax

1.1.1 A/D conversion time

(1) Conventional-specification products (μPD78F05xx and 78F05xxD)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1	36.7	μs
		2.7 V ≤ AV_{REF} < 4.0 V	12.2	36.7	μs
		2.3 V ≤ AV_{REF} < 2.7 V Note	27	66.6	μs

(2) Expanded-specification products (μPD78F05xxA and 78F05xxDA)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1	66.6	μs
		2.7 V ≤ AV_{REF} < 4.0 V	12.2	66.6	μs
		2.3 V ≤ AV_{REF} < 2.7 V Note	27	66.6	μs

Note Standard and (A) grade products only

1.1.2 X1 oscillator characteristics

(1) Conventional-specification products (μPD78F05xx and 78F05xxD)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	X1 clock oscillation frequency (f_X)	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0 Note 2		20.0	MHz
		2.7 V ≤ V_{DD} < 4.0 V	1.0 Note 2		10.0	
		1.8 V ≤ V_{DD} < 2.7 V Note 1	1.0		5.0	

(2) Expanded-specification products (μPD78F05xxA and 78F05xxDA)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	X1 clock oscillation frequency (f_X)	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0 Note 2		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V Note 1	1.0		5.0	

Notes 1. Standard and (A) grade products only

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

1.2 Features

- Minimum instruction execution time can be changed from high speed (0.1 μs: @ 20 MHz operation with high-speed system clock) to ultra low-speed (122 μs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM (flash memory), RAM capacities

ROM[Note]	High-Speed RAM[Note]	Expansion RAM[Note]	78K0/KB2	78K0/KC2		78K0/KD2	78K0/KE2	78K0/KF2
			30/36 pins	38/44 pins	48 pins	52 pins	64 pins	80 pins
128 KB	1 KB	6 KB	–	–	–	μPD78F0527D, 78F0527DA	μPD78F0537D, 78F0537DA	μPD78F0547D, 78F0547DA
						μPD78F0527, 78F0527A	μPD78F0537, 78F0537A	μPD78F0547 78F0547A
96 KB	1 KB	4 KB	–	–	–	μPD78F0526, 78F0526A	μPD78F0536, 78F0536A	μPD78F0546, 78F0546A
60 KB	1 KB	2 KB	–	–	μPD78F0515D, 78F0515DA	μPD78F0525, 78F0525A	μPD78F0535, 78F0535A	μPD78F0545, 78F0545A
					μPD78F0515, 78F0515A			
48 KB	1 KB	1 KB	–	–	μPD78F0514, 78F0514A	μPD78F0524, 78F0524A	μPD78F0534, 78F0534A	μPD78F0544, 78F0544A
32 KB	1 KB	–	μPD78F0503D, 78F0503DA	μPD78F0513D, 78F0513DA	μPD78F0513, 78F0513A	μPD78F0523, 78F0523A	μPD78F0533, 78F0533A	–
			μPD78F0503, 78F0503A	μPD78F0513, 78F0513A				
24 KB	1 KB	–	μPD78F0502, 78F0502A	μPD78F0512, 78F0512A	μPD78F0512, 78F0512A	μPD78F0522, 78F0522A	μPD78F0532, 78F0532A	–
16 KB	768 B	–	μPD78F0501, 78F0501A	μPD78F0511, 78F0511A	μPD78F0511, 78F0511A	μPD78F0521, 78F0521A	μPD78F0531, 78F0531A	–
8 KB	512 B	–	μPD78F0500, 78F0500A	–	–	–	–	–

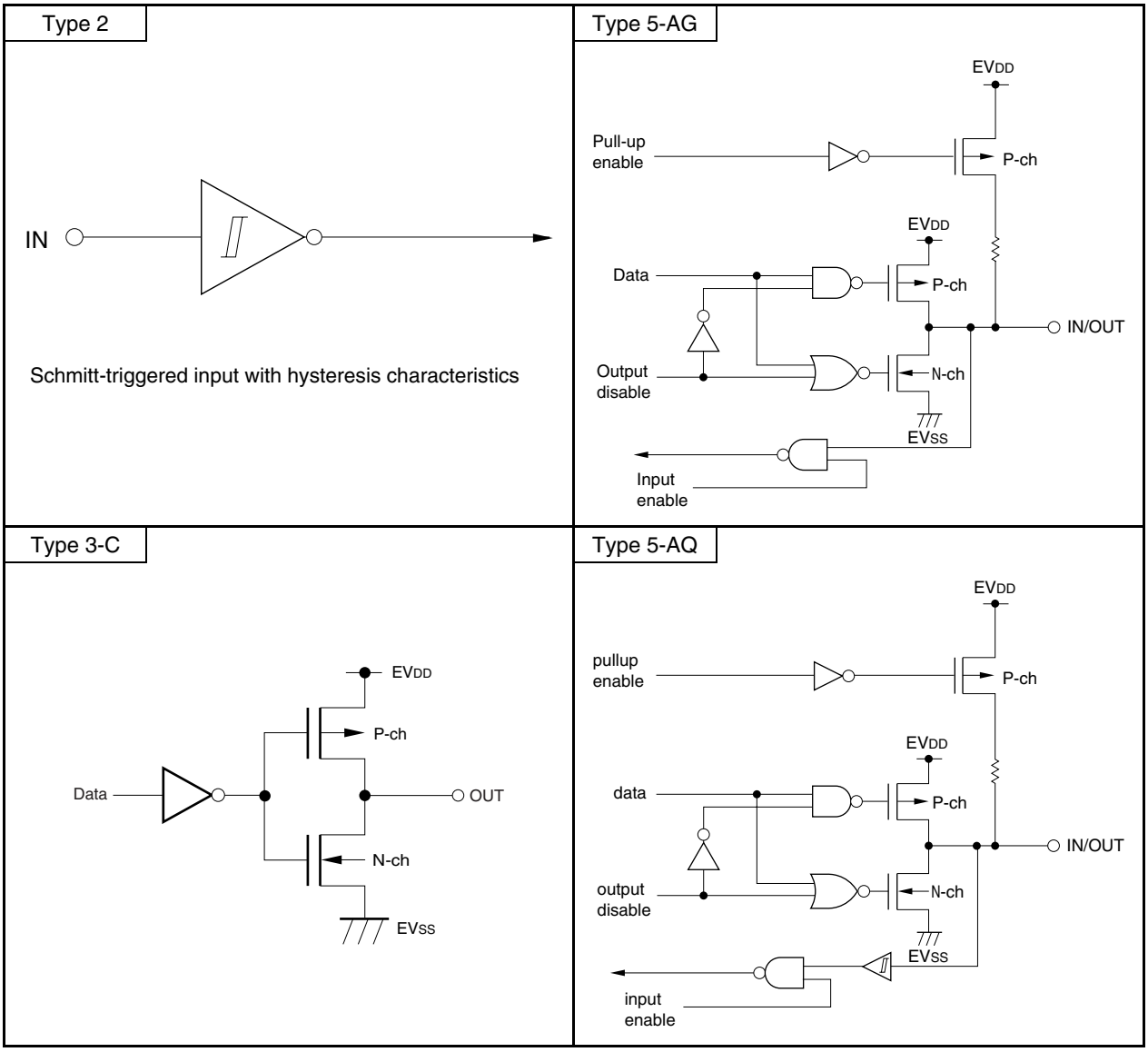
Note The internal flash memory, internal high-speed RAM capacities, and internal expansion RAM capacities can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS). For IMS and IXS, see **27.1 Internal Memory Size Switching Register** and **27.2 Internal Expansion RAM Size Switching Register**.

- Buffer RAM: 32 bytes (can be used for transfer in CSI with automatic transmit/receive function) (78K0/KF2 only)
- On-chip single-power-supply flash memory
- Self-programming (with boot swap function)
- On-chip debug function (μPD78F05xxD and 78F05xxDA only)[Note]

Note The μPD78F05xxD and 78F05xxDA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

- On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
- On-chip watchdog timer (operable with the on-chip internal low-speed oscillation clock)

Figure 2-1. Pin I/O Circuit List (1/2)



Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

3.4.6 Register indirect addressing

[Function]

Register pair contents specified by a register pair specify code in an instruction word and by a register bank select flag (RBS0 and RBS1) serve as an operand address for addressing the memory.

This addressing can be carried out for all of the memory spaces. However, before addressing a memory bank that is not set by the memory bank select register (BANK), change the setting of the memory bank by using BANK.

[Operand format]

Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; when selecting [DE] as register pair

Operation code	1	0	0	0	0	1	0	1

[Illustration]

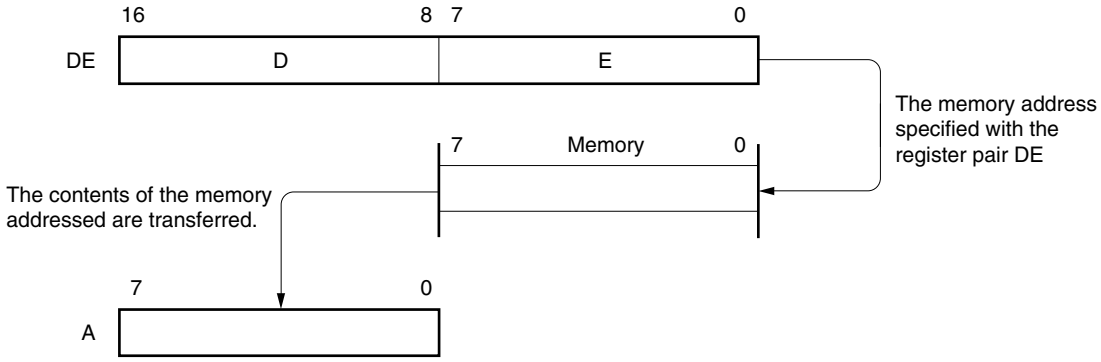


Figure 5-36. Format of Port Register (78K0/KD2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	0	0	0	P03	P02	P01	P00	FF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P3	0	0	0	0	P33	P32	P31	P30	FF03H	00H (output latch)	R/W
P4	0	0	0	0	0	0	P41	P40	FF04H	00H (output latch)	R/W
P6	0	0	0	0	P63	P62	P61	P60	FF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FF07H	00H (output latch)	R/W
P12	0	0	0	P124Note	P123Note	P122Note	P121Note	P120	FF0CH	00H (output latch)	R/W
P13	0	0	0	0	0	0	0	P130	FF0DH	00H (output latch)	R/W
P14	0	0	0	0	0	0	0	P140	FF0EH	00H (output latch)	R/W

Pmn	m = 0 to 4, 6, 7, 12 to 14; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note “0” is always read from the output latch of P121 to P124 if the pin is in the external clock input mode.

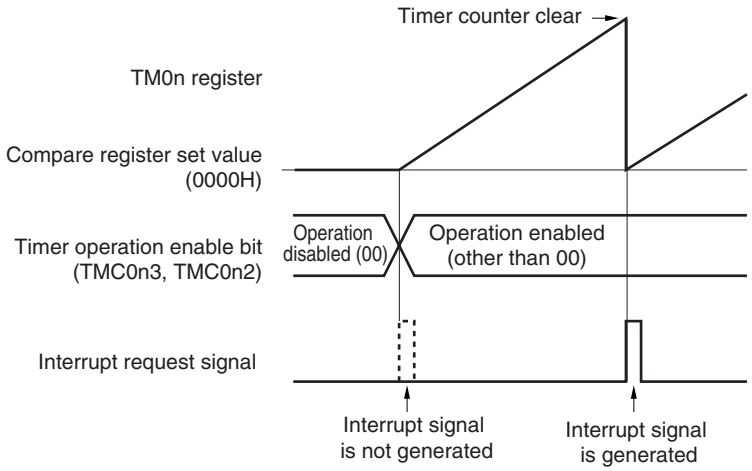
(iii) Setting range when CR00n or CR01n is used as a compare register

When CR00n or CR01n is used as a compare register, set it as shown below.

Operation	CR00n Register Setting Range	CR01n Register Setting Range
Operation as interval timer	0000H < N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH Normally, this setting is not used. Mask the match interrupt signal (INTTM01n).
Operation as square-wave output		
Operation as external event counter		
Operation in the clear & start mode entered by TI00n pin valid edge input	0000H[Note] ≤ N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH
Operation as free-running timer		
Operation as PPG output	M < N ≤ FFFFH	0000H[Note] ≤ M < N
Operation as one-shot pulse output	0000H[Note] ≤ N ≤ FFFFH (N ≠ M)	0000H[Note] ≤ M ≤ FFFFH (M ≠ N)

Note When 0000H is set, a match interrupt immediately after the timer operation does not occur and timer output is not changed, and the first match timing is as follows. A match interrupt occurs at the timing when the timer counter (TM0n register) is changed from 0000H to 0001H.

- When the timer counter is cleared due to overflow
- When the timer counter is cleared due to TI00n pin valid edge (when clear & start mode is entered by TI00n pin valid edge input)
- When the timer counter is cleared due to compare match (when clear & start mode is entered by match between TM0n and CR00n (CR00n = other than 0000H, CR01n = 0000H))



Remarks 1. N: CR00n register set value, M: CR01n register set value

2. For details of TMC0n3 and TMC0n2, see **7.3 (1) 16-bit timer mode control register 0n (TMC0n)**.

3. n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(2) Capture/compare control register 0n (CRC0n)

CRC0n is the register that controls the operation of CR00n and CR01n.

Changing the value of CRC0n is prohibited during operation (when TMC0n3 and TMC0n2 = other than 00).

CRC0n can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CRC0n to 00H.

Figure 7-8. Format of Capture/Compare Control Register 00 (CRC00)

Address: FFBCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	CRC001	CRC000

CRC002	CR010 operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC001	CR000 capture trigger selection
0	Captures on valid edge of TI010 pin
1	Captures on valid edge of TI000 pin by reverse phase[Note]
The valid edge of the TI010 and TI000 pin is set by PRM00. If ES001 and ES000 are set to 11 (both edges) when CRC001 is 1, the valid edge of the TI000 pin cannot be detected.	

CRC000	CR000 operating mode selection
0	Operates as compare register
1	Operates as capture register
If TMC003 and TMC002 are set to 11 (clear & start mode entered upon a match between TM00 and CR000), be sure to set CRC000 to 0.	

Note When the valid edge is detected from the TI010 pin, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal.

Caution To ensure that the capture operation is performed properly, the capture trigger requires a pulse two cycles longer than the count clock selected by prescaler mode register 00 (PRM00).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-25. Example of Register Settings in External Event Counter Mode (2/2)

(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

If M is set to CR00n, the interrupt signal (INTTM00n) is generated when the number of external events reaches (M + 1).

Setting CR00n to 0000H is prohibited.

(g) 16-bit capture/compare register 01n (CR01n)

Usually, CR01n is not used in the external event counter mode. However, a compare match interrupt (INTTM01n) is generated when the set value of CR01n matches the value of TM0n.

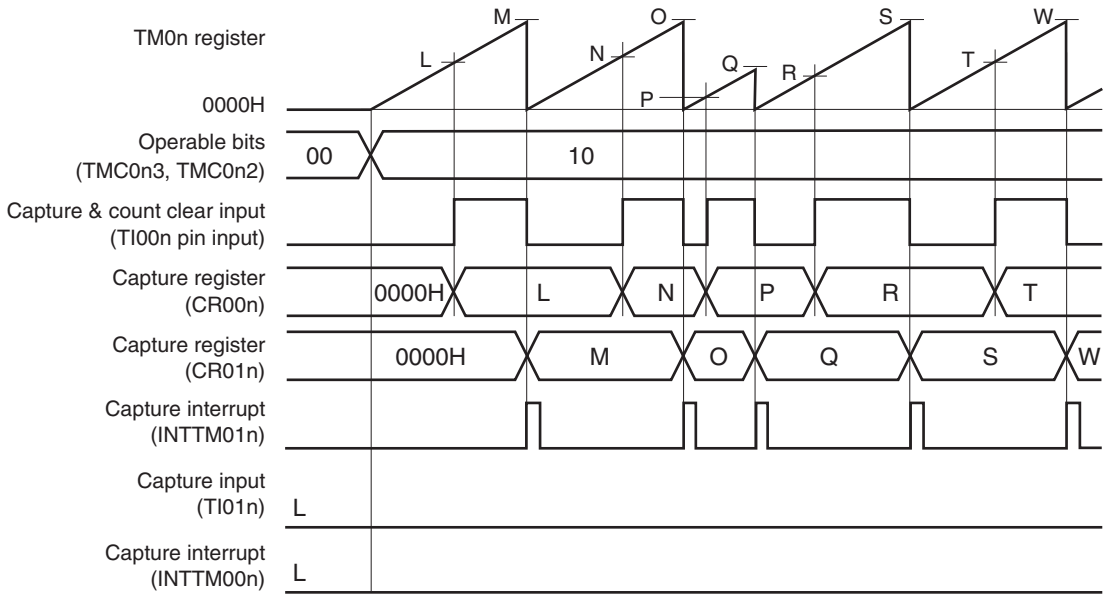
Therefore, mask the interrupt request by using the interrupt mask flag (TMMK01n).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-34. Timing Example of Clear & Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register, CR01n: Capture Register) (3/3)

(c) TOC0n = 13H, PRM0n = 00H, CRC0n = 07H, TMC0n = 0AH



This is an application example where the pulse width of the signal input to the TI00n pin is measured.
By setting CRC0n, the count value can be captured to CR00n in the phase reverse to the falling edge of the TI00n pin (i.e., rising edge) and to CR01n at the falling edge of the TI00n pin.
The high- and low-level widths of the input pulse can be calculated by the following expressions.

- High-level width = [CR01n value] – [CR00n value] × [Count clock cycle]
- Low-level width = [CR00n value] × [Count clock cycle]

If the reverse phase of the TI00n pin is selected as a trigger to capture the count value to CR00n, the INTTM00n signal is not generated. Read the values of CR00n and CR01n to measure the pulse width immediately after the INTTM01n signal is generated.
However, if the valid edge specified by bits 6 and 5 (ES1n1 and ES1n0) of prescaler mode register 0n (PRM0n) is input to the TI01n pin, the count value is not captured but the INTTM00n signal is generated. To measure the pulse width of the TI00n pin, mask the INTTM00n signal when it is not used.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

<10> By performing the procedures above, an arbitrary carrier clock is obtained. To stop the count operation, clear TMHE1 to 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the carrier clock output cycle and duty are as follows.

- Carrier clock output cycle = (N + M + 2)/f_{CNT}
- Duty = High-level width/carrier clock output width = (M + 1)/(N + M + 2)

Cautions 1. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

2. Set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

3. Set the values of the CMP01 and CMP11 registers in a range of 01H to FFH.

4. The set value of the CMP11 register can be changed while the timer counter is operating. However, it takes the duration of three operating clocks (signal selected by the CKS12 to CKS10 bits of the TMHMD1 register) since the value of the CMP11 register has been changed until the value is transferred to the register.

5. Be sure to set the RMC1 bit before the count operation is started.

Remarks 1. For the setting of the output pin, see **9.3 (3) Port mode register 1 (PM1)**.

2. For how to enable the INTTMH1 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

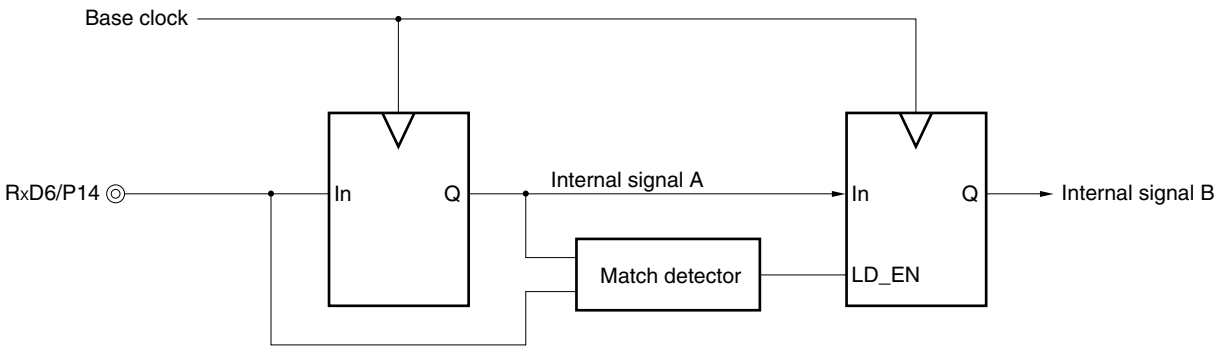
(g) Noise filter of receive data

The RxD6 signal is sampled with the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 15-21, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 15-21. Noise Filter Circuit



(h) SBF transmission

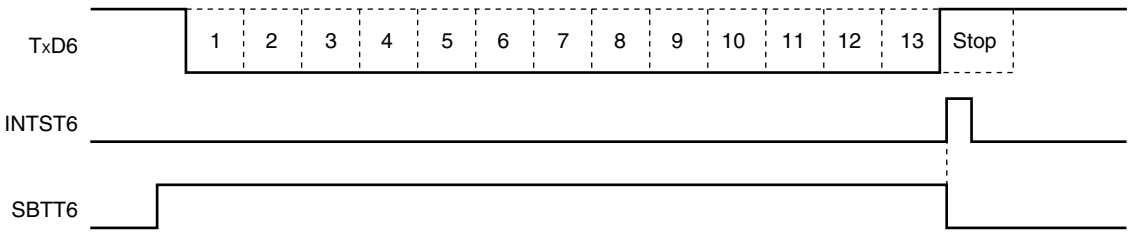
When the device is use in LIN communication operation, the SBF (Synchronous Break Field) transmission control function is used for transmission. For the transmission operation of LIN, see **Figure 15-1 LIN Transmission Operation**.

When bit 7 (POWER6) of asynchronous serial interface mode register 6 (ASIM6) is set to 1, the TxD6 pin outputs high level. Next, when bit 6 (TXE6) of ASIM6 is set to 1, the transmission enabled status is entered, and SBF transmission is started by setting bit 5 (SBTT6) of asynchronous serial interface control register 6 (ASICL6) to 1.

Thereafter, a low level of bits 13 to 20 (set by bits 4 to 2 (SBL62 to SBL60) of ASICL6) is output. Following the end of SBF transmission, the transmission completion interrupt request (INTST6) is generated and SBTT6 is automatically cleared. Thereafter, the normal transmission mode is restored.

Transmission is suspended until the data to be transmitted next is written to transmit buffer register 6 (TXB6), or until SBTT6 is set to 1.

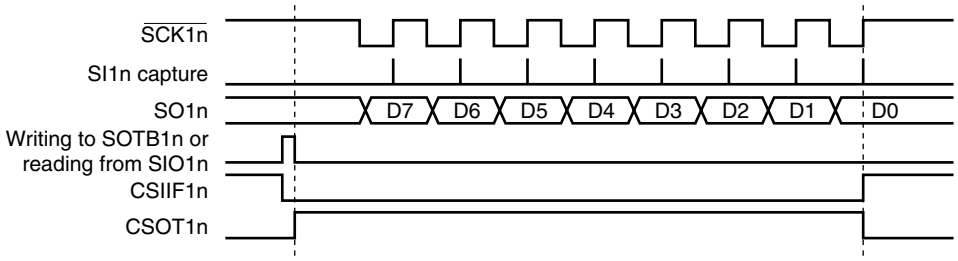
Figure 15-22. SBF Transmission



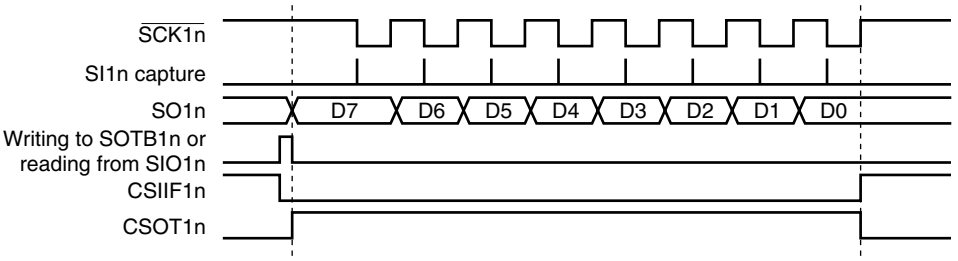
Remark TxD6: TxD6 pin (output)
INTST6: Transmission completion interrupt request
SBTT6: Bit 5 of asynchronous serial interface control register 6 (ASICL6)

Figure 16-10. Timing of Clock/Data Phase

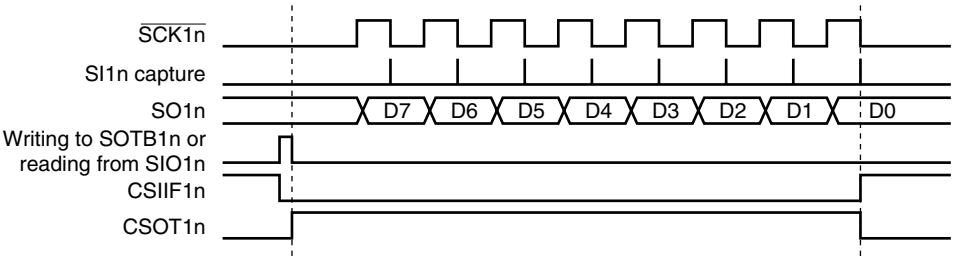
(a) Type 1: CKP1n = 0, DAP1n = 0, DIR1n = 0



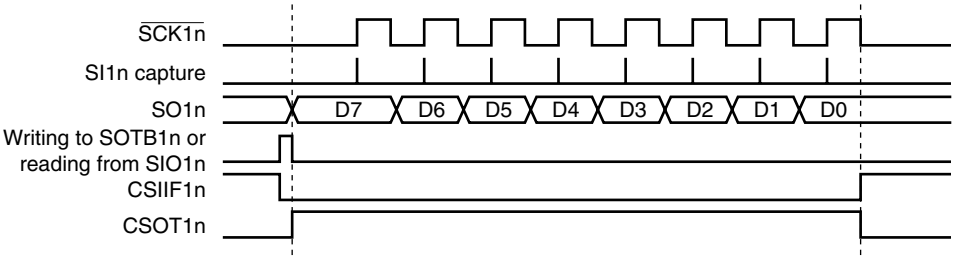
(b) Type 2: CKP1n = 0, DAP1n = 1, DIR1n = 0



(c) Type 3: CKP1n = 1, DAP1n = 0, DIR1n = 0



(d) Type 4: CKP1n = 1, DAP1n = 1, DIR1n = 0



Remarks 1. n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

2. The above figure illustrates a communication operation where data is transmitted with the MSB first.

(1) Serial I/O shift register 0 (SIOA0)

This is an 8-bit register used to store transmit/receive data in 1-byte transfer mode (bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) = 0). Writing transmit data to SIOA0 starts the communication. In addition, after a communication completion interrupt request (INTACSI) is output (bit 0 (TSF0) of serial status register 0 (CSIS0) = 0), data can be received by reading data from SIOA0.

This register can be written or read by an 8-bit memory manipulation instruction. However, writing to SIOA0 is prohibited when bit 0 (TSF0) of serial status register 0 (CSIS0) = 1.

Reset signal generation clears this register to 00H.

Cautions 1. A communication operation is started by writing to SIOA0. Consequently, when transmission is disabled (bit 3 (TXEA0) of CSIMA0 = 0), write dummy data to the SIOA0 register to start the communication operation, and then perform a receive operation.

2. Do not write data to SIOA0 while the automatic transmit/receive function is operating.

17.3 Registers Controlling Serial Interface CSIA0

Serial interface CSIA0 is controlled by the following nine registers.

- Serial operation mode specification register 0 (CSIMA0)
- Serial status register 0 (CSIS0)
- Serial trigger register 0 (CSIT0)
- Divisor selection register 0 (BRGCA0)
- Automatic data transfer address point specification register 0 (ADTP0)
- Automatic data transfer interval specification register 0 (ADTI0)
- Automatic data transfer address count register 0 (ADTC0)
- Port mode register 14 (PM14)
- Port register 14 (P14)

(1) Serial operation mode specification register 0 (CSIMA0)

This is an 8-bit register used to control the serial communication operation.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

CHAPTER 22 STANDBY FUNCTION

22.1 Standby Function and Configuration

22.1.1 Standby function

The standby function is mounted onto all 78K0/Kx2 microcontroller products.

The standby function is designed to reduce the operating current of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, internal low-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

Note The 78K0/KB2 is not provided with a subsystem clock oscillator.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The subsystem clock oscillation cannot be stopped. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

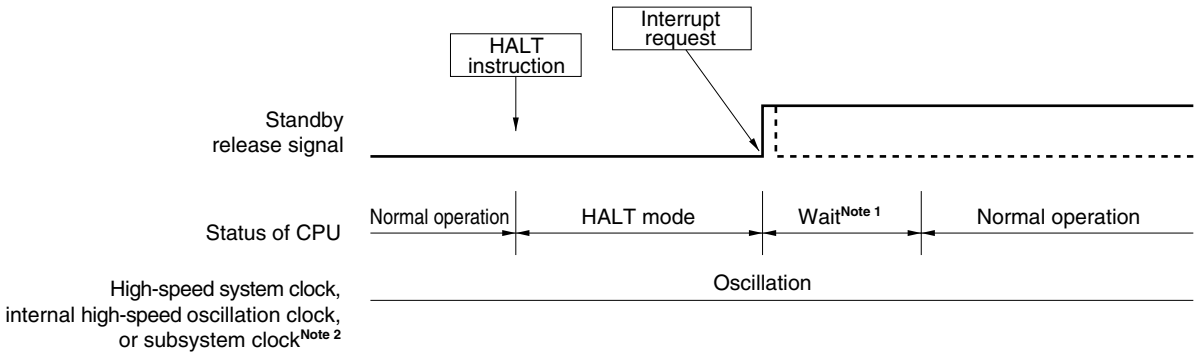
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 22-3. HALT Mode Release by Interrupt Request Generation



Notes 1. The wait time is as follows:

- When vectored interrupt servicing is carried out: 11 or 12 clocks
- When vectored interrupt servicing is not carried out: 4 or 5 clocks

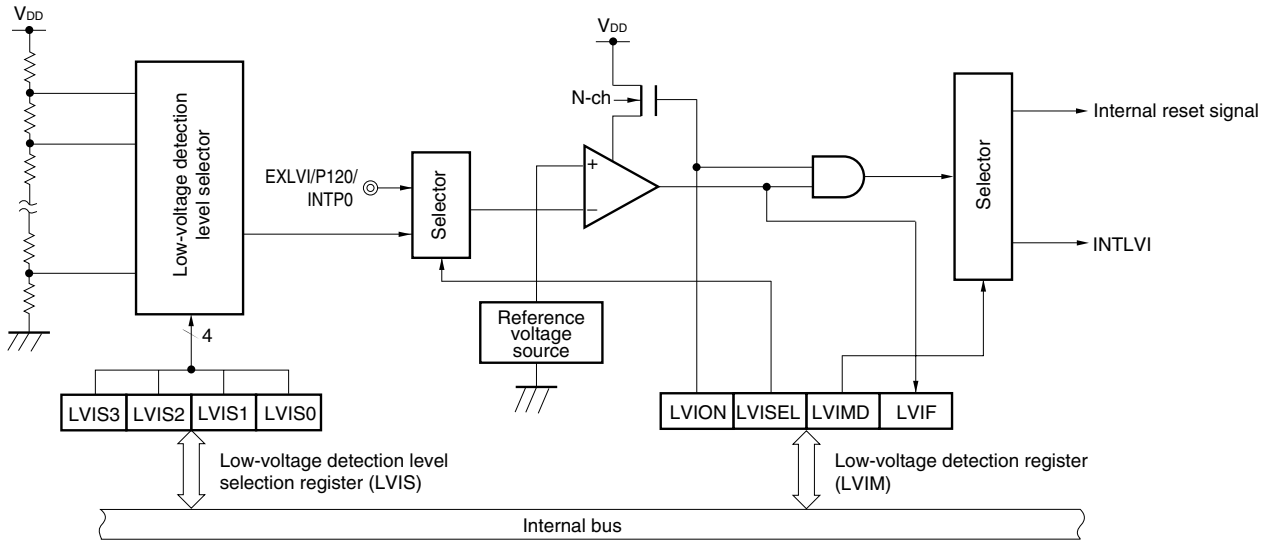
2. The 78K0/KB2 is not provided with a subsystem clock.

Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

25.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 25-1.

Figure 25-1. Block Diagram of Low-Voltage Detector



25.3 Registers Controlling Low-Voltage Detector

The low-voltage detector is controlled by the following registers.

- Low-voltage detection register (LVIM)
- Low-voltage detection level selection register (LVIS)
- Port mode register 12 (PM12)

(1) Low-voltage detection register (LVIM)

This register sets low-voltage detection and the operation mode.

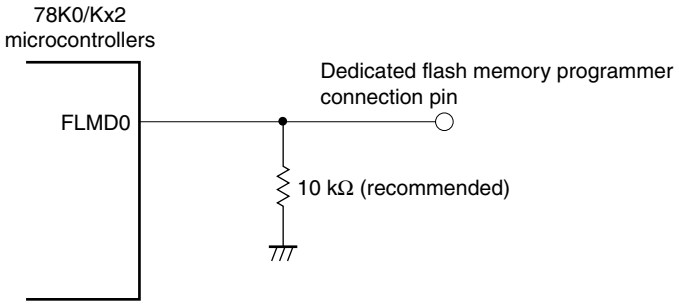
This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

27.6.1 FLMD0 pin

In the normal operation mode, 0 V is input to the FLMD0 pin. In the flash memory programming mode, the V_{DD} write voltage is supplied to the FLMD0 pin. An FLMD0 pin connection example is shown below.

Figure 27-6. FLMD0 Pin Connection Example



27.6.2 Serial interface pins

The pins used by each serial interface are listed below.

Table 27-5. Pins Used by Each Serial Interface

Serial Interface	Pins Used
CSI10	SO10, SI10, $\overline{SCK10}$
UART6	TxD6, RxD6

To connect the dedicated flash memory programmer to the pins of a serial interface that is connected to another device on the board, care must be exercised so that signals do not collide or that the other device does not malfunction.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

DC Characteristics (3/4)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA				0.7	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH1} = 2.0 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 0.5 mA				0.4	V
	V_{OL2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA				0.4	V
		P121 to P124	I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA				2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA				0.4	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA				0.6	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 3.0 mA				0.4	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA				0.4	V
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P140 to P145, FLMD0, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH2}	P20 to P27	V_I = AV_{REF} = V_{DD}				1	μA
	I_{LIH3}	P121 to 124 (X1, X2, XT1, XT2)	V_I = V_{DD}	I/O port mode			1	μA
				OSC mode			20	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P140 to P145, FLMD0, $\overline{\text{RESET}}$	V_I = V_{SS}				–1	μA
	I_{LIL2}	P20 to P27	V_I = V_{SS}, AV_{REF} = V_{DD}				–1	μA
	I_{LIL3}	P121 to 124 (X1, X2, XT1, XT2)	V_I = V_{SS}	I/O port mode			–1	μA
				OSC mode			–20	μA
Pull-up resistor	R_U	V_I = V_{SS}			10	20	100	kΩ
FLMD0 supply voltage	V_{IL}	In normal operation mode			0		0.2V_{DD}	V
	V_{IH}	In self-programming mode			0.8V_{DD}		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

DC Characteristics (4/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		3.2	5.5	mA
				Resonator connection		4.5	6.9	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		1.6	2.8	mA
				Resonator connection		2.3	3.9	mA
			f_{XH} = 10 MHz V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		1.5	2.7	mA
				Resonator connection		2.2	3.2	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.9	1.6	mA
				Resonator connection		1.3	2.0	mA
			f_{XH} = 5 MHz, V_{DD} = 2.0 V [Notes 2, 3]	Square wave input		0.7	1.4	mA
				Resonator connection		1.0	1.6	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			1.4	2.5	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		6	30	μA
				Resonator connection		15	35	μA
	I_{DD2}	HALT mode	f_{XH} = 20 MHz, V_{DD} = 5.0 V [Note 2]	Square wave input		0.8	2.6	mA
				Resonator connection		2.0	4.4	mA
			f_{XH} = 10 MHz, V_{DD} = 5.0 V [Notes 2, 3]	Square wave input		0.4	1.3	mA
				Resonator connection		1.0	2.4	mA
			f_{XH} = 5 MHz, V_{DD} = 3.0 V [Notes 2, 3]	Square wave input		0.2	0.65	mA
				Resonator connection		0.5	1.1	mA
			f_{RH} = 8 MHz, V_{DD} = 5.0 V [Note 4]			0.4	1.2	mA
			f_{SUB} = 32.768 kHz, V_{DD} = 5.0 V [Note 5]	Square wave input		3.0	27	μA
				Resonator connection		12	32	μA
	I_{DD3}[Note 6]	STOP mode				1	20	μA
			T_A = −40 to +70 °C			1	10	μA
A/D converter operating current	I_{ADC}[Note 7]	2.3 V ≤ AV_{REF} ≤ V_{DD}, ADCS = 1				0.86	1.9	mA
Watchdog timer operating current	I_{WDT}[Note 8]	During 240 kHz internal low-speed oscillation clock operation				5	10	μA
LVI operating current	I_{LVI}[Note 9]					9	18	μA

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or external subsystem clock frequency)

(Notes on next page)

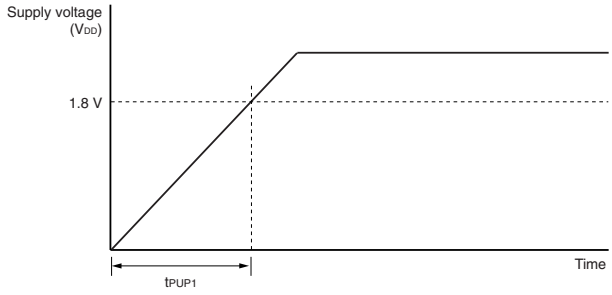
Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Supply Voltage Rise Time (T_A = –40 to +85°C, V_{SS} = EV_{SS} = 0 V)

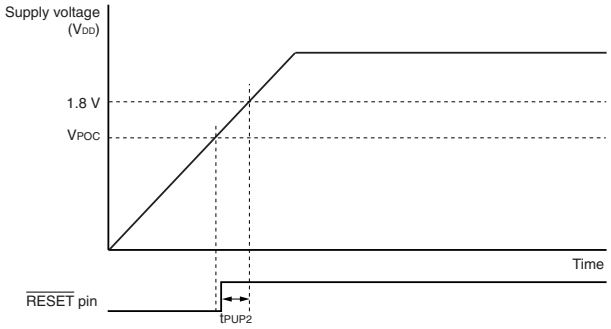
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (V_{DD}: 0 V → 1.8 V)	t_{PUP1}	POCMODE (option byte) = 0, when $\overline{RESET}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (releasing $\overline{RESET}$ input → V_{DD}: 1.8 V)	t_{PUP2}	POCMODE (option byte) = 0, when $\overline{RESET}$ input is used			1.9	ms

Supply Voltage Rise Time Timing

• When $\overline{RESET}$ pin input is not used



• When $\overline{RESET}$ pin input is used



2.7 V POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option bye) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until V_{POC} = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC}, similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until V_{DDPOC} = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at V_{POC} = 1.59 V (TYP.) and not at V_{DDPOC}. The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH}.