Renesas Electronics America Inc - UPD78F0537AGB-GAH-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0537agb-gah-ax

(4/6)

78K0/Kx2 Microcontrollers	Package	Product type	Quality grace	Part Number
78K0/KE2	64-pin plastic LQFP (14x14)	Conventional-specification products	Standard products	μPD78F0531GC-UBS-A, 78F0532GC-UBS-A, 78F0533GC-UBS-A, 78F0534GC-UBS-A, 78F0535GC-UBS-A, 78F0536GC-UBS-A, 78F0537GC-UBS-A, 78F0537DGC-UBS-A[Note]
			(A) grade products	μPD78F0531GC(A)-GAL-AX, 78F0532GC(A)-GAL-AX, 78F0533GC(A)-GAL-AX, 78F0534GC(A)-GAL-AX, 78F0535GC(A)-GAL-AX, 78F0536GC(A)-GAL-AX, 78F0537GC(A)-GAL-AX
			(A2) grade products	μPD78F0531GC(A2)-GAL-AX, 78F0532GC(A2)-GAL-AX, 78F0533GC(A2)-GAL-AX, 78F0534GC(A2)-GAL-AX, 78F0535GC(A2)-GAL-AX, 78F0536GC(A2)-GAL-AX, 78F0537GC(A2)-GAL-AX
		Expanded-specification products	Standard products	μPD78F0531AGC-GAL-AX, 78F0532AGC-GAL-AX, 78F0533AGC-GAL-AX, 78F0534AGC-GAL-AX, 78F0535AGC-GAL-AX, 78F0536AGC-GAL-AX, 78F0537AGC-GAL-AX, 78F0537DAGC-GAL-AX[Note]
			(A) grade products	μPD78F0531AGCA-GAL-G, 78F0532AGCA-GAL-G, 78F0533AGCA-GAL-G, 78F0534AGCA-GAL-G, 78F0535AGCA-GAL-G, 78F0536AGCA-GAL-G, 78F0537AGCA-GAL-G
			(A2) grade products	μPD78F0531AGCA2-GAL-G, 78F0532AGCA2-GAL-G, 78F0533AGCA2-GAL-G, 78F0534AGCA2-GAL-G, 78F0535AGCA2-GAL-G, 78F0536AGCA2-GAL-G, 78F0537AGCA2-GAL-G

Note The μPD78F0537D and 78F0537DA have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

(c) V_{DD} and EV_{DD}

V_{DD} is the positive power supply pin for P121 to P124 and other than ports[Note].

EV_{DD} is the positive power supply pin for ports other than P20 to P27 and P121 to P124.

Always make EV_{DD} the same potential as V_{DD}.

Note With products that are not mounted with an EV_{DD} pin, use V_{DD} as a positive power supply pin other than P20 to P27.

(d) V_{SS} and EV_{SS}

V_{SS} is the ground potential pin for P121 to P124 and other than ports.

EV_{SS} is the ground potential pin for ports other than P20 to P27 and P121 to P124.

Always make EV_{SS} the same potential as V_{SS}.

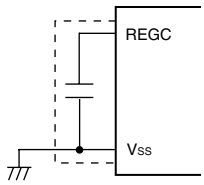
Note With products that are not mounted with an EV_{SS} pin, use V_{SS} as a ground potential pin other than P20 to P27.

2.2.13 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

2.2.14 REGC

This is the pin for connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF).



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

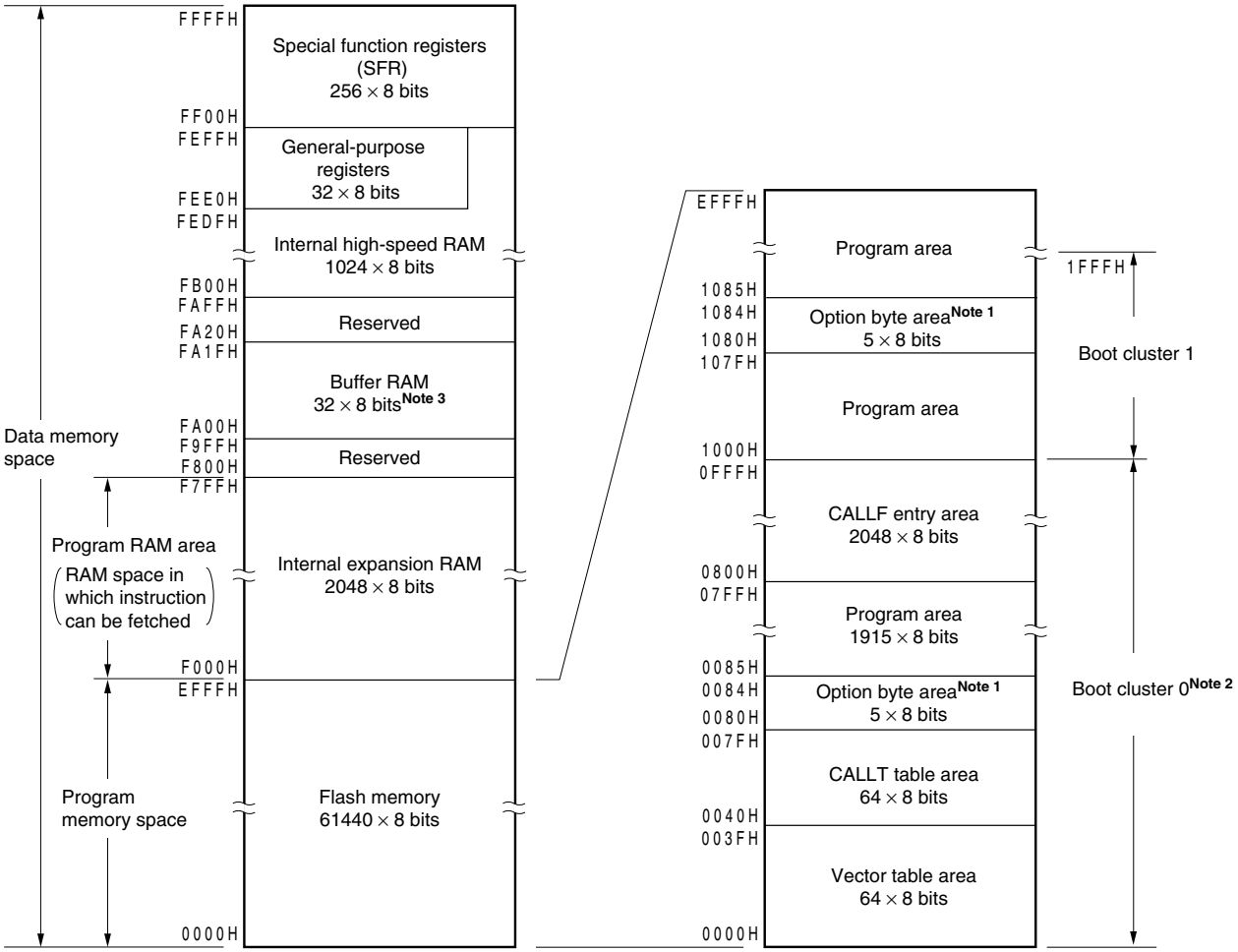
2.2.15 FLMD0

This is a pin for setting flash memory programming mode.

Connect FLMD0 to EV_{SS} or V_{SS} in the normal operation mode.

In flash memory programming mode, connect this pin to the flash memory programmer.

Figure 3-7. Memory Map (μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, 78F0535A, 78F0545, and 78F0545A)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H.
When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

3. The buffer RAM is incorporated only in the μPD78F0545 and 78F0545A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0515, 78F0515A, 78F0525, 78F0525A, 78F0535, and 78F0535A.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.

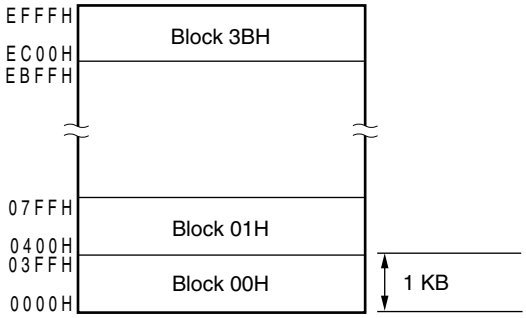
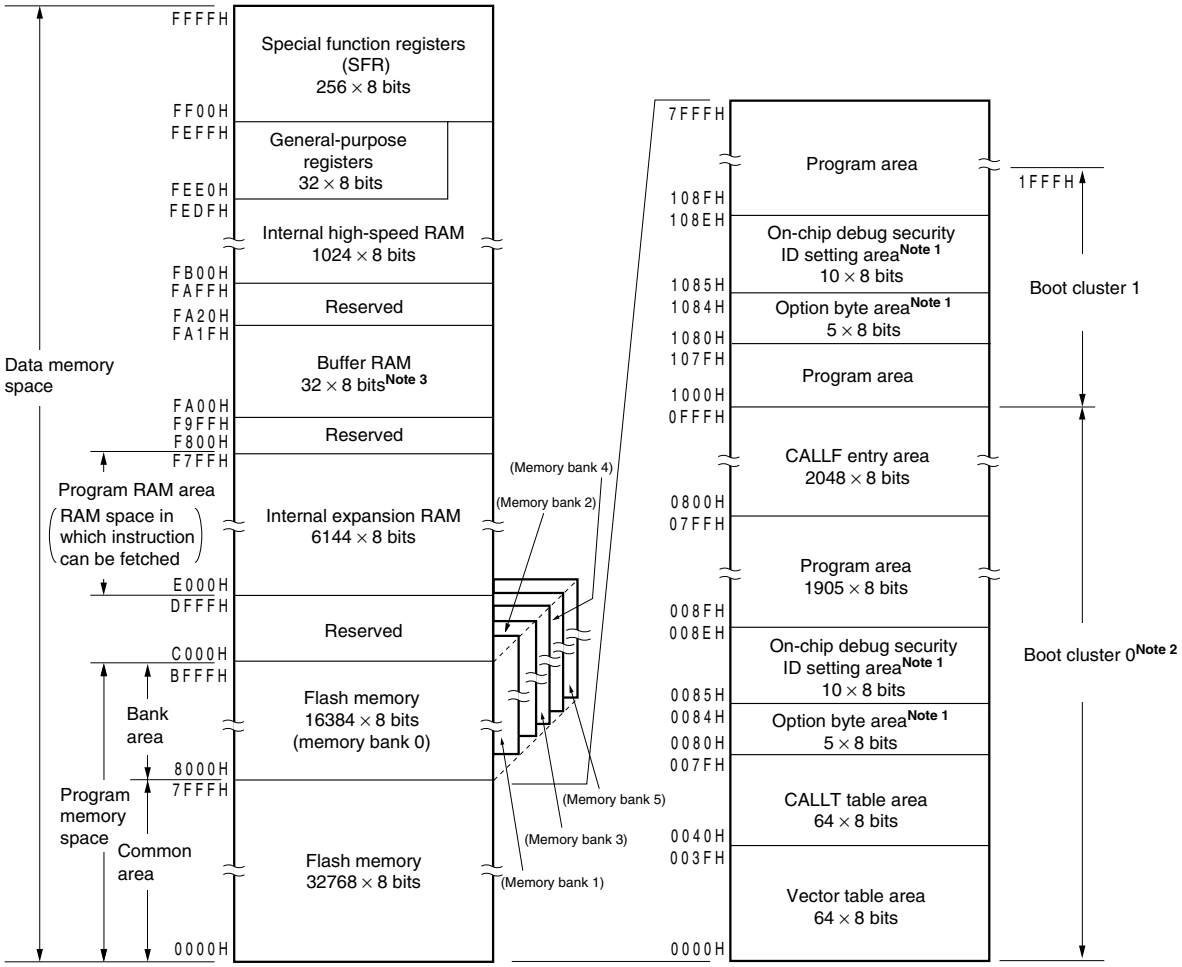


Figure 3-11. Memory Map (μPD78F0527D, 78F0527DA, 78F0537D, 78F0537DA, 78F0547D, and 78F0547DA)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **27.8 Security Settings**).

3. The buffer RAM is incorporated only in the μPD78F0547D and 78F0547DA (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0527D, 78F0527DA, 78F0537D and 78F0537DA.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-3 Correspondence Between Address Values and Block Numbers in Flash Memory**.

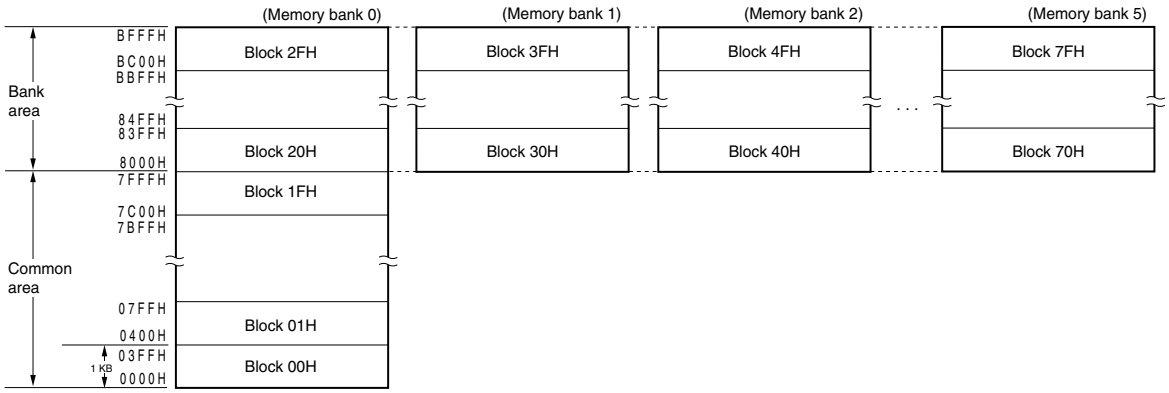
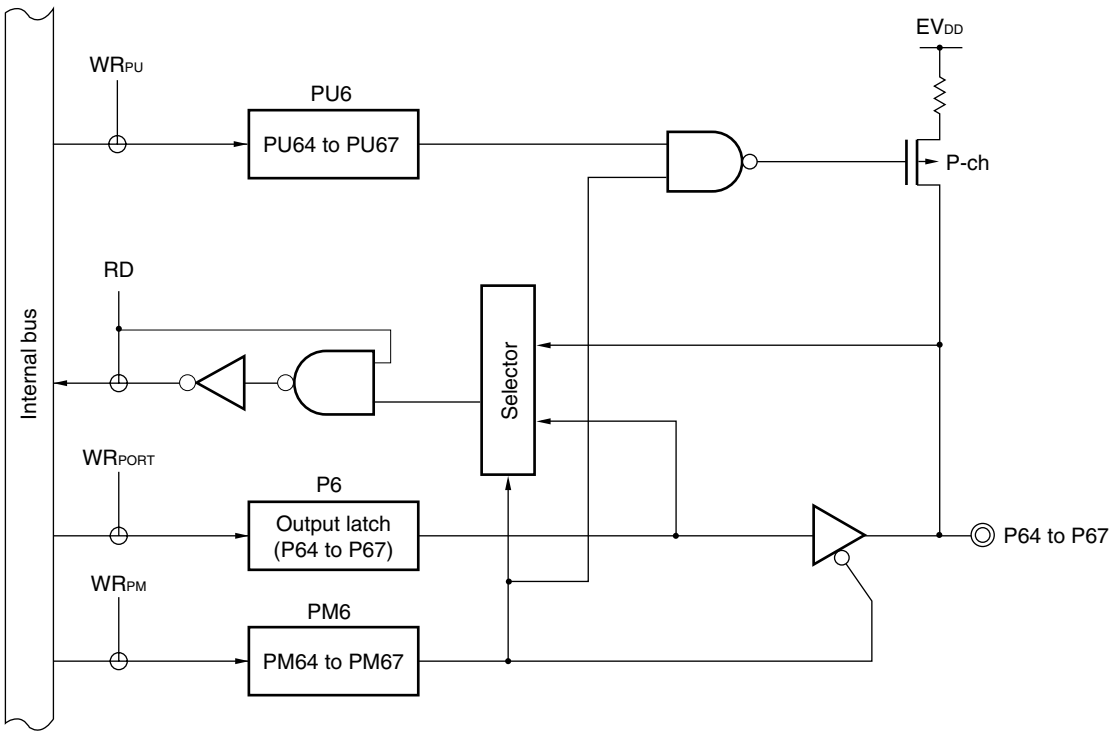


Figure 5-20. Block Diagram of P64 to P67



P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

Figure 7-56. Example of Register Settings for Pulse Width Measurement (1/2)

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	0/1	0/1	0	0

01: Free running timer mode
10: Clear and start mode entered by valid edge of TI00n pin.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	1	0/1	1

1: CR00n used as capture register

0: TI01n pin is used as capture trigger of CR00n.
1: Reverse phase of TI00n pin is used as capture trigger of CR00n.

1: CR01n used as capture register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0	0	0	0

(d) Prescaler mode register 0n (PRM0n)

ES1n1	ES1n0	ES0n1	ES0n0	3	2	PRM0n1	PRM0n0
0/1	0/1	0/1	0/1	0	0	0/1	0/1

Selects count clock
(setting valid edge of TI00n is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection
(setting when CRC0n1 = 1 is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

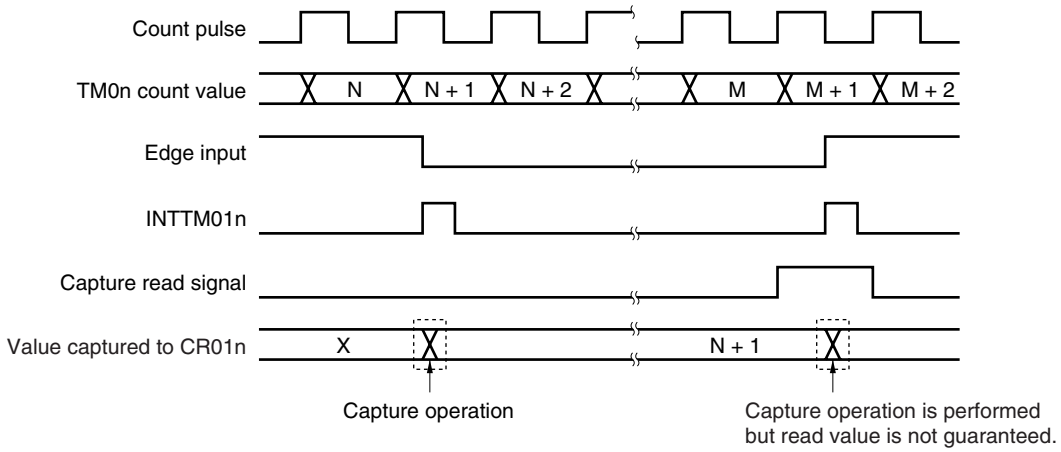
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(4) Timing of holding data by capture register

(a) When the valid edge is input to the TI00n/TI01n pin and the reverse phase of the TI00n pin is detected while CR00n/CR01n is read, CR01n performs a capture operation but the read value of CR00n/CR01n is not guaranteed. At this time, an interrupt signal (INTTM00n/INTTM01n) is generated when the valid edge of the TI00n/TI01n pin is detected (the interrupt signal is not generated when the reverse-phase edge of the TI00n pin is detected).

When the count value is captured because the valid edge of the TI00n/TI01n pin was detected, read the value of CR00n/CR01n after INTTM00n/INTTM01n is generated.

Figure 7-61. Timing of Holding Data by Capture Register



(b) The values of CR00n and CR01n are not guaranteed after 16-bit timer/event counter 0n stops.

(5) Setting valid edge

Set the valid edge of the TI00n pin while the timer operation is stopped (TMC0n3 and TMC0n2 = 00). Set the valid edge by using ES0n0 and ES0n1.

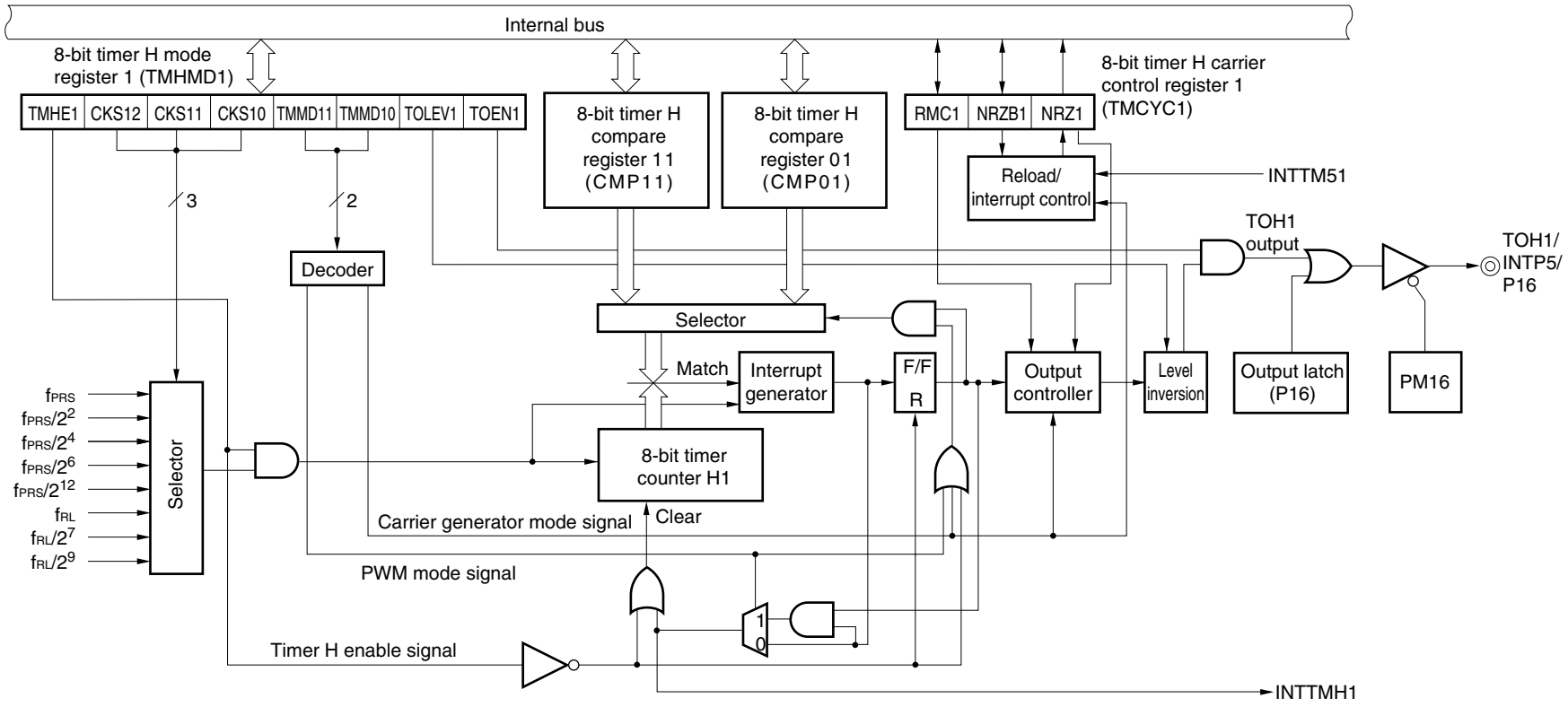
(6) Re-triggering one-shot pulse

Make sure that the trigger is not generated while an active level is being output in the one-shot pulse output mode. Be sure to input the next trigger after the current active level is output.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 9-2. Block Diagram of 8-Bit Timer H1



CHAPTER 11 WATCHDOG TIMER

11.1 Functions of Watchdog Timer

The watchdog timer is mounted onto all 78K0/Kx2 microcontroller products.

The watchdog timer operates on the internal low-speed oscillation clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to WDTE
- If data is written to WDTE during a window close period
- If the instruction is fetched from an area not set by the IMS and IXS registers (detection of an invalid check while the CPU hangs up)
- If the CPU accesses an area that is not set by the IMS and IXS registers (excluding FB00H to FFCFH and FFE0H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of RESF, see **CHAPTER 23 RESET FUNCTION**.

13.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$1LSB = 1/2^{10} = 1/1024$
$= 0.098\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 13-14. Overall Error

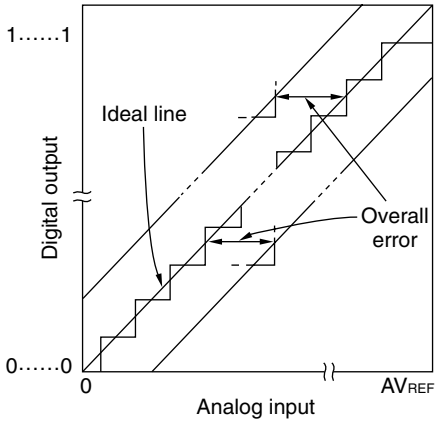
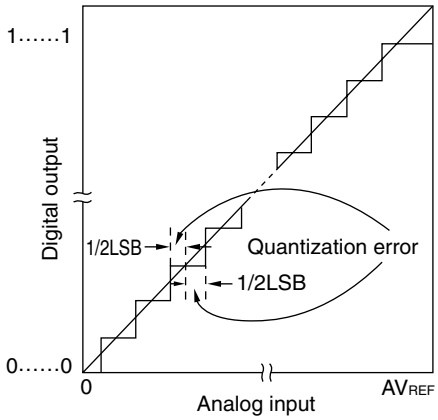


Figure 13-15. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.
If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

17.4.2 3-wire serial I/O mode

The one-byte data transmission/reception is executed in the mode in which bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) is cleared to 0.

The 3-wire serial I/O mode is useful for connecting peripheral ICs and display controllers with a clocked serial interface.

In this mode, communication is executed by using three lines: serial clock ($\overline{SCKA0}$), serial output (SOA0), and serial input (SIA0) lines.

(1) Registers used

- Serial operation mode specification register 0 (CSIMA0)[Note 1]
- Serial status register 0 (CSIS0)[Note 2]
- Divisor selection register 0 (BRGCA0)
- Port mode register 14 (PM14)
- Port register 14 (P14)

Notes 1. Bits 7, 6, and 4 to 1 (CSIAE0, ATE0, MASTER0, TXEA0, RXEA0, and DIR0) are used. Setting of bit 5 (ATM0) is invalid.

2. Only bit 0 (TSF0) and bit 6 (CKS00) are used.

The basic procedure of setting an operation in the 3-wire serial I/O mode is as follows.

<1> Set bit 6 (CKS00) of the CSIS0 register (see **Figure 17-3**)[Note 1].
<2> Set the BRGCA0 register (see **Figure 17-5**)[Note 1].
<3> Set bits 4 to 1 (MASTER0, TXEA0, RXEA0, and DIR0) of the CSIMA0 register (see **Figure 17-2**).
<4> Set bit 7 (CSIAE0) of the CSIMA0 register to 1 and clear bit 6 (ATE0) to 0.
<5> Write data to serial I/O shift register 0 (SIOA0). → Data transmission/reception is started[Note 2].

Notes 1. This register does not have to be set when the slave mode is specified (MASTER0 = 0).

2. Write dummy data to SIOA0 only for reception.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

(e) Automatic transmission/reception suspension and restart

Automatic transmission/reception can be temporarily suspended by setting bit 1 (ATSTP0) of serial trigger register 0 (CSIT0) to 1.

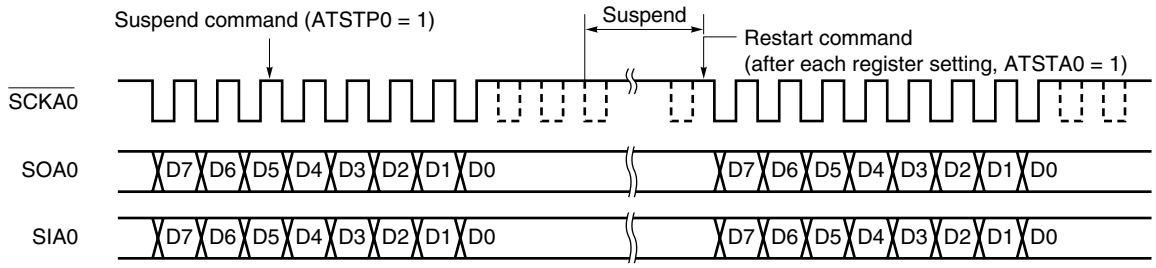
During 8-bit data communication, the transmission/reception is not suspended. It is suspended upon completion of 8-bit data communication.

When suspended, bit 0 (TSF0) of serial status register 0 (CSIS0) is cleared to 0 after transfer of the 8th bit.

Cautions 1. If the HALT instruction is executed during automatic transmission/reception, communication is suspended and the HALT mode is set if during 8-bit data communication. When the HALT mode is cleared, automatic transmission/reception is restarted from the suspended point.

2. When suspending automatic transmission/reception, do not change the operating mode to 3-wire serial I/O mode while TSF0 = 1.

Figure 17-22. Automatic Transmission/Reception Suspension and Restart



ATSTP0: Bit 1 of serial trigger register 0 (CSIT0)

ATSTA0: Bit 0 of CSIT0

CHAPTER 19 MULTIPLIER/DIVIDER

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2
Multiplier/divider	–	Products whose flash memory is less than 32 KB: – Products whose flash memory is at least 48 KB: √			

Remark √: Mounted, –: Not mounted

Caution Do not use serial interface IIC0 and the multiplier/divider simultaneously, because various flags corresponding to interrupt request sources are shared among serial interface IIC0 and the multiplier/divider.

19.1 Functions of Multiplier/Divider

The multiplier/divider has the following functions.

- 16 bits × 16 bits = 32 bits (multiplication)
- 32 bits ÷ 16 bits = 32 bits, 16-bit remainder (division)

19.2 Configuration of Multiplier/Divider

The multiplier/divider includes the following hardware.

Table 19-1. Configuration of Multiplier/Divider

Item	Configuration
Registers	Remainder data register 0 (SDR0) Multiplication/division data registers A0 (MDA0H, MDA0L) Multiplication/division data registers B0 (MDB0)
Control register	Multiplier/divider control register 0 (DMUC0)

Figure 19-1 shows the block diagram of the multiplier/divider.

25.4.2 When used as interrupt

(1) When detecting level of supply voltage (V_{DD})

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).
  - <3> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <4> Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <5> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <6> Use software to wait for an operation stabilization time (10 μs (MIN.)).
  - <7> Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, at bit 0 (LVIF) of LVIM.
  - <8> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <9> Release the interrupt mask flag of LVI (LVIMK).
  - <10> Execute the EI instruction (when vector interrupts are used).

  Figure 25-7 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <9> above.

- When stopping operation
  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVION to 0.

Table 27-16. Interrupt Response Time for Self Programming Library (Expanded-specification Products (μPD78F05xxA and 78F05xxDA)) (1/2)

(1) When internal high-speed oscillation clock is used

Library Name	Interrupt Response Time (μs (Max.))			
	Normal Model of C Compiler		Static Model of C Compiler/Assembler	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	1100.9	431.9	1095.3	426.3
Block erase library	1452.9	783.9	1447.3	778.3
Word write library	1247.2	579.2	1239.2	571.2
Block verify library	1125.9	455.9	1120.3	450.3
Set information library	906.9	312.0	905.8	311.0
EEPROM write library	1215.2	547.2	1213.9	545.9

Remarks 1. The above interrupt response times are those during stabilized operation of the internal high-speed oscillator (RSTS = 1).

2. RSTS: Bit 7 of the internal oscillation mode register (RCM)

(2) When high-speed system clock is used (normal model of C compiler)

Library Name	Interrupt Response Time (μs (Max.))			
	RSTOP = 0, RSTS = 1		RSTOP = 1	
	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range	Entry RAM location is outside short direct addressing range	Entry RAM location is in short direct addressing range
Block blank check library	179/f_{CPU} + 567	179/f_{CPU} + 246	179/f_{CPU} + 1708	179/f_{CPU} + 569
Block erase library	179/f_{CPU} + 780	179/f_{CPU} + 459	179/f_{CPU} + 1921	179/f_{CPU} + 782
Word write library	333/f_{CPU} + 763	333/f_{CPU} + 443	333/f_{CPU} + 1871	333/f_{CPU} + 767
Block verify library	179/f_{CPU} + 580	179/f_{CPU} + 259	179/f_{CPU} + 1721	179/f_{CPU} + 582
Set information library	80/f_{CPU} + 456	80/f_{CPU} + 200	80/f_{CPU} + 1598	80/f_{CPU} + 459
EEPROM write library[Note]	29/f_{CPU} + 767 333/f_{CPU} + 696	29/f_{CPU} + 447 333/f_{CPU} + 376	29/f_{CPU} + 767 333/f_{CPU} + 1838	29/f_{CPU} + 447 333/f_{CPU} + 700

Note The longer value of the EEPROM write library interrupt response time becomes the Max. value, depending on the value of f_{CPU}.

Remarks 1. f_{CPU}: CPU operation clock frequency

2. RSTOP: Bit 0 of the internal oscillation mode register (RCM)

3. RSTS: Bit 7 of the internal oscillation mode register (RCM)

<R> 27.11 Creating ROM Code to Place Order for Previously Written Product

Before placing an order with Renesas Electronics for a previously written product, the ROM code for the order must be created.

To create the ROM code, use the Hex Consolidation Utility (hereafter abbreviated to HCU) on the finished programs (hex files) and optional data (such as security settings for flash memory programs).

The HCU is a software tool that includes functions required for creating ROM code.

The HCU can be downloaded at the Renesas Electronics website.

(1) Website

http:www2.renesas.com/micro/en/ods → Click Version-up Service.

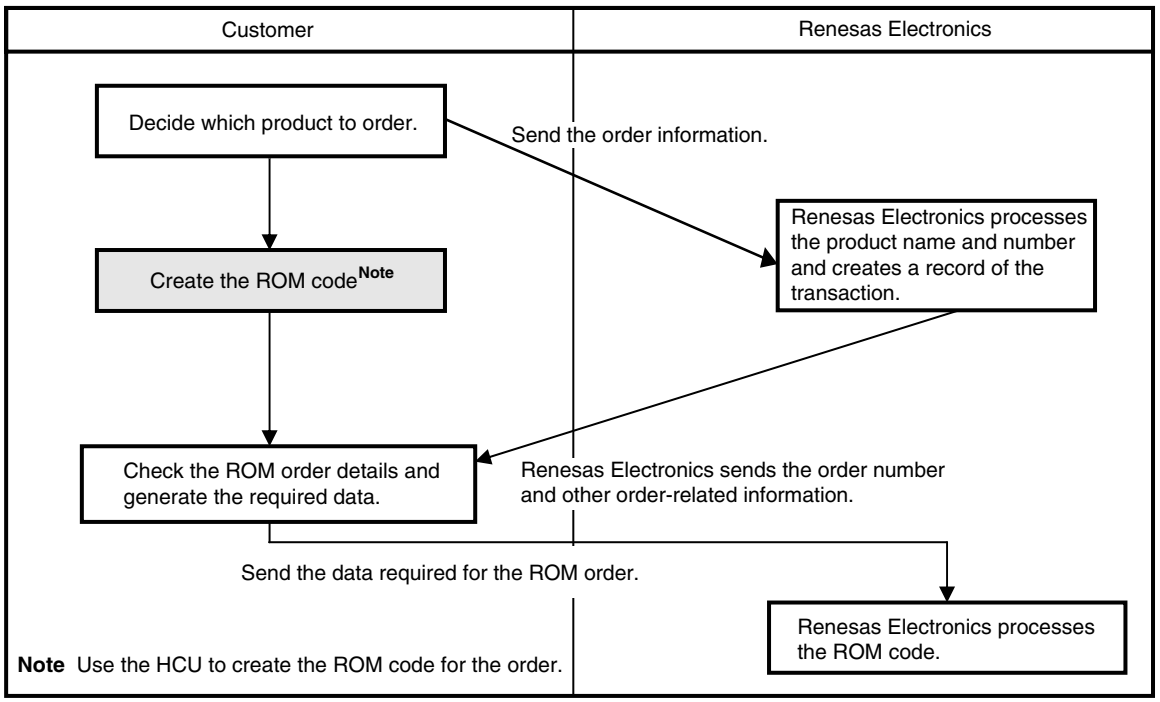
(2) Downloading the HCU

To download the HCU, click Software for previously written flash products and then HCU_GUI.

Remark For details about how to install and use the HCU, see the materials (the user's manual) that comes with the HCU at the above website.

27.11.1 Procedure for using ROM code to place an order

Use the HCU to create the ROM code by following the procedure below, and then place your order with Renesas Electronics. For details, see the ROM Code Ordering Method Information (C10302J).



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

DC Characteristics (2/4)

(T_A = –40 to +110°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high (products whose flash memory is at least 48 KB)[Note 1]	V_{IH1}	P02, P12, P13, P15, P40 to P47, P50 to P57, P64 to P67, P121 to P124, P144, P145		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P03 to P06, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140 to P143, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH4}	P60 to P63		0.7V_{DD}		6.0	V
Input voltage, high (products whose flash memory is less than 32 KB)[Note 2]	V_{IH1}	P02 to P06, P12, P13, P15, P40 to P43, P50 to P53, P121 to P124		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140, P141, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH4}	P60 to P63		0.7V_{DD}		6.0	V
Input voltage, low (products whose flash memory is at least 48 KB)[Note 1]	V_{IL1}	P02, P12, P13, P15, P40 to P47, P50 to P57, P60 to P67, P121 to P124, P144, P145		0		0.3V_{DD}	V
	V_{IL2}	P00, P01, P03 to P06, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140 to P143, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Input voltage, low (products whose flash memory is less than 32 KB)[Note 2]	V_{IL1}	P02 to P06, P12, P13, P15, P40 to P43, P50 to P53, P60 to P63, P121 to P124		0		0.3V_{DD}	V
	V_{IL2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140, P141, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –2.5 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OH2} = –100 μA	V_{DD} – 0.5			V
		P121 to P124	I_{OH2} = –100 μA	V_{DD} – 0.5			V

Notes 1. Supported products: 78K0/KD2 and 78K0/KE2 whose flash memory is at least 48 KB, and 78K0/KF2

2. Supported products: 78K0/KD2 and 78K0/KE2 whose flash memory is less than 32 KB, 78K0/KB2, and 78K0/KC2

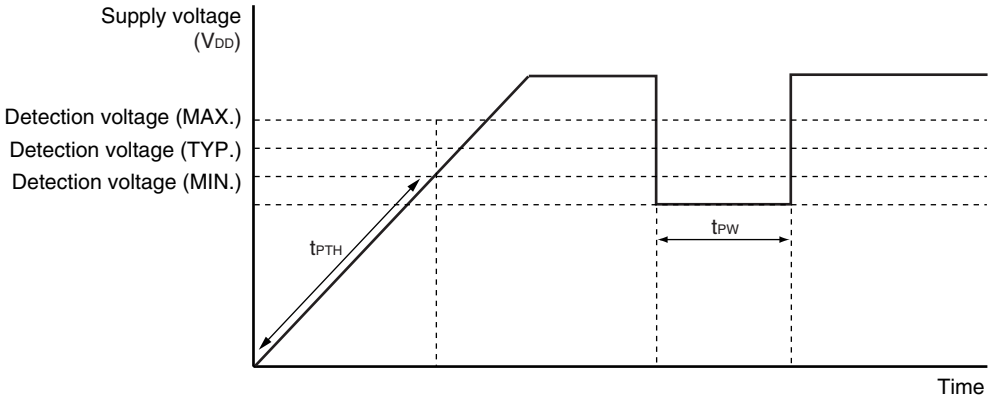
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

1.59 V POC Circuit Characteristics (T_A = –40 to +125°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		1.44	1.59	1.74	V
Power supply voltage rise inclination	t_{PTH}	V_{DD}: 0 V → change inclination of V_{POC}	0.5			V/ms
Minimum pulse width	t_{PW}		200			μs

1.59 V POC Circuit Timing

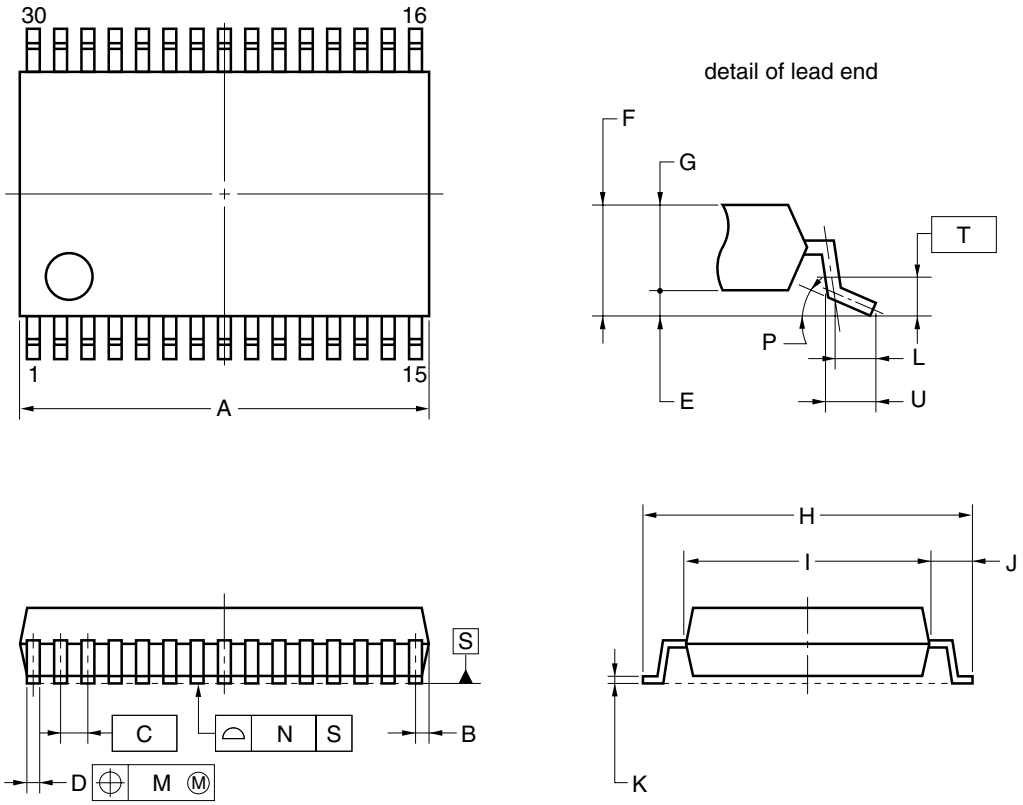


CHAPTER 34 PACKAGE DRAWINGS

34.1 78K0/KB2

- μPD78F0500MC-5A4-A, 78F0501MC-5A4-A, 78F0502MC-5A4-A, 78F0503MC-5A4-A, 78F0503DMC-5A4-A

30-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

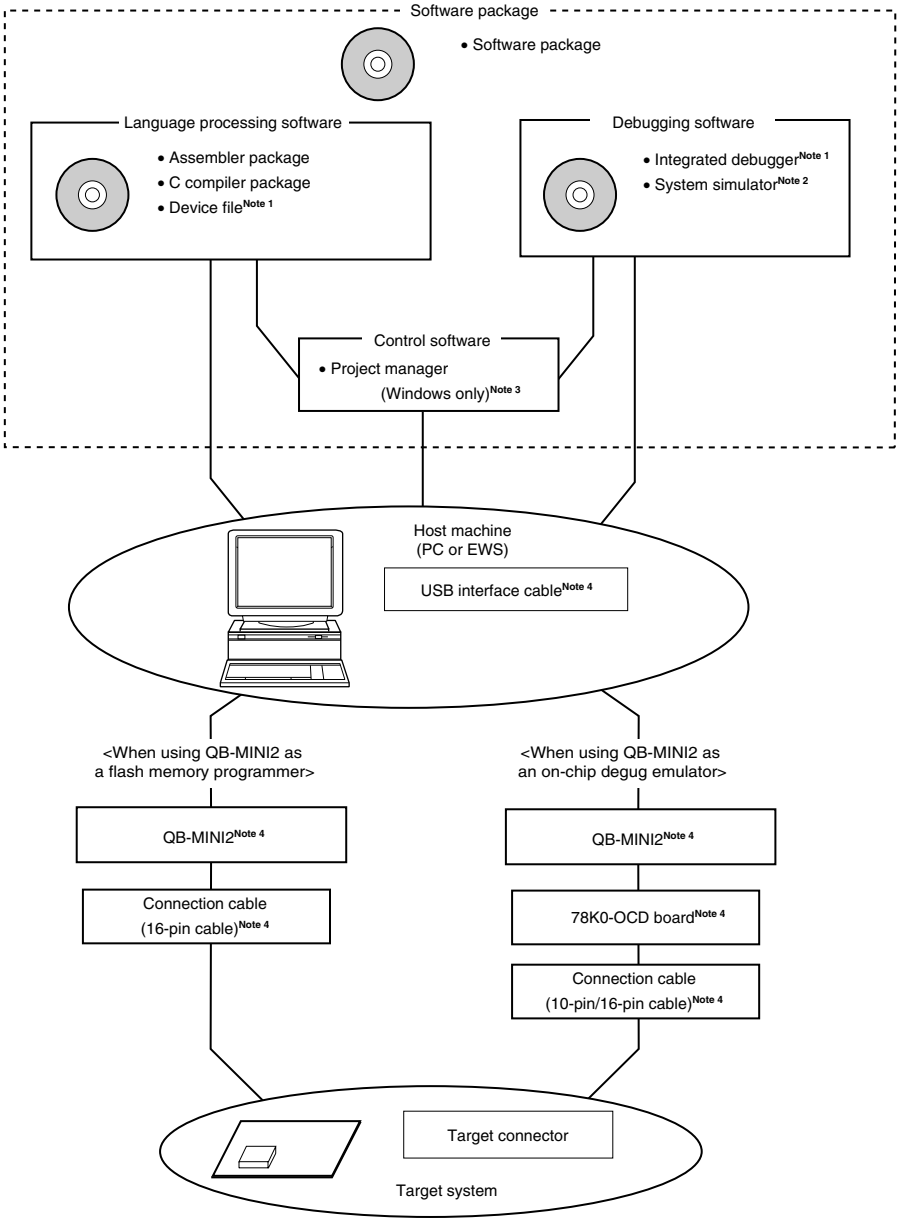
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

S30MC-65-5A4-2

Figure A-1. Development Tool Configuration (2/2)

(2) When using the on-chip debug emulator with programming function QB-MINI2



Notes 1. Download the device file for 78K0/Kx2 microcontrollers (DF780547) and the integrated debugger ID78K0-QB from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).

2. SM+ for 78K0 (instruction simulation version) is included in the software package. SM+ for 78K0/Kx2 (instruction + peripheral simulation version) is not included.

3. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows.

4. QB-MINI2 is supplied with USB interface cable, connection cables (10-pin cable and 16-pin cable), and 78K0-OCD board. Any other products are sold separately. In addition, download the software for operating the QB-MINI2 from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).