Renesas Electronics America Inc - UPD78F0537AGC-GAL-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0537agc-gal-ax

CONTENTS

2.1.4 78K0/KE2

(1) Port functions (1/2): 78K0/KE2

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P02				SO11 Note 1
P03				SI11 Note 1
P04				$\overline{\text{SCK11}}$ Note 1
P05				TI001 Note 1 / $\overline{\text{SSI11}}$ Note 1
P06				TI011 Note 1 / TO01 Note 1
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0 to ANI7
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1
P31				INTP2/OCD1A Note 2
P32				INTP3/OCD1B Note 2
P33				TI51/TO51/INTP4
P40 to P43	I/O	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P50 to P53	I/O	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P60	I/O	Port 6. 4-bit I/O port. Output of P60 to P63 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P62				EXSCL0
P63				–

Notes 1. Available only in the products whose flash memory is at least 48 KB.

2. μPD78F0537D and 78F0537DA (product with on-chip debug function) only

Table 3-8. Special Function Register List (4/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset	KB2	KC2	KD2	KE2	KF2
					1 Bit	8 Bits	16 Bits						
FFA5H	IIC shift register 0	IIC0		R/W	–	√	–	00H	√	√	√	√	√
FFA6H	IIC control register 0	IICC0		R/W	√	√	–	00H	√	√	√	√	√
FFA7H	Slave address register 0	SVA0		R/W	–	√	–	00H	√	√	√	√	√
FFA8H	IIC clock selection register 0	IICCL0		R/W	√	√	–	00H	√	√	√	√	√
FFA9H	IIC function expansion register 0	IICX0		R/W	√	√	–	00H	√	√	√	√	√
FFAAH	IIC status register 0	IICS0		R	√	√	–	00H	√	√	√	√	√
FFABH	IIC flag register 0	IICF0		R/W	√	√	–	00H	√	√	√	√	√
FFACH	Reset control flag register	RESF		R	–	√	–	00H Note 1	√	√	√	√	√
FFB0H FFB1H	16-bit timer counter 01	TM01		R	–	–	√	0000H	–	–	–	Note 2	√
FFB2H FFB3H	16-bit timer capture/compare register 001	CR001		R/W	–	–	√	0000H	–	–	–	Note 2	√
FFB4H FFB5H	16-bit timer capture/compare register 011	CR011		R/W	–	–	√	0000H	–	–	–	Note 2	√
FFB6H	16-bit timer mode control register 01	TMC01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFB7H	Prescaler mode register 01	PRM01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFB8H	Capture/compare control register 01	CRC01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFB9H	16-bit timer output control register 01	TOC01		R/W	√	√	–	00H	–	–	–	Note 2	√
FFBAH	16-bit timer mode control register 00	TMC00		R/W	√	√	–	00H	√	√	√	√	√
FFBBH	Prescaler mode register 00	PRM00		R/W	√	√	–	00H	√	√	√	√	√
FFBCH	Capture/compare control register 00	CRC00		R/W	√	√	–	00H	√	√	√	√	√
FFBDH	16-bit timer output control register 00	TOC00		R/W	√	√	–	00H	√	√	√	√	√
FFBEH	Low-voltage detection register	LVIM		R/W	√	√	–	00H Note 3	√	√	√	√	√
FFBFH	Low-voltage detection level selection register	LVIS		R/W	√	√	–	00H Note 3	√	√	√	√	√
FFE0H	Interrupt request flag register 0L	IF0	IF0L	R/W	√	√	√	00H	√	√	√	√	√
FFE1H	Interrupt request flag register 0H		IF0H	R/W	√	√		00H	√	√	√	√	√
FFE2H	Interrupt request flag register 1L	IF1	IF1L	R/W	√	√	√	00H	√	√	√	√	√
FFE3H	Interrupt request flag register 1H		IF1H	R/W	√	√		00H	√	√	√	√	√
FFE4H	Interrupt mask flag register 0L	MK0	MK0L	R/W	√	√	√	FFH	√	√	√	√	√
FFE5H	Interrupt mask flag register 0H		MK0H	R/W	√	√		FFH	√	√	√	√	√
FFE6H	Interrupt mask flag register 1L	MK1	MK1L	R/W	√	√	√	FFH	√	√	√	√	√
FFE7H	Interrupt mask flag register 1H		MK1H	R/W	√	√		FFH	√	√	√	√	√

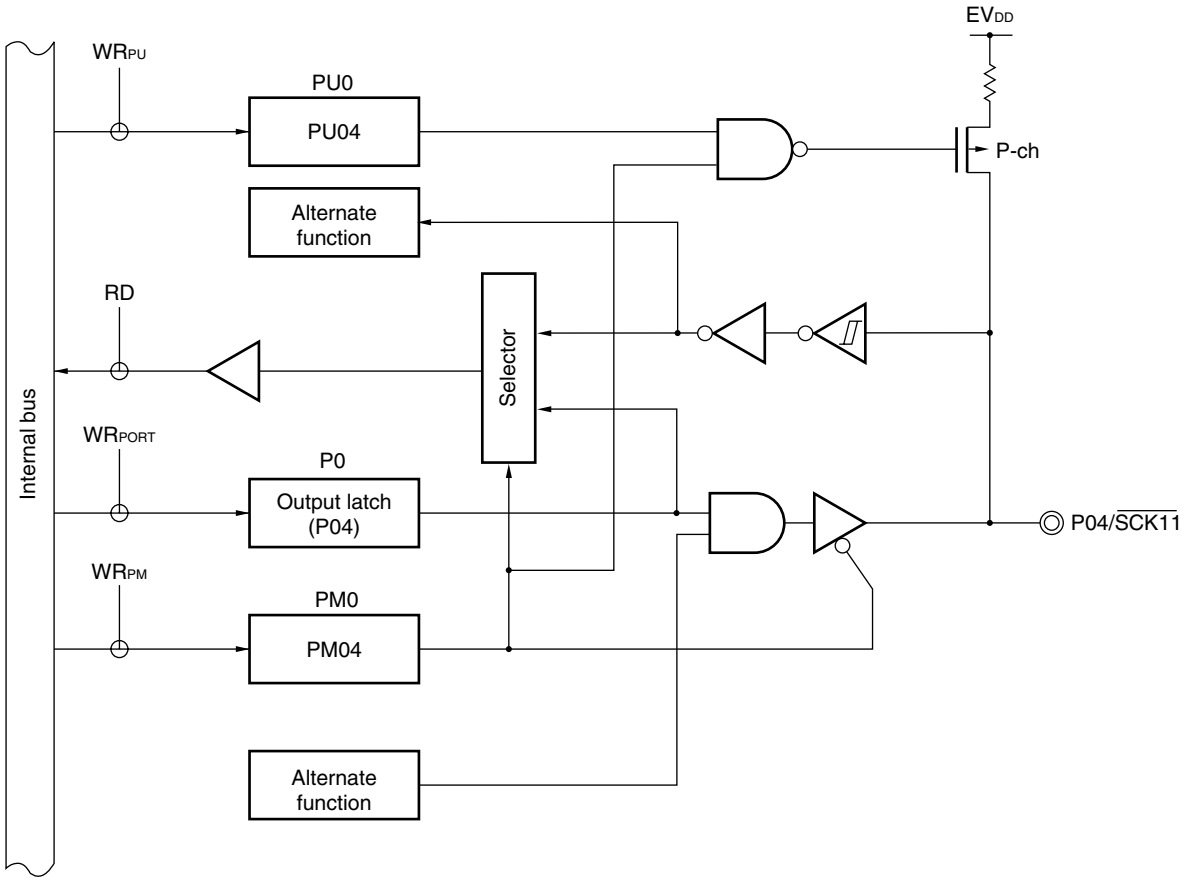
Notes 1. The reset value of RESF varies depending on the reset source.

2. This register is incorporated only in products whose flash memory is at least 48 KB.

3. The reset values of LVIM and LVIS vary depending on the reset source.

Figure 5-5. Block Diagram of P04 (2/2)

(2) 78K0/KE2 products whose flash memory is at least 48 KB and 78K0/KF2

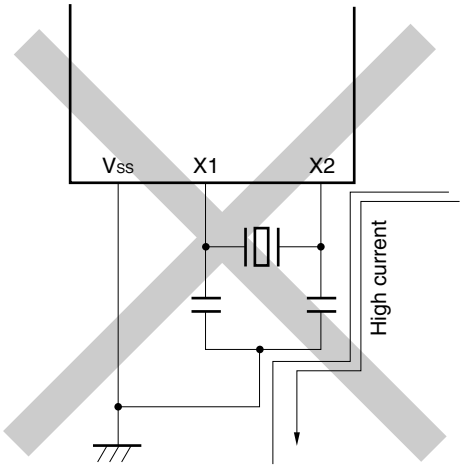


P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

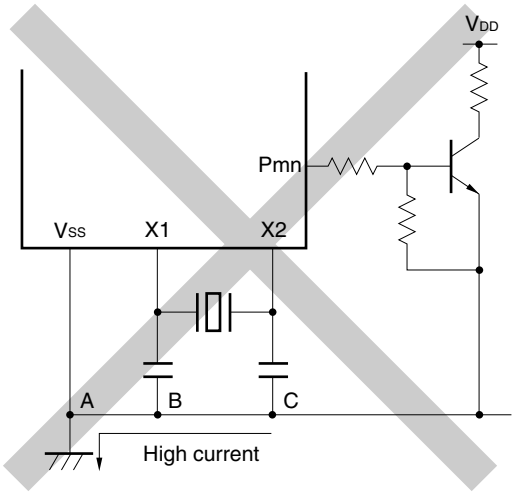
Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 6-14. Examples of Incorrect Resonator Connection (2/2)

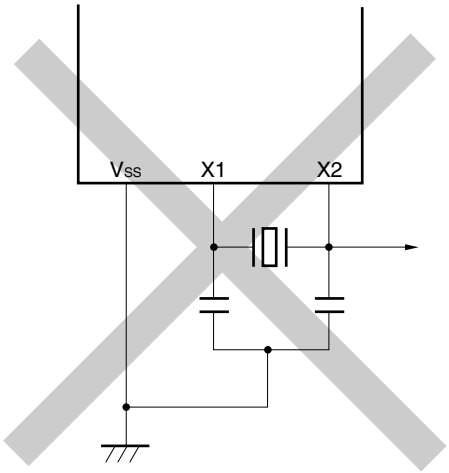
(c) Wiring near high alternating current



(d) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(e) Signals are fetched



Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Caution 2. When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

6.4.3 When subsystem clock is not used

If it is not necessary to use the subsystem clock[Note] for low power consumption operations, or if not using the subsystem clock as an I/O port, set the XT1 and XT2 pins to I/O mode (OSCSELS = 0) and connect them as follows.

Note The 78K0/KB2 is not provided with a subsystem clock.

Input (PM123/PM124 = 1): Independently connect to V_{DD} or V_{SS} via a resistor.
Output (PM123/PM124 = 0): Leave open.

Remark OSCSELS: Bit 4 of clock operation mode select register (OSCCTL)
PM123, PM124: Bits 3 and 4 of port mode register 12 (PM12)

6.4.4 Internal high-speed oscillator

The internal high-speed oscillator is incorporated in the 78K0/Kx2 microcontrollers. Oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal high-speed oscillator automatically starts oscillation (8 MHz (TYP.)).

6.4.5 Internal low-speed oscillator

The internal low-speed oscillator is incorporated in the 78K0/Kx2 microcontrollers.

The internal low-speed oscillation clock is only used as the watchdog timer and the clock of 8-bit timer H1. The internal low-speed oscillation clock cannot be used as the CPU clock.

“Can be stopped by software” or “Cannot be stopped” can be selected by the option byte. When “Can be stopped by software” is set, oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal low-speed oscillator automatically starts oscillation, and the watchdog timer is driven (240 kHz (TYP.)) if the watchdog timer operation is enabled using the option byte.

6.4.6 Prescaler

The prescaler generates the CPU clock by dividing the main system clock when the main system clock is selected as the clock to be supplied to the CPU.

Figure 7-6. Format of 16-Bit Timer Mode Control Register 00 (TMC00)

Address: FFBAH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
TMC00	0	0	0	0	TMC003	TMC002	TMC001	OVF00

TMC003	TMC002	Operation enable of 16-bit timer/event counter 00
0	0	Disables 16-bit timer/event counter 00 operation. Stops supplying operating clock. Clears 16-bit timer counter 00 (TM00).
0	1	Free-running timer mode
1	0	Clear & start mode entered by TI000 pin valid edge input[Note]
1	1	Clear & start mode entered upon a match between TM00 and CR000

TMC001	Condition to reverse timer output (TO00)
0	• Match between TM00 and CR000 or match between TM00 and CR010
1	• Match between TM00 and CR000 or match between TM00 and CR010 • Trigger input of TI000 pin valid edge

OVF00	TM00 overflow flag
Clear (0)	Clears OVF00 to 0 or TMC003 and TMC002 = 00
Set (1)	Overflow occurs.
OVF00 is set to 1 when the value of TM00 changes from FFFFH to 0000H in all the operation modes (free-running timer mode, clear & start mode entered by TI000 pin valid edge input, and clear & start mode entered upon a match between TM00 and CR000). It can also be set to 1 by writing 1 to OVF00.	

Note The TI000 pin valid edge is set by bits 5 and 4 (ES001, ES000) of prescaler mode register 00 (PRM00).

Figure 7-25. Example of Register Settings in External Event Counter Mode (2/2)

(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

If M is set to CR00n, the interrupt signal (INTTM00n) is generated when the number of external events reaches (M + 1).

Setting CR00n to 0000H is prohibited.

(g) 16-bit capture/compare register 01n (CR01n)

Usually, CR01n is not used in the external event counter mode. However, a compare match interrupt (INTTM01n) is generated when the set value of CR01n matches the value of TM0n.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK01n).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Notes 2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V ≤ V_{DD} < 2.7 V, the setting of CKS02 = CKS01 = CKS00 = 0 (count clock: f_{PRS}) is prohibited.

3. This is settable only if 4.0 V ≤ V_{DD} ≤ 5.5 V.

4. Note the following points when selecting the TM50 output as the count clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Cautions 1. When TMHE0 = 1, setting the other bits of TMHMD0 is prohibited. However, TMHMD0 can be refreshed (the same value is written).

2. In the PWM output mode, be sure to set the 8-bit timer H compare register 10 (CMP10) when starting the timer count operation (TMHE0 = 1) after the timer count operation was stopped (TMHE0 = 0) (be sure to set again even if setting the same value to CMP10).

3. The actual TOH0/P15 pin output is determined depending on PM15 and P15, besides TOH0 output.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

11.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 11-1. Configuration of Watchdog Timer

Item	Configuration
Control register	Watchdog timer enable register (WDTE)

How the counter operation is controlled, overflow time, and window open period are set by the option byte.

Table 11-2. Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (0080H)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)

Remark For the option byte, see **CHAPTER 26 OPTION BYTE**.

Figure 11-1. Block Diagram of Watchdog Timer

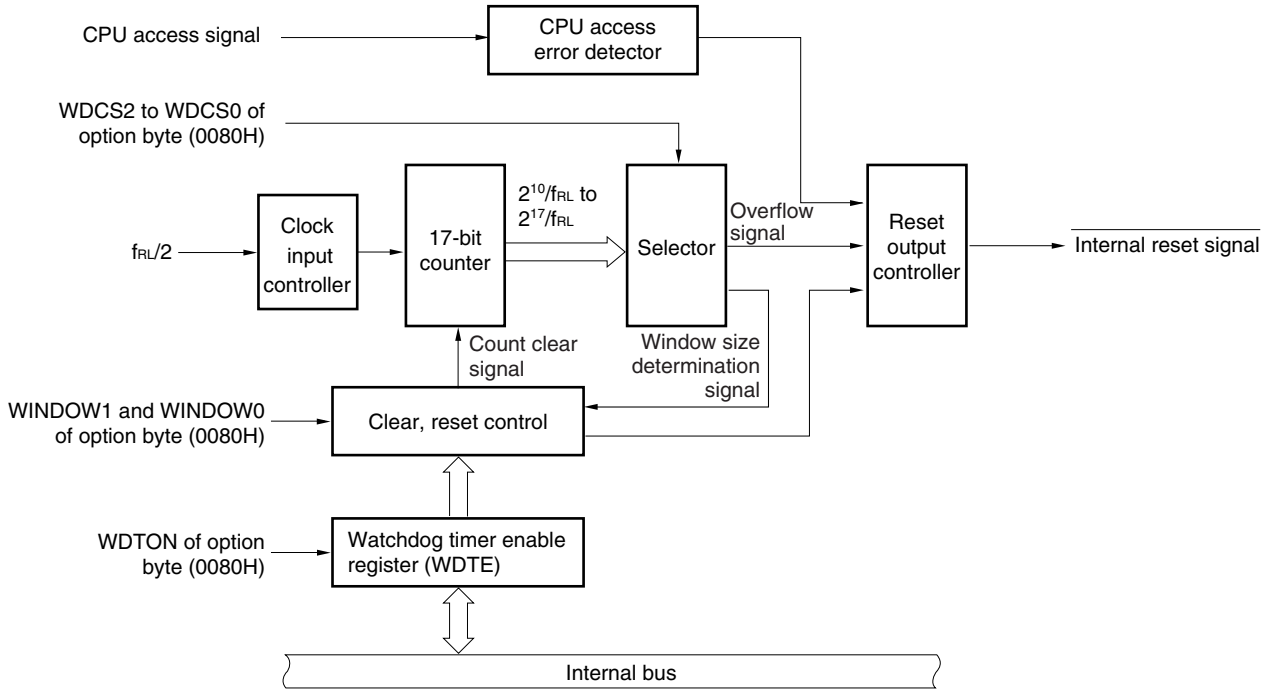
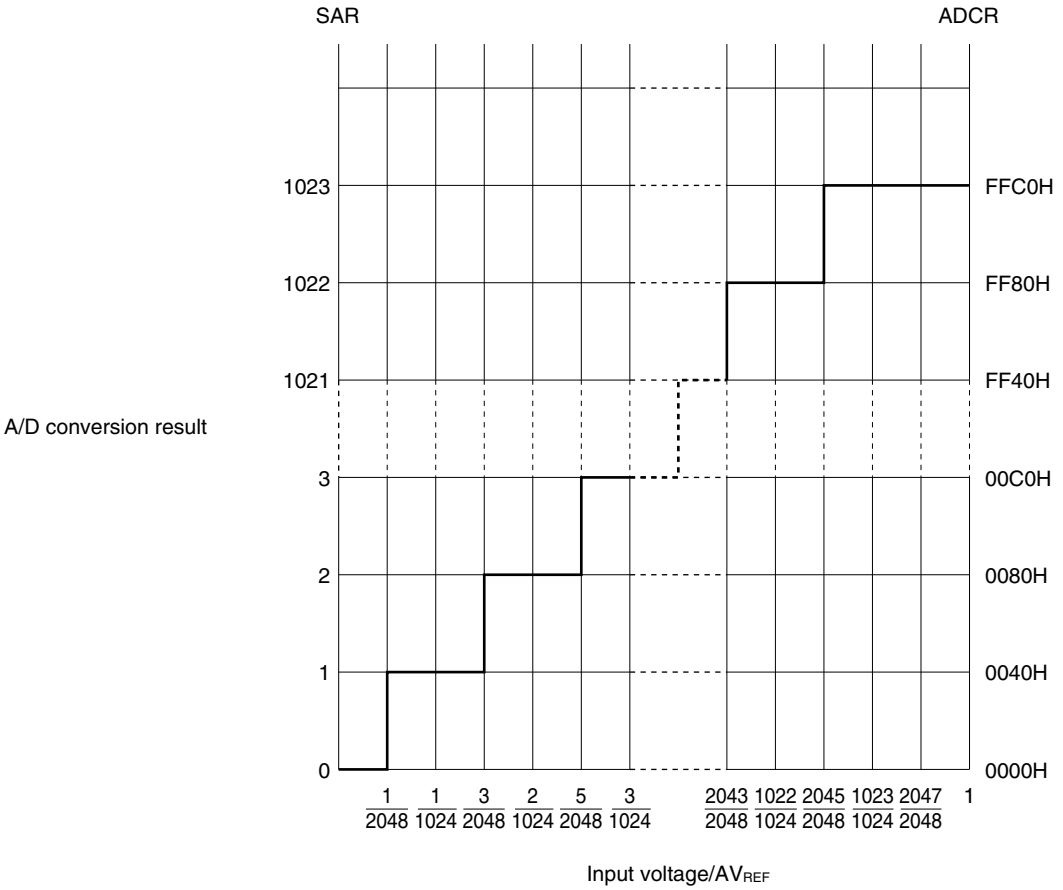


Figure 13-12 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 13-12. Relationship Between Analog Input Voltage and A/D Conversion Result



Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when $f_{PRS} = f_{XH}$ (XSEL = 1).)

2. Set the serial clock to satisfy the following conditions.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD) and Expanded-specification Products (μPD78F05xxA and 78F05xxDA)		
	Standard Products	(A) Grade Products	(A2) Grade Products
4.0 V ≤ V_{DD} ≤ 5.5 V	Serial clock ≤ 6.25 MHz	Serial clock ≤ 5 MHz	Serial clock ≤ 5 MHz
2.7 V ≤ V_{DD} < 4.0 V	Serial clock ≤ 4 MHz	Serial clock ≤ 2.5 MHz	Serial clock ≤ 2.5 MHz
1.8 V ≤ V_{DD} < 2.7 V	Serial clock ≤ 2 MHz	Serial clock ≤ 1.66 MHz	–

3. Do not start communication with the external clock from the $\overline{SCK10}$ pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. Do not write to CSIC10 while CSIE10 = 1 (operation enabled).

2. To use P10/$\overline{SCK10}$/TxD0 and P12/SO10 as general-purpose ports, set CSIC10 in the default status (00H).

3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock frequency

(3) Serial trigger register 0 (CSIT0)

This is an 8-bit register used to control execution/stop of automatic data transfer between buffer RAM and serial I/O shift register 0 (SIOA0).

This register can be set by a 1-bit or 8-bit memory manipulation instruction. This register can be set when bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) is 1.

Reset signal generation clears this register to 00H.

Figure 17-4. Format of Serial Trigger Register 0 (CSIT0)

Address: FF92H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
CSIT0	0	0	0	0	0	0	ATSTP0	ATSTA0

ATSTP0	Automatic data transfer stop
0	–
1	Automatic data transfer stopped

ATSTA0	Automatic data transfer start
0	–
1	Automatic data transfer started

Cautions 1. Even if ATSTP0 or ATSTA0 is set to 1, automatic transfer cannot be started/stopped until 1-byte transfer is complete.

2. ATSTP0 and ATSTA0 change to 0 automatically after the interrupt signal INTACSI is generated.

3. After automatic data transfer is stopped, the data address when the transfer stopped is stored in automatic data transfer address count register 0 (ADTC0). However, since no function to restart automatic data transfer is incorporated, when transfer is stopped by setting ATSTP0 = 1, start automatic data transfer by setting ATSTA0 to 1 after re-setting the registers.

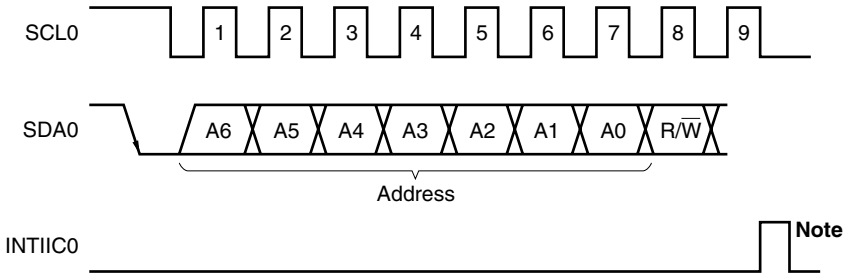
18.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in slave address register 0 (SVA0). If the address data matches the SVA0 register values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 18-14. Address



Note INTIIC0 is not issued if data other than a local address or extension code is received during slave device operation.

The slave address and the eighth bit, which specifies the transfer direction as described in **18.5.3 Transfer direction specification** below, are together written to IIC shift register 0 (IIC0) and are then output. Received addresses are written to IIC0.

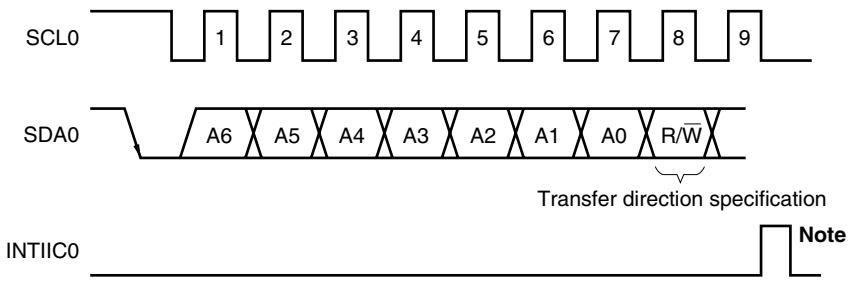
The slave address is assigned to the higher 7 bits of IIC0 register.

18.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of “0”, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of “1”, it indicates that the master device is receiving data from a slave device.

Figure 18-15. Transfer Direction Specification



Note INTIIC0 is not issued if data other than a local address or extension code is received during slave device operation.

Cautions 1. To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.

2. Even if "internal low-speed oscillator can be stopped by software" is selected by the option byte, the internal low-speed oscillation clock continues in the STOP mode in the status before the STOP mode is set. To stop the internal low-speed oscillator's oscillation in the STOP mode, stop it by software and then execute the STOP instruction.

3. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), switch the CPU clock to the internal high-speed oscillation clock before the execution of the STOP instruction using the following procedure.

<1> Set RSTOP to 0 (starting oscillation of the internal high-speed oscillator) → <2> Set MCM0 to 0 (switching the CPU from X1 oscillation to internal high-speed oscillation) → <3> Check that MCS is 0 (checking the CPU clock) → <4> Check that RSTS is 1 (checking internal high-speed oscillation operation) → <5> Execute the STOP instruction

Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

4. If the STOP instruction is executed when AMPH = 1, supply of the CPU clock is stopped for 4.06 to 16.12 μs after the STOP mode is released when the internal high-speed oscillation clock is selected as the CPU clock, or for the duration of 160 external clocks when the high-speed system clock (external clock input) is selected as the CPU clock.

5. Execute the STOP instruction after having confirmed that the internal high-speed oscillator is operating stably (RSTS = 1).

Cautions 3. When using LVI as an interrupt, if LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

4. With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.

(2) Low-voltage detection level selection register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 25-3. Format of Low-Voltage Detection Level Selection Register (LVIS)

Address: FFBFH After reset: 00H[Note 1] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.24 V ±0.1 V)
0	0	0	1	V_{LVI1} (4.09 V ±0.1 V)
0	0	1	0	V_{LVI2} (3.93 V ±0.1 V)
0	0	1	1	V_{LVI3} (3.78 V ±0.1 V)
0	1	0	0	V_{LVI4} (3.62 V ±0.1 V)
0	1	0	1	V_{LVI5} (3.47 V ±0.1 V)
0	1	1	0	V_{LVI6} (3.32 V ±0.1 V)
0	1	1	1	V_{LVI7} (3.16 V ±0.1 V)
1	0	0	0	V_{LVI8} (3.01 V ±0.1 V)
1	0	0	1	V_{LVI9} (2.85 V ±0.1 V)
1	0	1	0	V_{LVI10} (2.70 V ±0.1 V) [Note 2]
1	0	1	1	V_{LVI11} (2.55 V ±0.1 V) [Note 2]
1	1	0	0	V_{LVI12} (2.39 V ±0.1 V) [Note 2]
1	1	0	1	V_{LVI13} (2.24 V ±0.1 V) [Note 2]
1	1	1	0	V_{LVI14} (2.08 V ±0.1 V) [Note 2]
1	1	1	1	V_{LVI15} (1.93 V ±0.1 V) [Note 2]

Notes 1. The value of LVIS is not reset but retained as is, upon a reset by LVI. It is cleared to 00H upon other resets.

2. Do not set V_{LVI10} to V_{LVI15} for (A2) grade products.

Cautions 1. Be sure to clear bits 4 to 7 to "0".

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.

4. With the conventional-specification products (μPD78F05xx and 78F05xxD), after an LVI reset has been generated, do not write values to LVIS and LVIM when LVION = 1.

CHAPTER 27 FLASH MEMORY

The 78K0/Kx2 microcontrollers incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board.

27.1 Internal Memory Size Switching Register

Select the internal memory capacity using the internal memory size switching register (IMS).
IMS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IMS to CFH.

Caution Be sure to set each product to the values shown in Table 27-1 after a reset release.

Figure 27-1. Format of Internal Memory Size Switching Register (IMS)

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

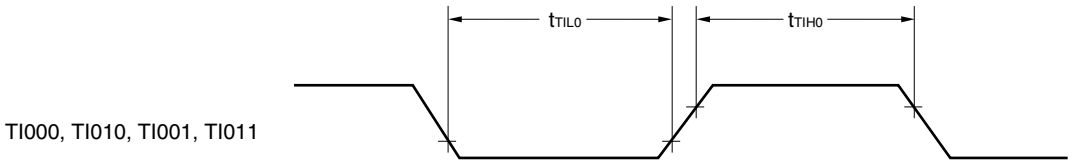
RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	0	0	768 bytes
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

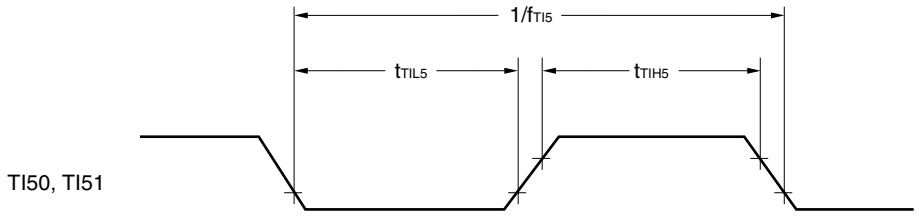
ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	0	1	0	8 KB
0	1	0	0	16 KB
0	1	1	0	24 KB
1	0	0	0	32 KB
1	1	0	0	48 KB
1	1	1	1	60 KB
Other than above				Setting prohibited

Caution To set the memory size, set IMS and then IXS. Set the memory size so that the internal ROM and internal expansion RAM areas do not overlap.

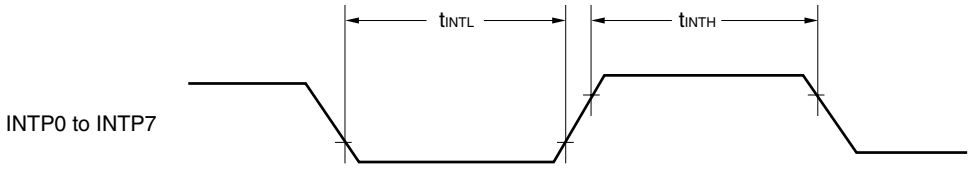
Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

TI Timing

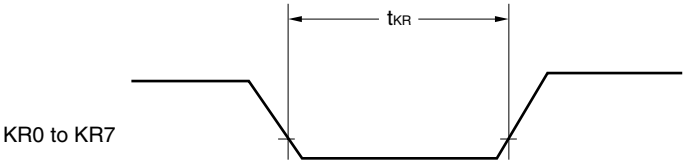




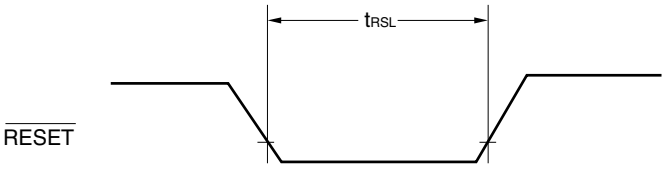
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

LVI Circuit Characteristics (T_A = –40 to +125°C, $V_{POC} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $AV_{REF} \leq V_{DD}$, $V_{SS} = EV_{SS}$ = 0 V)

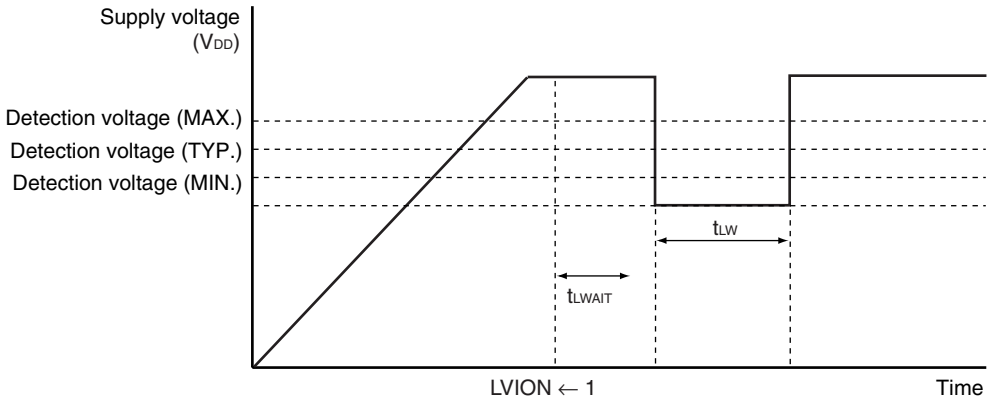
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.14	4.24	4.34	V
		V_{LVI1}		3.99	4.09	4.19	V
		V_{LVI2}		3.83	3.93	4.03	V
		V_{LVI3}		3.68	3.78	3.88	V
		V_{LVI4}		3.52	3.62	3.72	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.06	3.16	3.26	V
		V_{LVI8}		2.91	3.01	3.11	V
		V_{LVI9}		2.75	2.85	2.95	V
	External input pin[Note 1]	EXLVI	EXLVI < V_{DD}, 2.7 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note 2]		t_{LWAIT}		10			μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 9

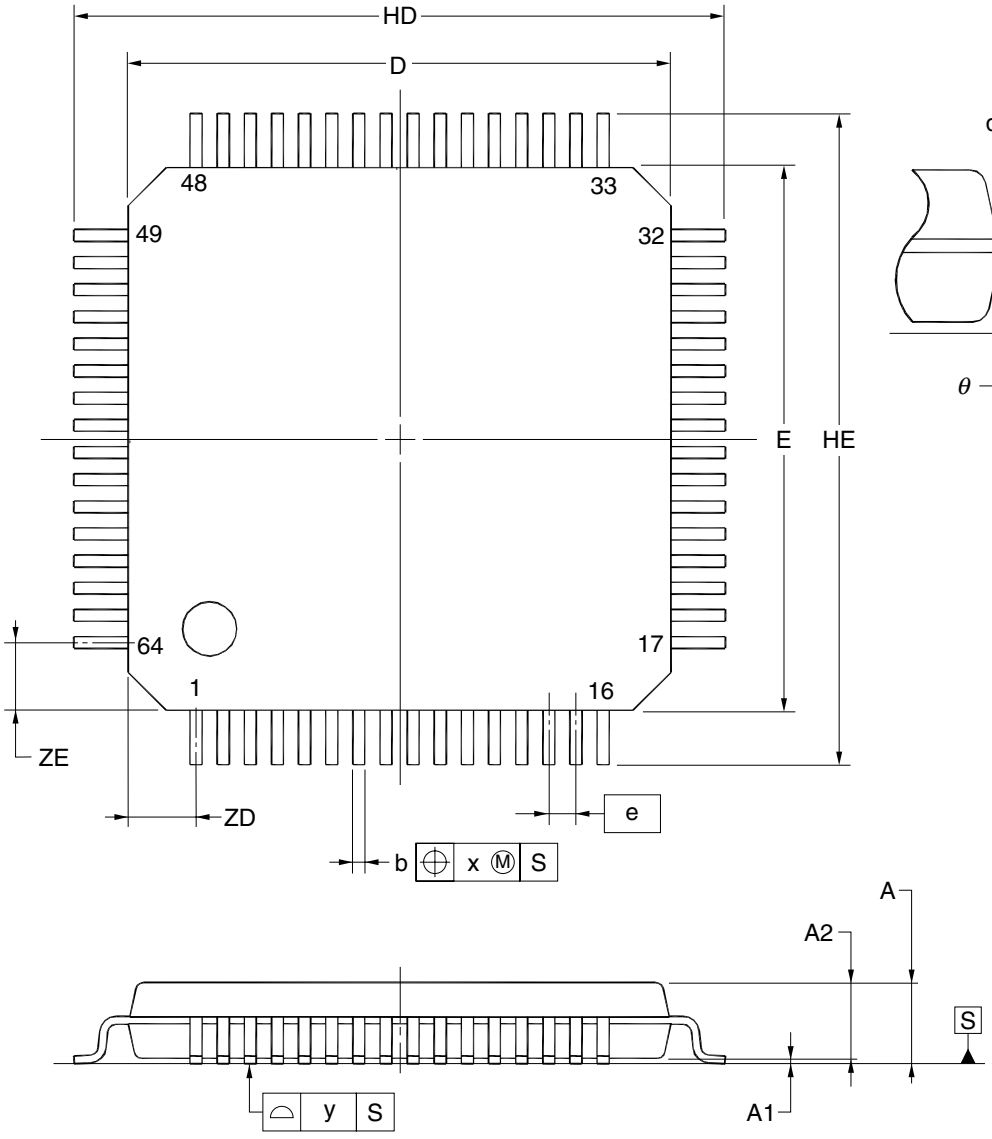
LVI Circuit Timing



34.4 78K0/KE2

- μPD78F0531GB-UEU-A, 78F0532GB-UEU-A, 78F0533GB-UEU-A, 78F0534GB-UEU-A, 78F0535GB-UEU-A, 78F0536GB-UEU-A, 78F0537GB-UEU-A, 78F0537DGB-UEU-A

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.55}_{-0.45}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P64GB-50-UEU

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.