Renesas Electronics America Inc - UPD78F0537AGK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0537agk-gaj-ax

4.4.3 Subroutine call between memory banks

Subroutines cannot be directly called between memory banks.

To call a subroutine between memory banks, branch once to the common area (0000H to 7FFFH), specify the memory bank at the calling destination by using the BANK register there, execute the CALL instruction, and branch to the call destination by that instruction.

At this time, save the current value of the BANK register to RAM. Restore the value of the BANK register before executing the RET instruction.

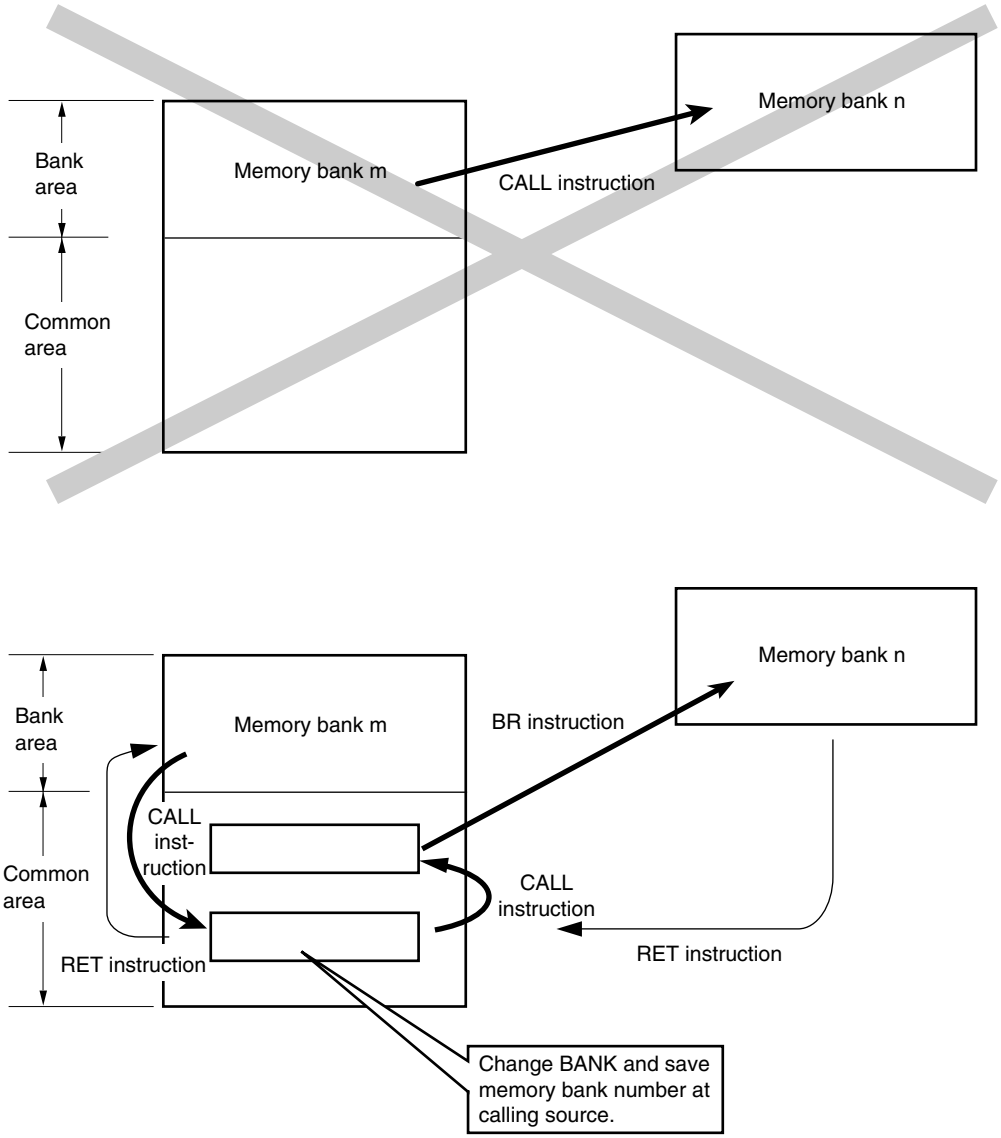
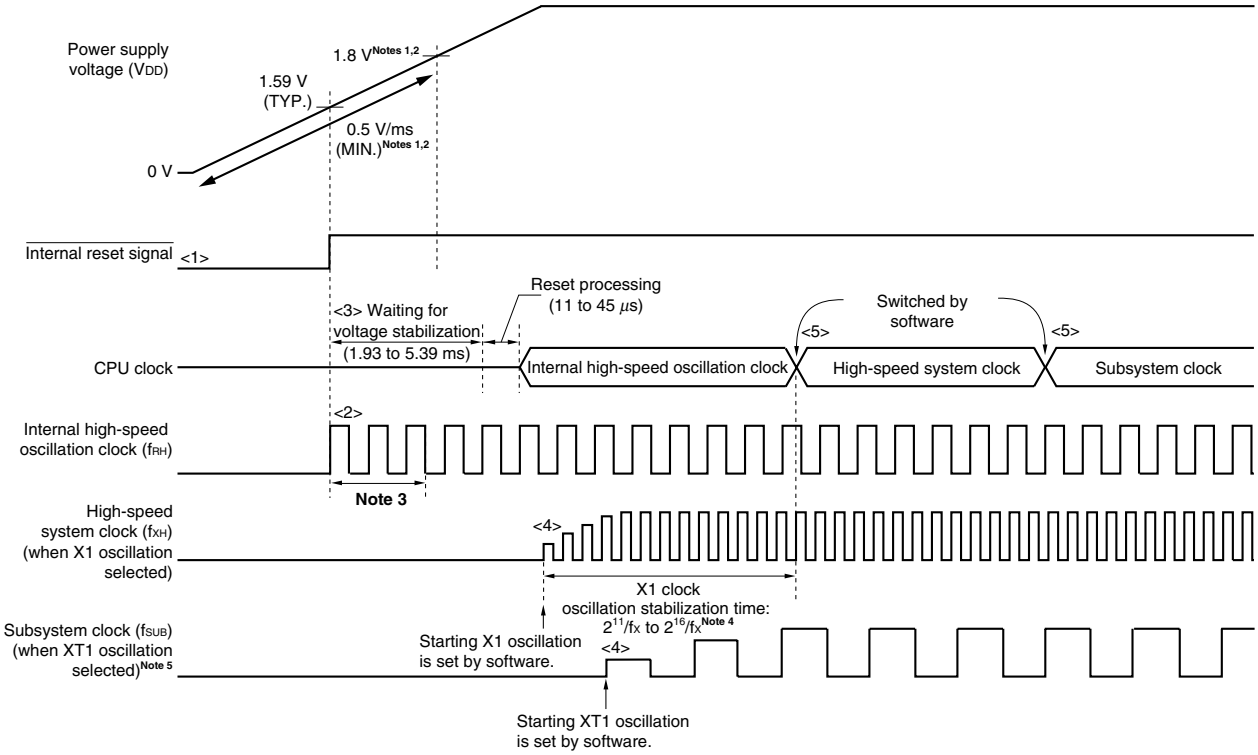


Figure 6-15. Clock Generator Operation When Power Supply Voltage Is Turned On (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.59 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> When the power supply voltage rises with a slope of 0.5 V/ms (MIN.), the CPU starts operation on the internal high-speed oscillation clock after the reset is released and after the stabilization times for the voltage of the power supply and regulator have elapsed, and then reset processing is performed.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **(1)** in **6.6.1 Example of controlling high-speed system clock** and **(1)** in **6.6.3 Example of controlling subsystem clock)**.

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **(3)** in **6.6.1 Example of controlling high-speed system clock** and **(3)** in **6.6.3 Example of controlling subsystem clock**).

Notes 1. With standard and (A) grade products, if the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 1.8 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 1.8 V, or set the 2.7 V/1.59 V POC mode by using the option byte (POCMODE = 1) (see **Figure 6-16**). When a low level has been input to the $\overline{\text{RESET}}$ pin until the voltage reaches 1.8 V, the CPU operates with the same timing as <2> and thereafter in Figure 6-15, after the reset has been released by the $\overline{\text{RESET}}$ pin.

2. With (A2) grade products, if the voltage rises with a slope of less than 0.75 V/ms (MIN.) from power application until the voltage reaches 2.7 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 2.7 V. When a low level has been input to the $\overline{\text{RESET}}$ pin until the voltage reaches 2.7 V, the CPU operates with the same timing as <2> and thereafter in Figure 6-15, after the reset has been released by the $\overline{\text{RESET}}$ pin.

3. The internal voltage stabilization time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

Remark 2. When switching the CPU clock from the main system clock to the subsystem clock, calculate the number of clocks by rounding up to the next clock and discarding the decimal portion, as shown below.

Example When switching CPU clock from $f_{XP}/2$ to $f_{SUB}/2$ (@ oscillation with f_{XP} = 10 MHz, f_{SUB} = 32.768 kHz)

f_{XP}/f_{SUB} = 10000/32.768 ≅ 305.1 → 306 clocks

By setting bit 0 (MCM0) of the main clock mode register (MCM), the main system clock can be switched (between the internal high-speed oscillation clock and the high-speed system clock).

The actual switchover operation is not performed immediately after rewriting to MCM0; operation continues on the pre-switchover clock for several clocks (see **Table 6-10**).

Whether the CPU is operating on the internal high-speed oscillation clock or the high-speed system clock can be ascertained using bit 1 (MCS) of MCM.

Table 6-10. Maximum Time Required for Main System Clock Switchover

Set Value Before Switchover	Set Value After Switchover	
MCM0	MCM0	
	0	1
0		1 + $2f_{RH}/f_{XH}$ clock
1	1 + $2f_{XH}/f_{RH}$ clock	

Cautions 1. When switching the internal high-speed oscillation clock to the high-speed system clock, bit 2 (XSEL) of MCM must be set to 1 in advance. The value of XSEL can be changed only once after a reset release.

2. Do not rewrite MCM0 when the CPU clock operates with the subsystem clock.

Remarks 1. The number of clocks listed in Table 6-10 is the number of main system clocks before switchover.

2. Calculate the number of clocks in Table 6-10 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{RH} = 8 MHz, f_{XH} = 10 MHz)

1 + $2f_{RH}/f_{XH}$ = 1 + 2 × 8/10 = 1 + 2 × 0.8 = 1 + 1.6 = 2.6 → 2 clocks

6.6.10 Peripheral hardware and source clocks

The following lists peripheral hardware and source clocks incorporated in the 78K0/Kx2 microcontrollers.

Remark The peripheral hardware depends on the product. See **1.7 Block Diagram** and **1.8 Outline of Functions**.

Table 6-13. Peripheral Hardware and Source Clocks

Peripheral Hardware \ Source Clock		Peripheral Hardware Clock (f_{PRS})	Subsystem Clock (f_{SUB})[Note 1]	Internal Low-Speed Oscillation Clock (f_{RL})	TM50 Output	External Clock from Peripheral Hardware Pins
16-bit timer/ event counter	00	Y	N	N	N	Y (TI000 pin)[Note 2]
	01	Y	N	N	N	Y (TI001 pin)[Note 2]
8-bit timer/ event counter	50	Y	N	N	N	Y (TI50 pin)[Note 2]
	51	Y	N	N	N	Y (TI51 pin)[Note 2]
8-Bit timer	H0	Y	N	N	Y	N
	H1	Y	N	Y	N	N
Watch timer		Y	Y	N	N	N
Watchdog timer		N	N	Y	N	N
Buzzer output		Y	N	N	N	N
Clock output		Y	Y	N	N	N
A/D converter		Y	N	N	N	N
Serial interface	UART0	Y	N	N	Y	N
	UART6	Y	N	N	Y	N
	CSI10	Y	N	N	N	Y ($\overline{SCK10}$ pin)[Note 2]
	CSI11	Y	N	N	N	Y ($\overline{SCK11}$ pin)[Note 2]
	CSIA0	Y	N	N	N	Y ($\overline{SCKA0}$ pin)[Note 2]
	IIC0	Y	N	N	N	Y (EXSCL0, SCL0 pin)[Note 2]

Notes 1. The 78K0/KB2 is not provided with a subsystem clock.

2. Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Remark Y: Can be selected, N: Cannot be selected

Table 7-2. Capture Operation of CR00n and CR01n

External Input Signal / Capture Operation	TI00n Pin Input		TI01n Pin Input	
Capture operation of CR00n	CRC0n1 = 1 TI00n pin input (reverse phase)	Set values of ES0n1 and ES0n0 Position of edge to be captured	CRC0n1 bit = 0 TI01n pin input	Set values of ES1n1 and ES1n0 Position of edge to be captured
		01: Rising		01: Rising
		00: Falling		00: Falling
		11: Both edges (cannot be captured)		11: Both edges
	Interrupt signal	INTTM00n signal is not generated even if value is captured.	Interrupt signal	INTTM00n signal is generated each time value is captured.
Capture operation of CR01n	TI00n pin input[Note]	Set values of ES0n1 and ES0n0 Position of edge to be captured		
		01: Rising		
		00: Falling		
		11: Both edges		
	Interrupt signal	INTTM01n signal is generated each time value is captured.		

Note The capture operation of CR01n is not affected by the setting of the CRC0n1 bit.

Caution To capture the count value of the TM0n register to the CR00n register by using the phase reverse to that input to the TI00n pin, the interrupt request signal (INTTM00n) is not generated after the value has been captured. If the valid edge is detected on the TI01n pin during this operation, the capture operation is not performed but the INTTM00n signal is generated as an external interrupt signal. To not use the external interrupt, mask the INTTM00n signal.

Remarks 1. CRC0n1: See **7.3 (2) Capture/compare control register 0n (CRC0n)**.
ES1n1, ES1n0, ES0n1, ES0n0: See **7.3 (4) Prescaler mode register 0n (PRM0n)**.

2. n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(3) 16-bit timer output control register 0n (TOC0n)

TOC0n is an 8-bit register that controls the TO0n output.

TOC0n can be rewritten while only OSPT0n is operating (when TMC0n3 and TMC0n2 = other than 00). Rewriting the other bits is prohibited during operation.

However, TOC0n4 can be rewritten during timer operation as a means to rewrite CR01n (see **7.5.1 Rewriting CR01n during TM0n operation**).

TOC0n can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TOC0n to 00H.

Caution Be sure to set TOC0n using the following procedure.

<1> Set TOC0n4 and TOC0n1 to 1.

<2> Set only TOE0n to 1.

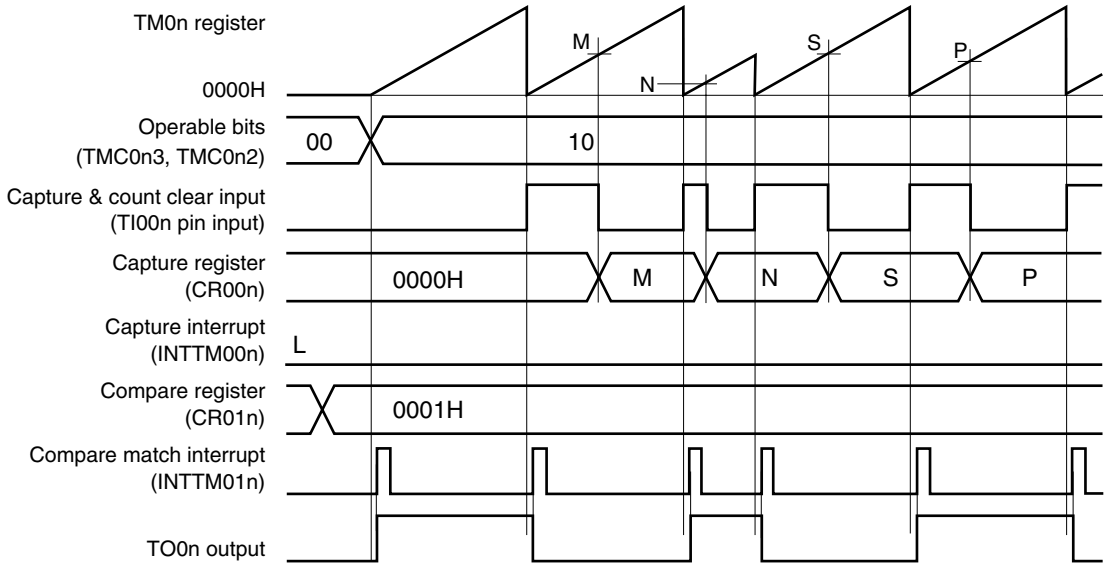
<3> Set either of LVS0n or LVR0n to 1.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-32. Timing Example of Clear & Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register, CR01n: Compare Register) (1/2)

(a) TOC0n = 13H, PRM0n = 10H, CRC0n, = 03H, TMC0n = 08H, CR01n = 0001H



This is an application example where the TO0n output level is to be inverted when the count value has been captured & cleared.

TM0n is cleared at the rising edge detection of the TI00n pin and it is captured to CR00n at the falling edge detection of the TI00n pin.

When bit 1 (CRC0n1) of capture/compare control register 0n (CRC0n) is set to 1, the count value of TM0n is captured to CR00n in the phase reverse to that of the signal input to the TI00n pin, but the capture interrupt signal (INTTM00n) is not generated. However, the INTTM00n signal is generated when the valid edge of the TI01n pin is detected. Mask the INTTM00n signal when it is not used.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(7) Operation of OVF0n flag

(a) Setting OVF0n flag (1)

The OVF0n flag is set to 1 in the following case, as well as when TM0n overflows.

Select the clear & start mode entered upon a match between TM0n and CR00n.

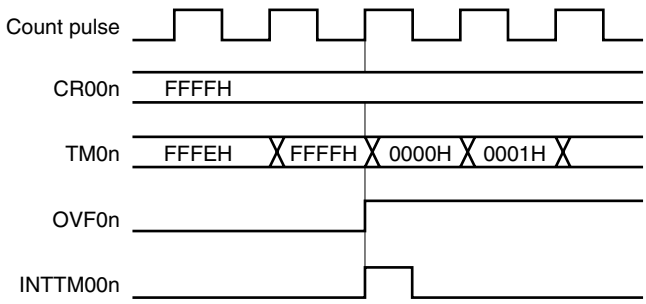
↓

Set CR00n to FFFFH.

↓

When TM0n matches CR00n and TM0n is cleared from FFFFH to 0000H

Figure 7-62. Operation Timing of OVF0n Flag



(b) Clearing OVF0n flag

Even if the OVF0n flag is cleared to 0 after TM0n overflows and before the next count clock is counted (before the value of TM0n becomes 0001H), it is set to 1 again and clearing is invalid.

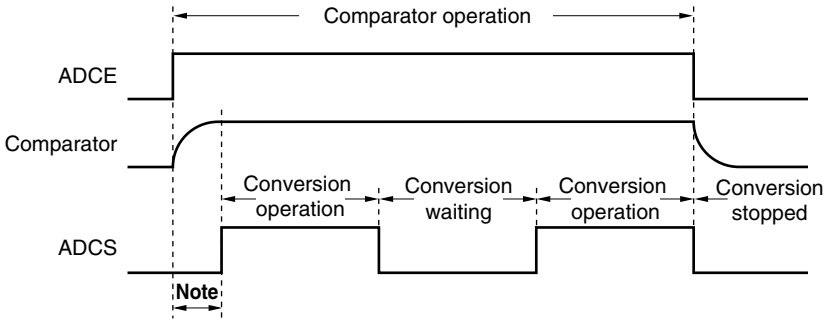
(8) One-shot pulse output

One-shot pulse output operates correctly in the free-running timer mode or the clear & start mode entered by the TI00n pin valid edge. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM0n and CR00n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 13-4. Timing Chart When Comparator Is Used



Note To stabilize the internal circuit, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 μs or longer.

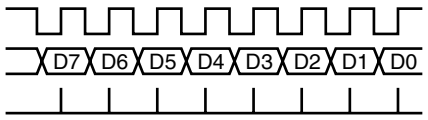
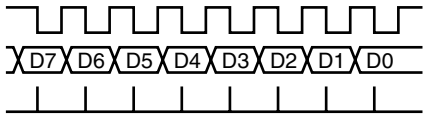
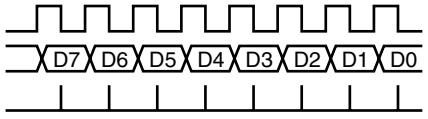
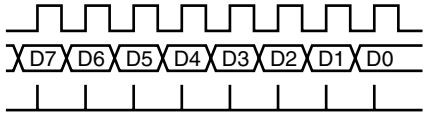
Cautions 1. A/D conversion must be stopped before rewriting bits FR0 to FR2, LV1, and LV0 to values other than the identical data.

2. If data is written to ADM, a wait cycle is generated. Do not write data to ADM when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

Figure 16-6. Format of Serial Clock Selection Register 11 (CSIC11)

Address: FF89H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CSIC11	0	0	0	CKP11	DAP11	CKS112	CKS111	CKS110

CKP11	DAP11	Specification of data transmission/reception timing	Type
0	0		1
0	1		2
1	0		3
1	1		4

CKS112	CKS111	CKS110	CSI11 serial clock selection[Notes 1, 2]				Mode
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz	
0	0	0	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz	Setting prohibited	Master mode
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	
0	1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	
0	1	1	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	
1	0	0	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz	625 kHz	
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz	
1	1	0	$f_{PRS}/2^7$	15.63 kHz	39.06 kHz	78.13 kHz	156.25 kHz	
1	1	1	External clock input from $\overline{SCK11}$[Note 3]					Slave mode

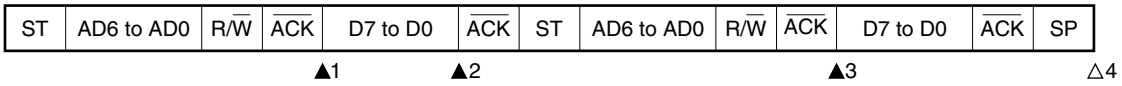
Note 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when $f_{PRS} = f_{XH}$ (XSEL = 1).)

(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))

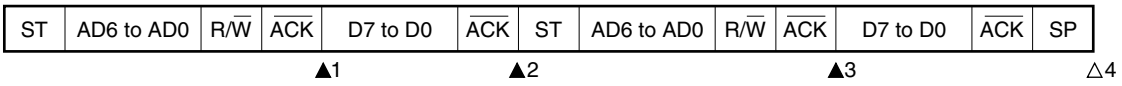


▲1 ▲2 ▲3 △4

▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001×000B
▲3: IICS0 = 00000110B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))



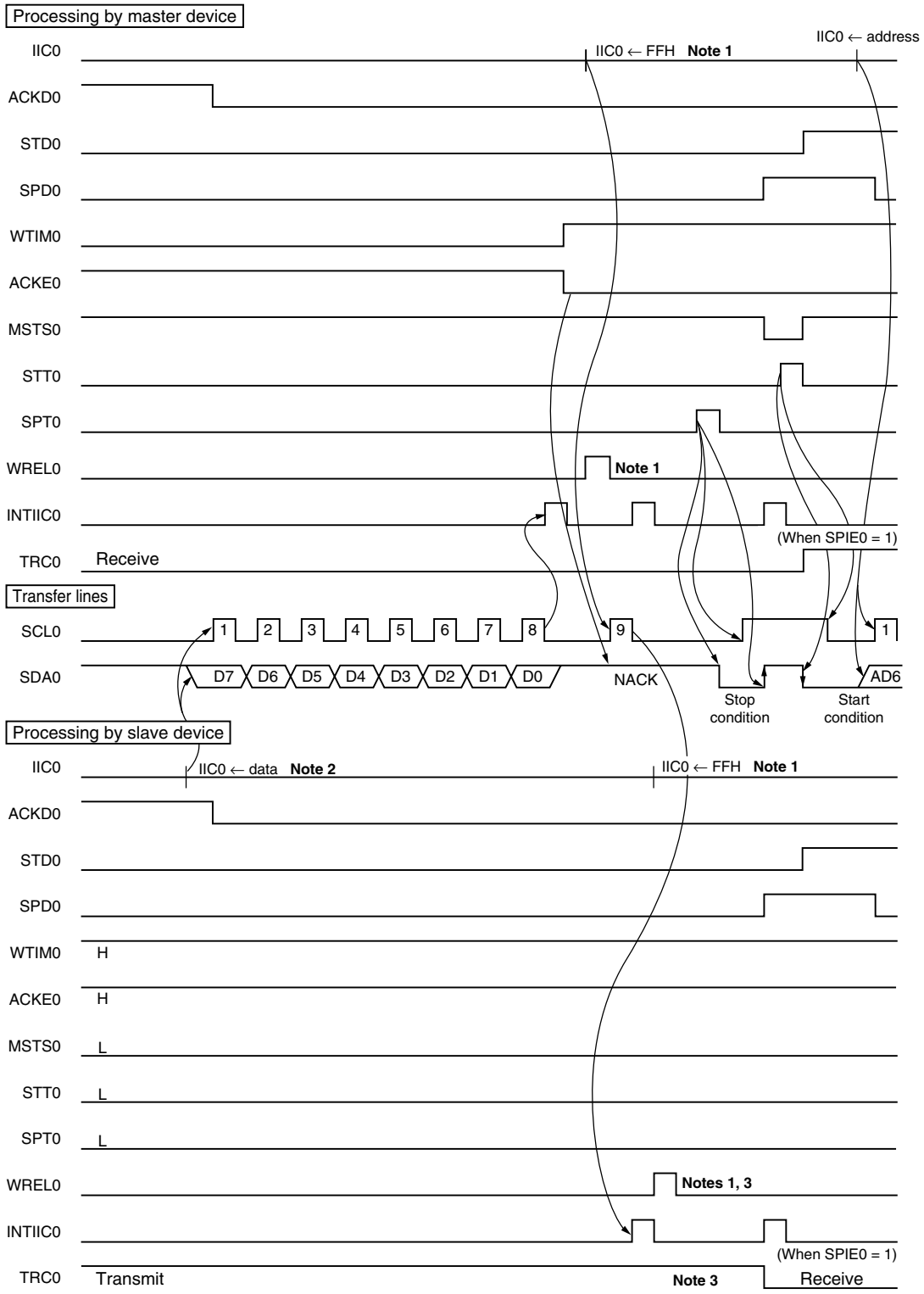
▲1 ▲2 ▲3 △4

▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001××00B
▲3: IICS0 = 00000110B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 18-28. Example of Slave to Master Communication
(When 8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Stop condition



Notes 1. To cancel wait, write “FFH” to IIC0 or set WREL0.

2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

3. If a wait state during slave transmission is canceled by setting WREL0, TRC0 will be cleared.

20.4.4 Interrupt request hold

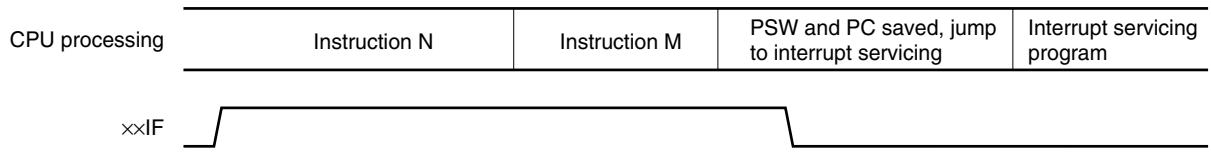
There are instructions where, even if an interrupt request is issued for them while another instruction is being executed, request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV A, PSW
- MOV PSW, A
- MOV1 PSW. bit, CY
- MOV1 CY, PSW. bit
- AND1 CY, PSW. bit
- OR1 CY, PSW. bit
- XOR1 CY, PSW. bit
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- PUSH PSW
- POP PSW
- BT PSW. bit, $addr16
- BF PSW. bit, $addr16
- BTCLR PSW. bit, $addr16
- EI
- DI
- Manipulation instructions for the IF0L, IF0H, IF1L, IF1H, MK0L, MK0H, MK1L, MK1H, PR0L, PR0H, PR1L, and PR1H registers.

Caution The BRK instruction is not one of the above-listed interrupt request hold instructions. However, the software interrupt activated by executing the BRK instruction causes the IE flag to be cleared. Therefore, even if a maskable interrupt request is generated during execution of the BRK instruction, the interrupt request is not acknowledged.

Figure 20-23 shows the timing at which interrupt requests are held pending.

Figure 20-23. Interrupt Request Hold



Remarks 1. Instruction N: Interrupt request hold instruction

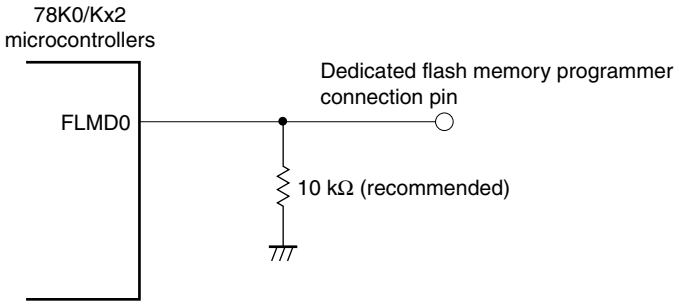
2. Instruction M: Instruction other than interrupt request hold instruction

3. The ××PR (priority level) values do not affect the operation of ××IF (interrupt request).

27.6.1 FLMD0 pin

In the normal operation mode, 0 V is input to the FLMD0 pin. In the flash memory programming mode, the V_{DD} write voltage is supplied to the FLMD0 pin. An FLMD0 pin connection example is shown below.

Figure 27-6. FLMD0 Pin Connection Example



27.6.2 Serial interface pins

The pins used by each serial interface are listed below.

Table 27-5. Pins Used by Each Serial Interface

Serial Interface	Pins Used
CSI10	SO10, SI10, $\overline{SCK10}$
UART6	TxD6, RxD6

To connect the dedicated flash memory programmer to the pins of a serial interface that is connected to another device on the board, care must be exercised so that signals do not collide or that the other device does not malfunction.

(2) Non-port functions

Port		78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
		30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Power supply, ground		V_{DD}, EV_{DD}[Note 1], V_{SS}, EV_{SS}[Note 1], AV_{REF}, AV_{SS}	V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, V_{SS}, EV_{SS}, AV_{REF}, AV_{SS}	
Regulator		REGC						
Reset		$\overline{\text{RESET}}$						
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK, EXCLKS					
Writing to flash memory		FLMD0						
Interrupt		INTP0 to INTP5			INTP0 to INTP6		INTP0 to INTP7	
Key interrupt		–	KR0, KR1	KR0 to KR3		KR0 to KR7		
Timer	TM00	TI000, TI010, TO00						
	TM01	–					TI001[Note 2], TI011[Note 2], TO01[Note 2]	
	TM50	TI50, TO50						
	TM51	TI51, TO51						
	TMH0	TOH0						
	TMH1	TOH1						
Serial interface	UART0	RxD0, TxD0						
	UART6	RxD6, TxD6						
	IIC0	SCL0, SDA0	SCL0, SDA0, EXSCL0					
	CSI10	$\overline{\text{SCK10}}$, SI10, SO10						
	CSI11	–					$\overline{\text{SCK11}}$[Note 2], SI11[Note 2], SO11[Note 2], $\overline{\text{SSI11}}$[Note 2]	
	CSIA0	–						$\overline{\text{SCKA0}}$, SIA0, SOA0, BUSY0, STB0
A/D converter		ANI0 to ANI3	ANI0 to ANI5	ANI0 to ANI7				
Clock output		–			PCL			
Buzzer output		–					BUZ	
Low-voltage detector (LVI)		EXLVI						

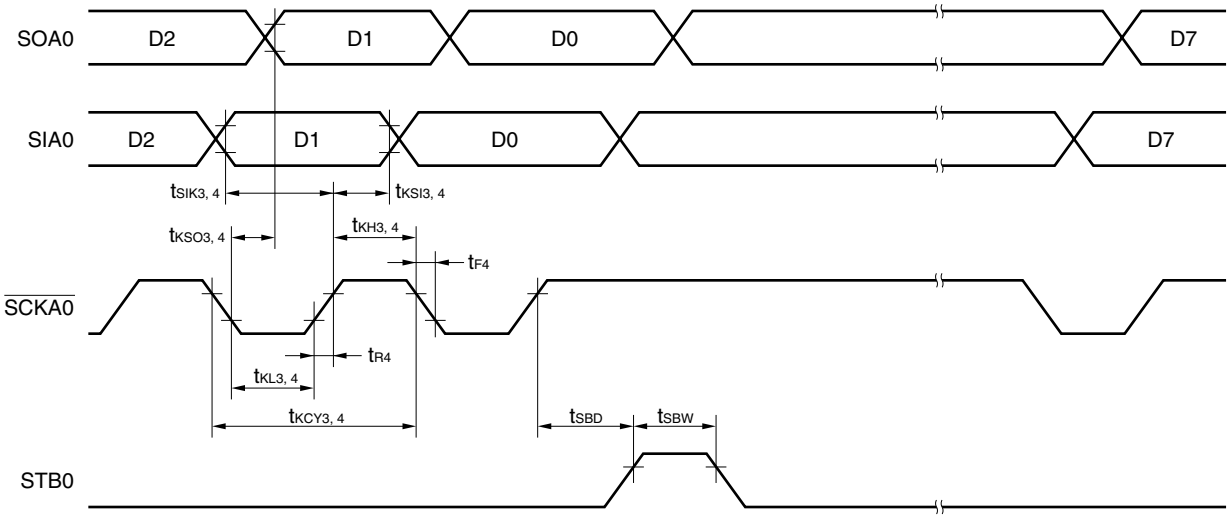
Notes 1. This is not mounted onto 30-pin products.

2. This is not mounted onto the 78K0/KE2 products whose flash memory is less than 32 KB.

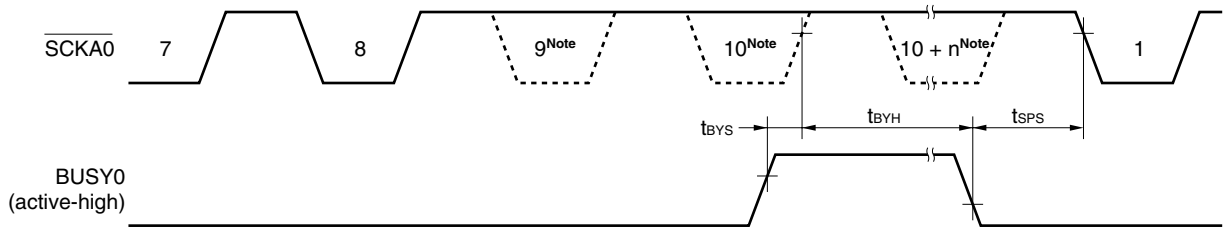
Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Serial Transfer Timing (2/2)

CSIA0:



CSIA0 (busy processing):

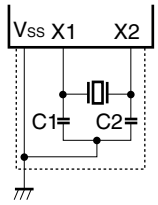


Note SCKA0 does not become low level here, but the timing is illustrated so that the timing specifications can be shown.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

X1 Oscillator Characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
Ceramic resonator, Crystal resonator		X1 clock oscillation frequency (f_X)Note 1	Conventional-specification Products (μPD78F05xx (A2))	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0Note 2		20.0	MHz
				2.7 V ≤ V_{DD} < 4.0 V	1.0Note 2		10.0	
			Expanded-specification Products (μPD78F05xxA(A2))		1.0Note 2		20.0	MHz

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

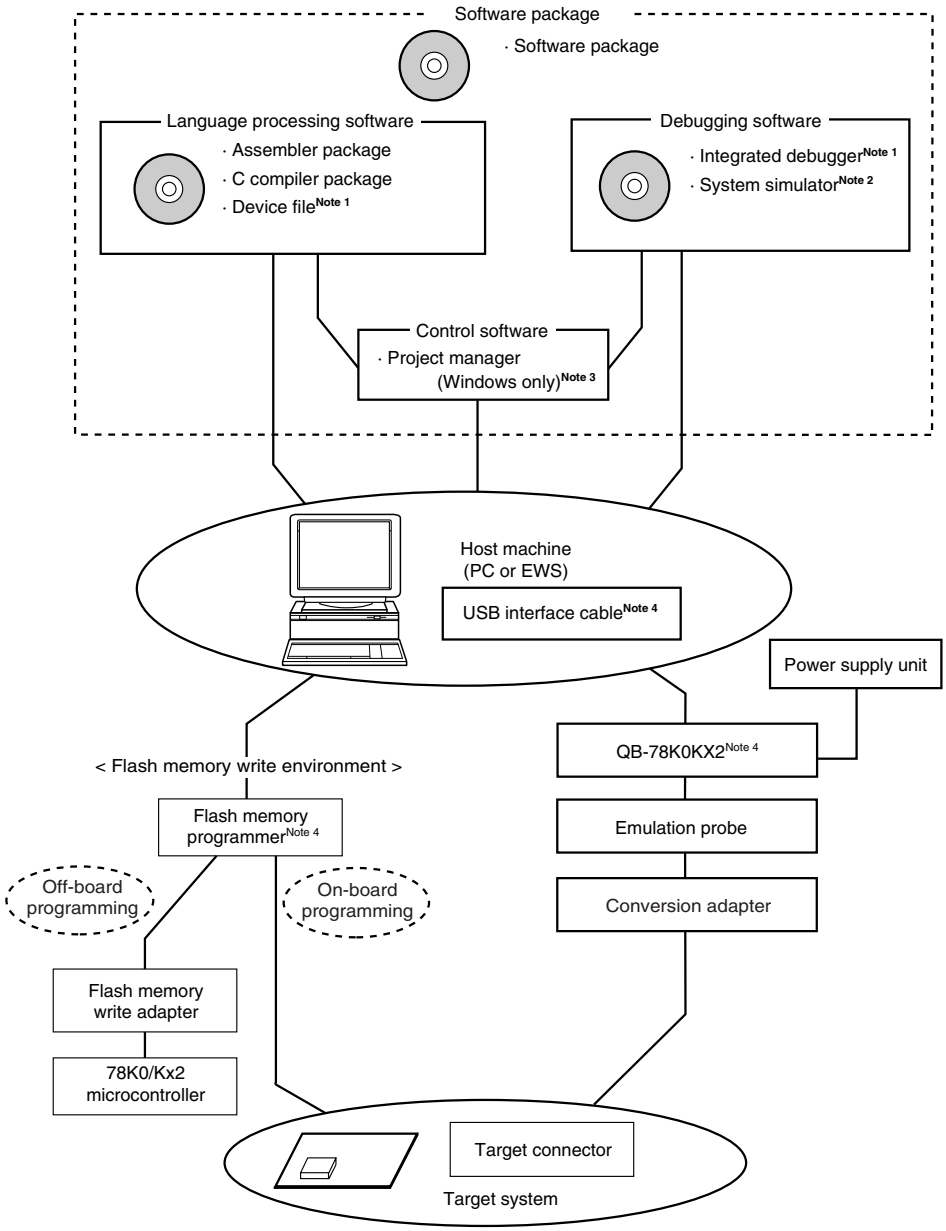
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Figure A-1. Development Tool Configuration (1/2)

(1) When using the in-circuit emulator QB-78K0KX2



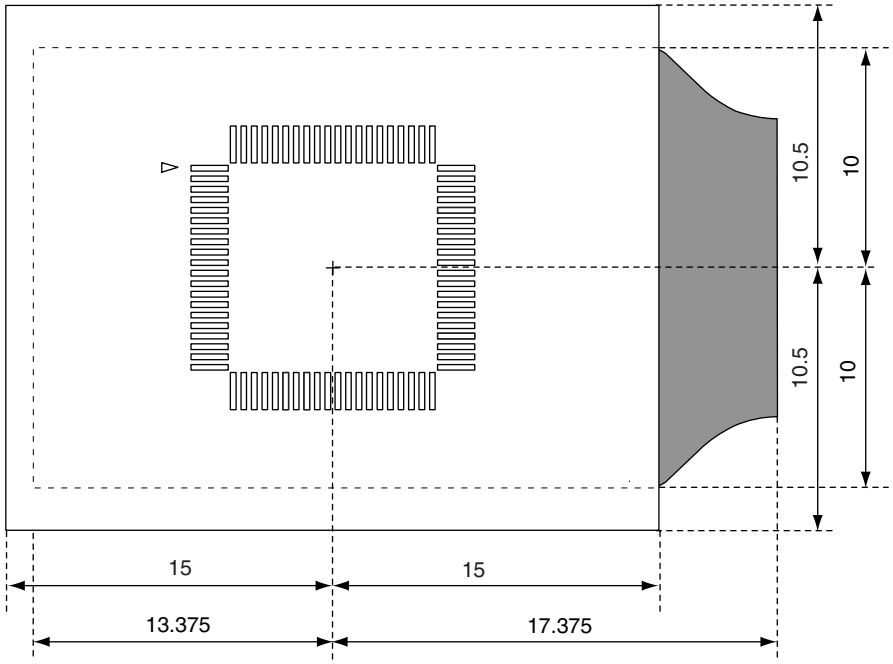
Notes 1. Download the device file for 78K0/Kx2 microcontrollers (DF780547) and the integrated debugger ID78K0-QB from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).

2. SM+ for 78K0 (instruction simulation version) is included in the software package. SM+ for 78K0/Kx2 (instruction + peripheral simulation version) is not included.

3. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows™.

4. QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator with programming function QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Any other products are sold separately.

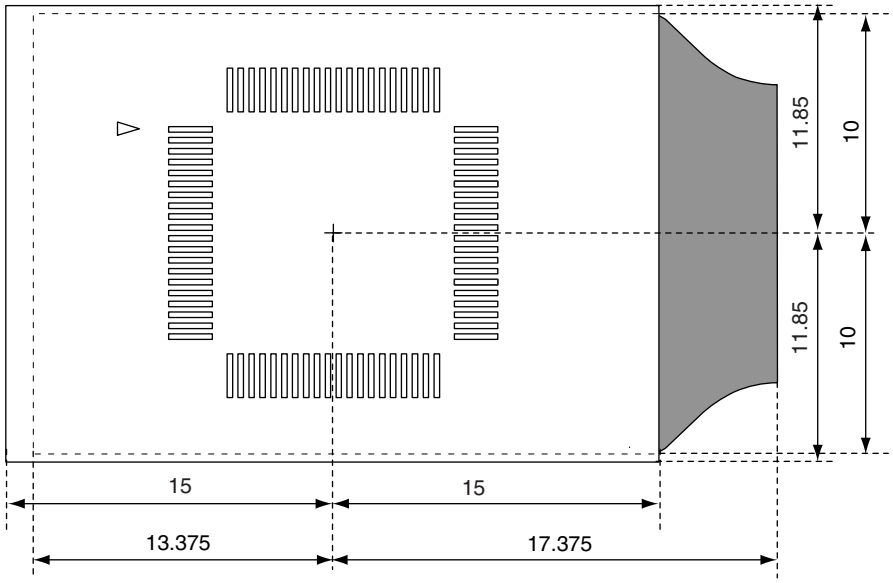
Figure B-8. For 64-Pin GB Package



□ : Exchange adapter area: Components up to 17.45 mm in height can be mounted[Note]
■ : Emulation probe tip area: Components up to 24.45 mm in height can be mounted[Note]

Note Height can be adjusted by using space adapters (each adds 2.4 mm)

Figure B-9. For 64-Pin GC Package



□ : Exchange adapter area: Components up to 17.45 mm in height can be mounted[Note]
■ : Emulation probe tip area: Components up to 24.45 mm in height can be mounted[Note]

Note Height can be adjusted by using space adapters (each adds 2.4 mm)

APPENDIX E REVISION HISTORY

E.1 Major Revisions in This Edition

Page	Description	Classification
R01UH0008EJ0400 → R01UH0008EJ0401		
pp. 97, 396, 399, 722, 723	Deletion of **Note**	(c)
p. 93	Change of Recommended Connection of Unused Pins of FLMD0 pin in **Table 2-3. Pin I/O Circuit Types**	(a)
p. 135	Change of **Note 2** of **Table 3-8. Special Function Register List (5/5)**	(c)
U18598JJ3V0UD00 → R01UH0008EJ0400		
Throughout	Deletion of "**recommended**" from **Caution** "**Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: recommended).**"	(c)
CHAPTER 1 OUTLINE		
p. 41	Change of status of **64-pin plastic FBGA (4x4)** of **78K0/KE2** from under development to mass production	(b)
CHAPTER 2 PIN FUNCTIONS		
p. 69	Change of **2. 1. 3 78K0/KD2 (2) Non-port functions: 78K0/KD2**	(c)
pp. 72, 73	Change of **2. 1. 4 78K0/KE2 (2) Non-port functions: 78K0/KE2**	(c)
p. 93	Change of **Table 2-3. Pin I/O Circuit Types (3/3)**	(c)
CHAPTER 6 CLOCK GENERATOR		
p. 230	Change of **Caution 2** in **Figure 6-3. Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KB2)**	(a)
p. 231	Change of **Caution 2** in **Figure 6-4. Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)**	(a)
p. 259	Change of **Figure 6-18. CPU Clock Status Transition Diagram (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0), 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)**	(c)
CHAPTER 7 16-BIT TIMER/EVENT COUNTERS 00 AND 01		
p. 299	Change of **Caution** in **7.4.4 Operation in clear & start mode entered by TI00n pin valid edge input**	(c)
CHAPTER 18 SERIAL INTERFACE IIC0		
p. 553	Addition of **Caution** to **Figure 18-3. Format of IIC Shift Register 0 (IIC0)**	(c)
p. 553	Change of description of **18.2 (2) Slave address register 0 (SVA0)**	(c)
p. 557	Addition of **Note** to **Figure 18-5. Format of IIC Control Register 0 (IICC0) (1/4)** and change of **Caution**	(c)
p. 559	Change of **Figure 18-5. Format of IIC Control Register 0 (IICC0) (3/4)**	(c)
p. 560	Change of **Figure 18-5. Format of IIC Control Register 0 (IICC0) (4/4)**	(c)
p. 562	Change of **Figure 18-6. Format of IIC Status Register 0 (IICS0) (2/3)**	(c)
CHAPTER 20 INTERRUPT FUNCTIONS		
p. 634	Change of **(C) External maskable interrupt (INTKR)** in **Figure 20-1 Basic Configuration of Interrupt Function**	(c)
CHAPTER 22 STANDBY FUNCTION		
p. 673	Addition of **Note** to **Figure 22-4. HALT Mode Release by Reset**	(c)
p. 680	Addition of **Note** to **Figure 22-7. STOP Mode Release by Reset**	(c)
CHAPTER 27 FLASH MEMORY		
p. 730	Change of description of **27.6.5 REGC pin**	(c)
p. 755	Addition of **27.11 Creating ROM Code to Place Order for Previously Written Product**	(c)
APPENDIX E REVISION HISTORY		
p. 975	Addition of **C.2 Revision History of Preceding Editions**	(c)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents