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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0544agc-gad-ax

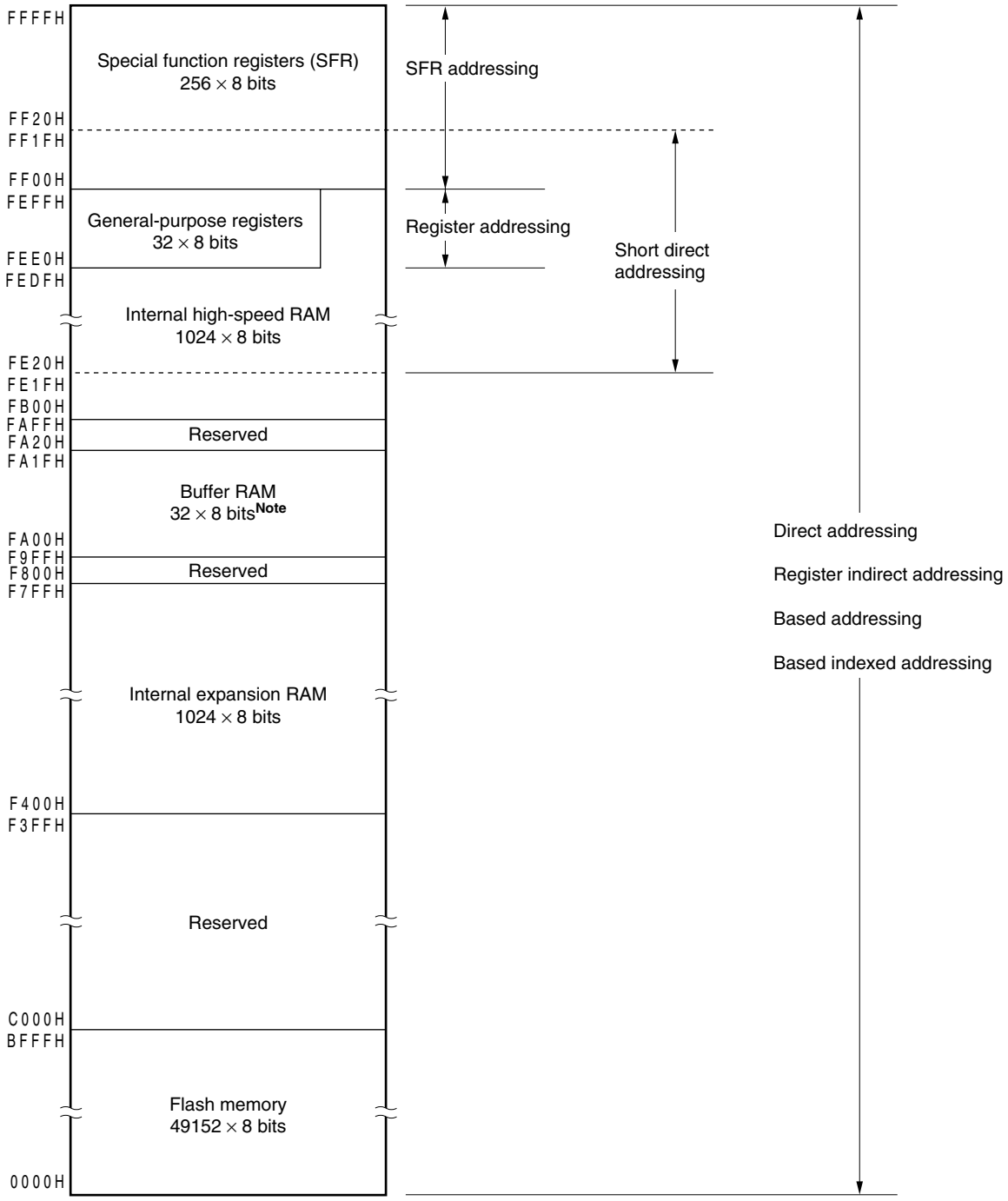
Table 3-2. Set Values of Internal Memory Size Switching Register (IMS) and Internal Expansion RAM Size Switching Register (IXS) (48-pin products of the 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)

48-pin products of the 78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2	IMS	IXS	ROM Capacity	Internal High-Speed RAM Capacity	Internal Expansion RAM Capacity
μPD78F0511, 78F0511A	μPD78F0521, 78F0521A	μPD78F0531, 78F0531A	–	04H	0CH	16 KB	768 bytes	–
μPD78F0512, 78F0512A	μPD78F0522, 78F0522A	μPD78F0532, 78F0532A	–	C6H	0CH	24 KB	1 KB	–
μPD78F0513, 78F0513A	μPD78F0523, 78F0523A	μPD78F0533, 78F0533A	–	C8H	0CH	32 KB	1 KB	–
μPD78F0514, 78F0514A	μPD78F0524, 78F0524A	μPD78F0534, 78F0534A	μPD78F0544, 78F0544A	CCH	0AH	48 KB	1 KB	1 KB
μPD78F0515, 78F0515A, 78F0515D[Note 1], 78F0515DA[Note 1]	μPD78F0525, 78F0525A	μPD78F0535, 78F0535A	μPD78F0545, 78F0545A	CFH	08H	60 KB		2 KB
–	μPD78F0526, 78F0526A	μPD78F0536, 78F0536A	μPD78F0546, 78F0546A	CCH[Note 2]	04H	96 KB[Note 2]		4 KB
–	μPD78F0527, 78F0527A, 78F0527D[Note 1], 78F0527DA[Note 1]	μPD78F0537, 78F0537A, 78F0537D[Note 1], 78F0537DA[Note 1]	μPD78F0547, 78F0547A, 78F0547D[Note 1], 78F0547DA[Note 1]	CCH[Note 2]	00H	128 KB[Note 2]		6 KB

Notes 1. The ROM and RAM capacities of the products with the on-chip debug function can be debugged according to the debug target products. Set IMS and IXS according to the debug target products.

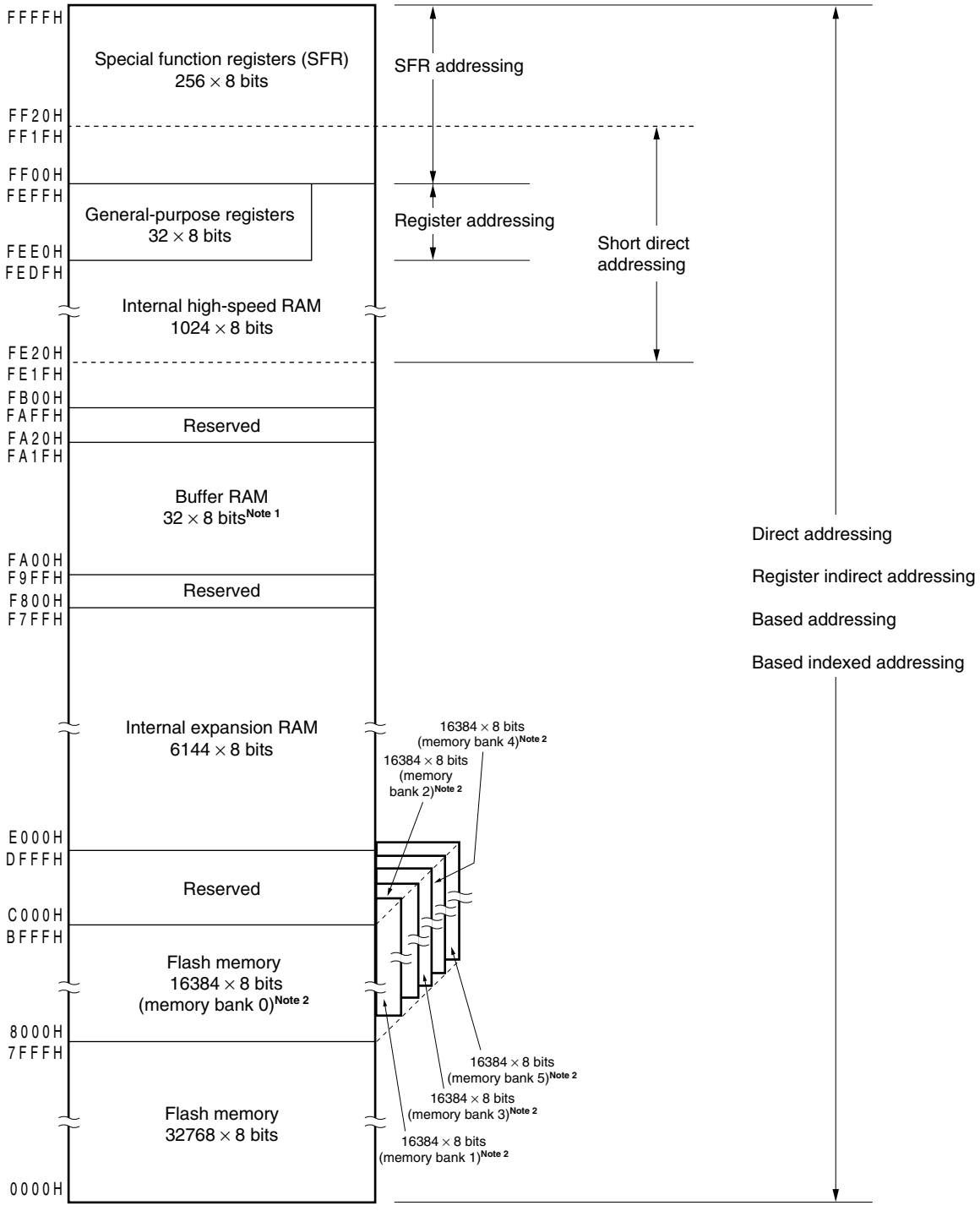
2. The μPD78F05x6 and 78F05x6A (x = 2 to 4) have internal ROMs of 96 KB, and the μPD78F05x7, 78F05x7A, 78F05x7D and 78F05x7DA (x = 2 to 4) have those of 128 KB. However, the set value of IMS of these devices is the same as those of the 48 KB product because memory banks are used. For how to set the memory banks, see **4.3 Memory Bank Select Register (BANK)**.

Figure 3-16. Correspondence Between Data Memory and Addressing
(μPD78F0514, 78F0514A, 78F0524, 78F0524A, 78F0534, 78F0534A, 78F0544, and 78F0544A)



Note The buffer RAM is incorporated only in the μPD78F0544 and 78F0544A (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0514, 78F0514A, 78F0524, 78F0524A, 78F0534, and 78F0534A.

Figure 3-19. Correspondence Between Data Memory and Addressing
(μPD78F0527, 78F0527A, 78F0537, 78F0537A, 78F0547, 78F0547A, 78F0527D, 78F0527DA, 78F0537D, 78F0537DA, 78F0547D and 78F0547DA)



Notes 1. The buffer RAM is incorporated only in the μPD78F0547, 78F0547A, 78F0547D and 78F0547DA (78K0/KF2). The area from FA00H to FA1FH cannot be used with the μPD78F0527, 78F0527A, 78F0537, 78F0537A, 78F0527D, 78F0527DA, 78F0537D and 78F0537DA.

2. To branch to or address a memory bank that is not set by the memory bank select register (BANK), change the setting of the memory bank by using BANK.

Table 3-8. Special Function Register List (5/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset	KB2	KC2	KD2	KE2	KF2
					1 Bit	8 Bits	16 Bits						
FFE8H	Priority specification flag register 0L	PR0	PR0L	R/W	√	√	√	FFH	√	√	√	√	√
FFE9H	Priority specification flag register 0H		PR0H	R/W	√	√		FFH	√	√	√	√	√
FFEAH	Priority specification flag register 1L	PR1	PR1L	R/W	√	√	√	FFH	√	√	√	√	√
FFEBH	Priority specification flag register 1H		PR1H	R/W	√	√		FFH	√	√	√	√	√
FFF0H	Internal memory size switching register[Notes 3,4]	IMS		R/W	–	√	–	CFH	√	√	√	√	√
FFF3H	Memory bank select register	BANK		R/W	–	√	–	00H	–	–	Note 1	Note 1	Note 1
FFF4H	Internal expansion RAM size switching register[Notes 3,4]	IXS		R/W	–	√	–	0CH	Note 2	Note 2	Note 2	Note 2	√
FFFBH	Processor clock control register	PCC		R/W	√	√	–	01H	√	√	√	√	√

Notes 1. This register is incorporated only in products whose flash memory is at least 96 KB.

2. Set this register only in products with internal expansion RAM.

3. Regardless of the internal memory capacity, the initial values of the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS) of all products in the 78K0/Kx2 microcontrollers are fixed (IMS = CFH, IXS = 0CH). Therefore, set the value corresponding to each product as indicated in Tables 3-1 and 3-2.

4. The ROM and RAM capacities of the products with the on-chip debug function can be debugged by setting IMS and IXS, according to the debug target products. Set IMS and IXS according to the debug target products.

CHAPTER 4 MEMORY BANK SELECT FUNCTION (PRODUCTS WHOSE FLASH MEMORY IS AT LEAST 96 KB ONLY)

4.1 Memory Bank

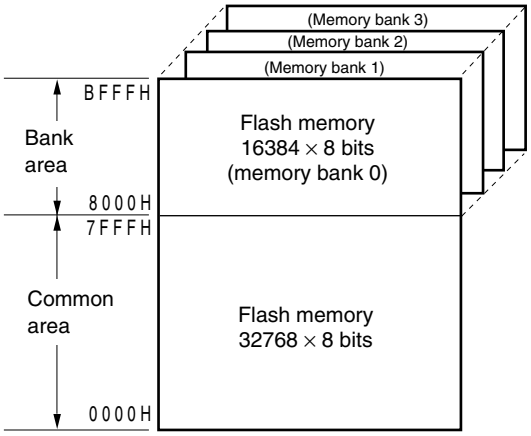
The μPD78F05x6, 78F05x6A, 78F05x7, 78F05x7A, 78F05x7D and 78F05x7DA of 78K0/KD2, 78K0/KE2, and 78K0/KF2 implement a ROM capacity of 96 KB or 128 KB by selecting a memory bank from a memory space of 8000H to BFFFH.

The μPD78F05x6 and 78F05x6A have memory banks 0 to 3, and the μPD78F05x7, 78F05x7A, 78F05x7D and 78F05x7DA have memory banks 0 to 5, as shown below.

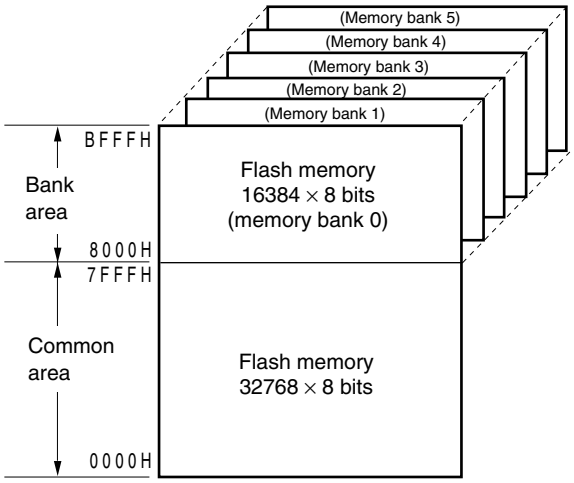
The memory banks are selected by using a memory bank select register (BANK).

Figure 4-1. Internal ROM (Flash Memory) Configuration

(a) μPD78F05x6 and 78F05x6A (products whose flash memory is 96 KB)

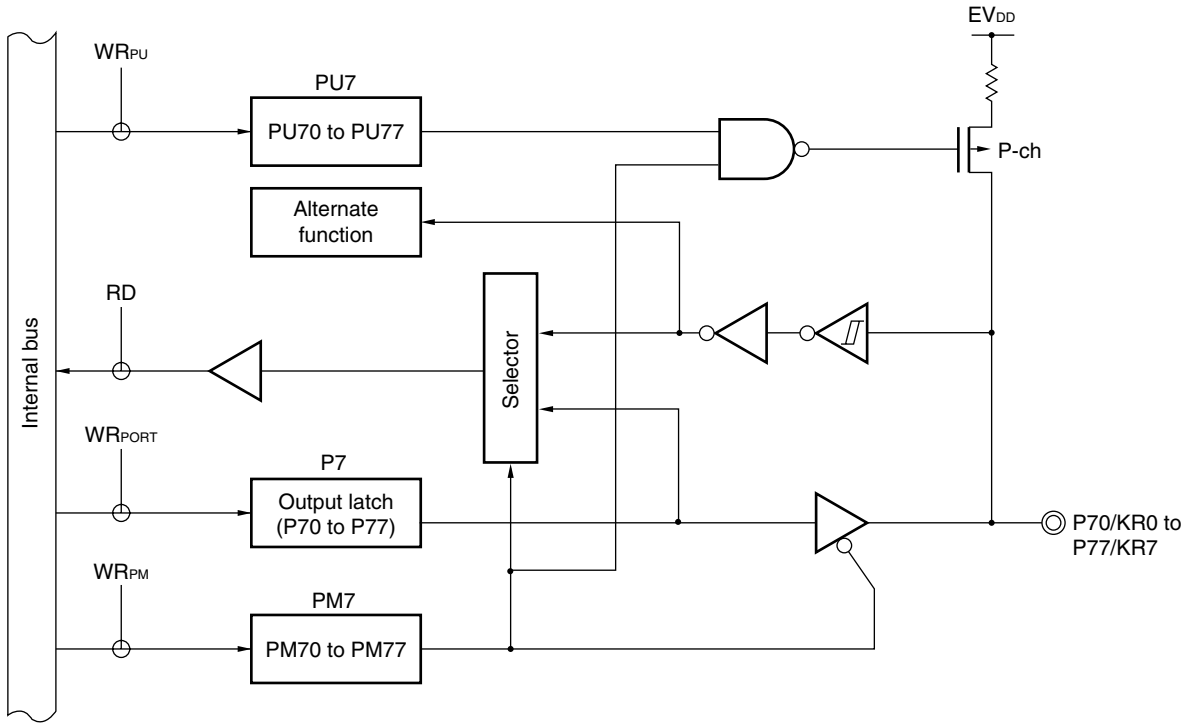


(b) μPD78F05x7, 78F05x7A, 78F05x7D, and 78F05x7DA (products whose flash memory is 128 KB)



Remark x = 2 to 4

Figure 5-21. Block Diagram of P70 to P77



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

Caution For the 38-pin products of 78K0/KC2, be sure to set bits 2 and 3 of PM7 and P7 to "0".

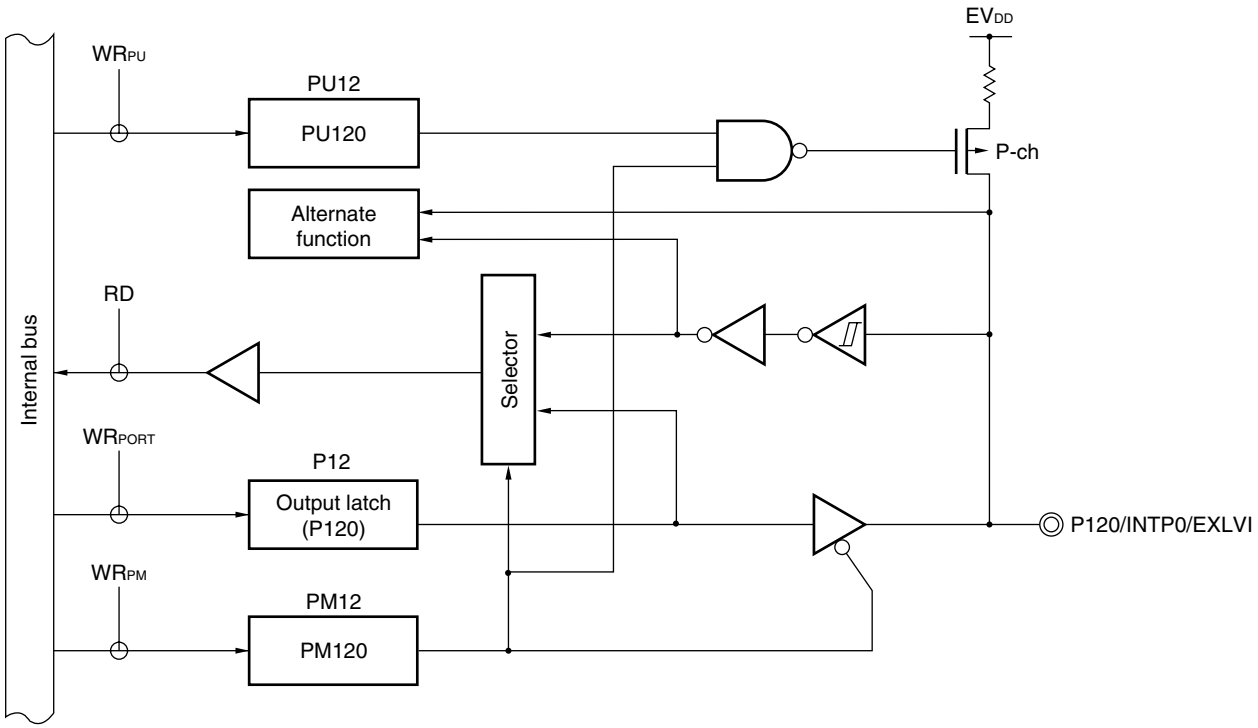
Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Caution 2. Process the P121/X1/OCD0A pin of the products mounted with the on-chip debug function (μPD78F05xxD and 78F05xxDA) as follows, when it is not used when it is connected to a flash memory programmer or an on-chip debug emulator.

		P121/X1/OCD0A
Flash memory programmer connection		Connect to V_{SS} via a resistor.
On-chip debug emulator connection (when it is not used as an on-chip debug mode setting pin)	During reset	
	During reset released	Input: Connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.

Remark X1 and X2 of the product with an on-chip debug function (μPD78F05xxD and 78F05xxDA) can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For how to connect an on-chip debug emulator (QB-MINI2), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION (μPD78F05xxD AND 78F05xxDA ONLY).**

Figure 5-22. Block Diagram of P120

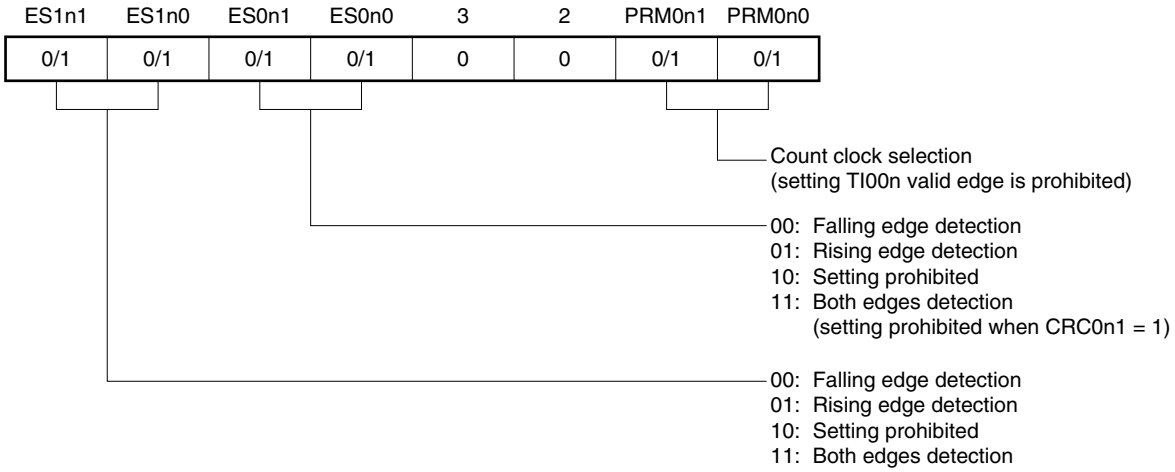


P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 7-43. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 0n (PRM0n)



(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM00n) is generated. The count value of TM0n is not cleared.

To use this register as a capture register, select either the TI00n or TI01n pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR00n.

(g) 16-bit capture/compare register 01n (CR01n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM01n) is generated. The count value of TM0n is not cleared.

When this register is used as a capture register, the TI00n pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR01n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(1) 8-bit timer counter 5n (TM5n)

TM5n is an 8-bit register that counts the count pulses and is read-only.

The counter is incremented in synchronization with the rising edge of the count clock.

Figure 8-3. Format of 8-Bit Timer Counter 5n (TM5n)

Address: FF16H (TM50), FF1FH (TM51) After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
TM5n (n = 0, 1)								

In the following situations, the count value is cleared to 00H.

<1> Reset signal generation

<2> When TCE5n is cleared

<3> When TM5n and CR5n match in the mode in which clear & start occurs upon a match of the TM5n and CR5n.

(2) 8-bit timer compare register 5n (CR5n)

CR5n can be read and written by an 8-bit memory manipulation instruction.

Except in PWM mode, the value set in CR5n is constantly compared with the 8-bit timer counter 5n (TM5n) count value, and an interrupt request (INTTM5n) is generated if they match.

In the PWM mode, TO5n output becomes inactive when the values of TM5n and CR5n match, but no interrupt is generated.

The value of CR5n can be set within 00H to FFH.

Reset signal generation clears CR5n to 00H.

Figure 8-4. Format of 8-Bit Timer Compare Register 5n (CR5n)

Address: FF17H (CR50), FF41H (CR51) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CR5n (n = 0, 1)								

Cautions 1. In the mode in which clear & start occurs on a match of TM5n and CR5n (TMC5n6 = 0), do not write other values to CR5n during operation.

2. In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.

Remark n = 0, 1

Figure 9-6. Format of 8-Bit Timer H Mode Register 1 (TMHMD1)

Address: FF6CH After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock selection[Note 1]				
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz	20 MHz[Note 3]
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
1	0	0	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz	4.88 kHz
1	0	1	$f_{RL}/2^7$	1.88 kHz (TYP.)			
1	1	0	$f_{RL}/2^9$	0.47 kHz (TYP.)			
1	1	1	f_{RL}	240 kHz (TYP.)			

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disables output
1	Enables output

Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when f_{PRS} = f_{XH} (XSEL = 1).)

13.4.3 A/D converter operation mode

The operation mode of the A/D converter is the select mode. One channel of analog input is selected from ANI0 to ANI7 by the analog input channel specification register (ADS) and A/D conversion is executed.

Remark ANI0 to ANI3: 78K0/KB2
ANI0 to ANI5: 38-pin products of the 78K0/KC2
ANI0 to ANI7: Products other than above

(1) A/D conversion operation

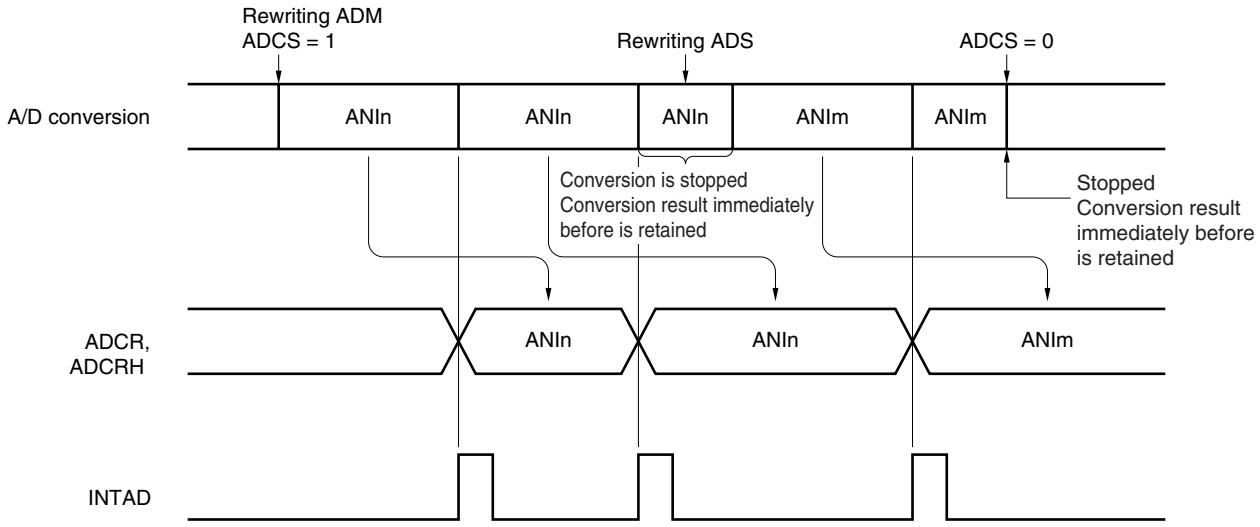
By setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 1, the A/D conversion operation of the voltage, which is applied to the analog input pin specified by the analog input channel specification register (ADS), is started.

When A/D conversion has been completed, the result of the A/D conversion is stored in the A/D conversion result register (ADCR), and an interrupt request signal (INTAD) is generated. When one A/D conversion has been completed, the next A/D conversion operation is immediately started.

If ADS is rewritten during A/D conversion, the A/D conversion operation under execution is stopped and restarted from the beginning.

If 0 is written to ADCS during A/D conversion, A/D conversion is immediately stopped. At this time, the conversion result immediately before is retained.

Figure 13-13. A/D Conversion Operation



Remarks 1. 78K0/KB2: n = 0 to 3, 38-pin products of the 78K0/KC2: n = 0 to 5, other products: n = 0 to 7

2. 78K0/KB2: m = 0 to 3, 38-pin products of the 78K0/KC2: m = 0 to 5, other products: m = 0 to 7

Caution Make sure POWER6 = 0 when rewriting TPS63 to TPS60.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

(5) Baud rate generator control register 6 (BRGC6)

This register sets the division value of the 8-bit counter of serial interface UART6.

BRGC6 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Remark BRGC6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 15-9. Format of Baud Rate Generator Control Register 6 (BRGC6)

Address: FF57H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
BRGC6	MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60

MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60	k	Output clock selection of 8-bit counter
0	0	0	0	0	0	×	×	×	Setting prohibited
0	0	0	0	0	1	0	0	4	$f_{XCLK6}/4$
0	0	0	0	0	1	0	1	5	$f_{XCLK6}/5$
0	0	0	0	0	1	1	0	6	$f_{XCLK6}/6$
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	0	252	$f_{XCLK6}/252$
1	1	1	1	1	1	0	1	253	$f_{XCLK6}/253$
1	1	1	1	1	1	1	0	254	$f_{XCLK6}/254$
1	1	1	1	1	1	1	1	255	$f_{XCLK6}/255$

Cautions 1. Make sure that bit 6 (TXE6) and bit 5 (RXE6) of the ASIM6 register = 0 when rewriting the MDL67 to MDL60 bits.

2. The baud rate is the output clock of the 8-bit counter divided by 2.

Remarks 1. f_{XCLK6}: Frequency of base clock selected by the TPS63 to TPS60 bits of CKSR6 register

2. k: Value set by MDL67 to MDL60 bits (k = 4, 5, 6, ..., 255)

3. ×: Don't care

The features of serial interface CSIA0 are as follows.

- Master mode/slave mode selectable
- Communication data length: 8 bits
- MSB/LSB-first selectable for communication data
- Automatic transmit/receive function:
  Number of transfer bytes can be specified between 1 and 32
  Transfer interval can be specified (0 to 63 clocks)
  Single communication/repeat communication selectable
  Internal 32-byte buffer RAM
- On-chip dedicated baud rate generator (6/8/16/32 divisions)
- 3-wire SOA0: Serial data output
  SIA0: Serial data input
  $\overline{\text{SCKA0}}$: Serial clock I/O
- Handshake function incorporated STB0: Strobe output
  BUSY0: Busy input
- Detection of bit shift error due to BUSY0 signal
- Transmission/reception completion interrupt: INTACSI

17.2 Configuration of Serial Interface CSIA0

Serial interface CSIA0 consists of the following hardware.

Table 17-1. Configuration of Serial Interface CSIA0

Item	Configuration
Controller	Serial transfer controller
Registers	Serial I/O shift register 0 (SIOA0)
Control registers	Serial operation mode specification register 0 (CSIMA0) Serial status register 0 (CSIS0) Serial trigger register 0 (CSIT0) Divisor selection register 0 (BRGCA0) Automatic data transfer address point specification register 0 (ADTP0) Automatic data transfer interval specification register 0 (ADTI0) Automatic data transfer address count register 0 (ADTC0) Port mode register 14 (PM14) Port register 14 (P14)

Figure 20-13. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KC2)

Address: FFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	DUALPR0 CSIPR10 STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR1L	1	PPR6Note 1	WTPR	KRPR	TMPR51	WTIPR	SRPR0	ADPR

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	<0>
PR1H	1	1	1	1	1	1	1	IICPR0 DMUPRNote 2

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Notes 1. 48-pin products only.

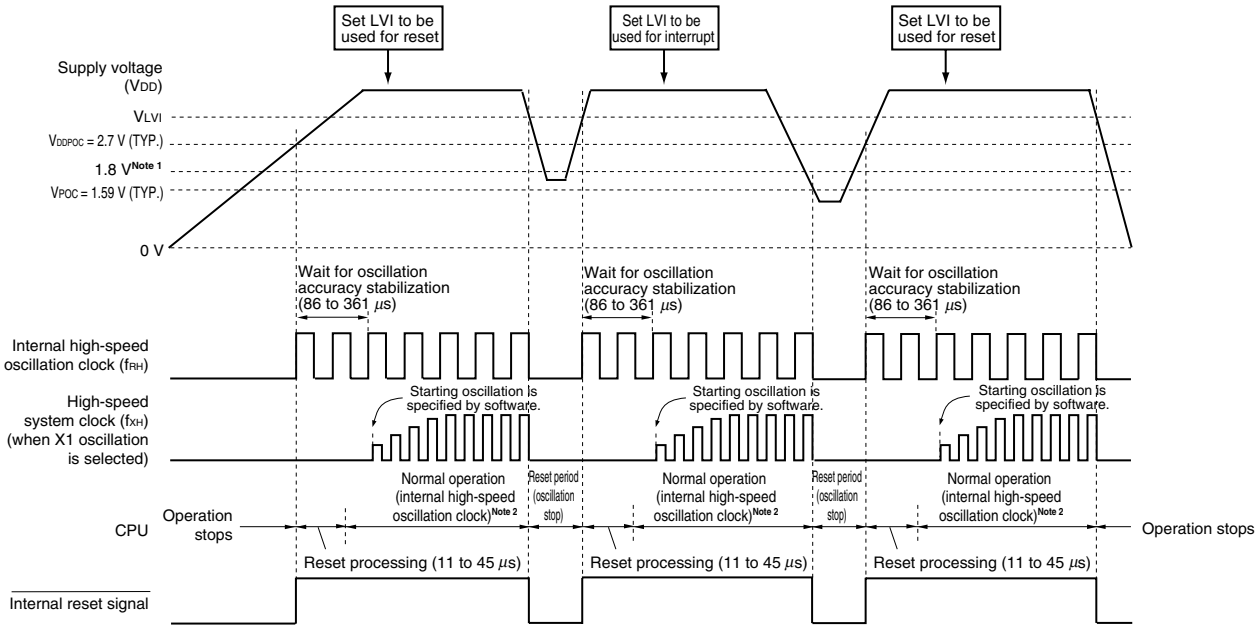
2. Products whose flash memory is at least 48 KB only.

Cautions 1. Be sure to set bits 6 and 7 of PR1L to 1 in the 38-pin and 44-pin products.
Be sure to set bit 7 of PR1L to 1 in the 48-pin products.

2. Be sure to set bits 1 to 7 of PR1H to 1.

Figure 24-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)

(2) In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)



Notes 1. The guaranteed operation range for the standard and (A) grade products is 1.8 V ≤ V_{DD} ≤ 5.5 V, and 2.7 V ≤ V_{DD} ≤ 5.5 V for the (A2) grade products. To set the voltage range below the guaranteed operation range to the reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input a low level to the $\overline{\text{RESET}}$ pin.

2. The CPU clock can be switched from the internal high-speed oscillation clock to the high-speed system clock or subsystem clock[Note 3]. To use the X1 clock, use the OSTC register to confirm the lapse of the oscillation stabilization time. To use the XT1 clock[Note 3], use the timer function for confirmation of the lapse of the stabilization time.

3. The 78K0/KB2 is not provided with subsystem clock and XT1 clock.

Cautions 1. Set the low-voltage detector by software after the reset status is released (see CHAPTER 25 LOW-VOLTAGE DETECTOR).

2. A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the supply voltage reaches 1.59 V (TYP.). If the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) within 1.93 ms, the power supply oscillation stabilization time of 0 to 5.39 ms is automatically generated before reset processing.

Remark V_{LVI}: LVI detection voltage
V_{POC}: POC detection voltage

24.4 Cautions for Power-on-Clear Circuit

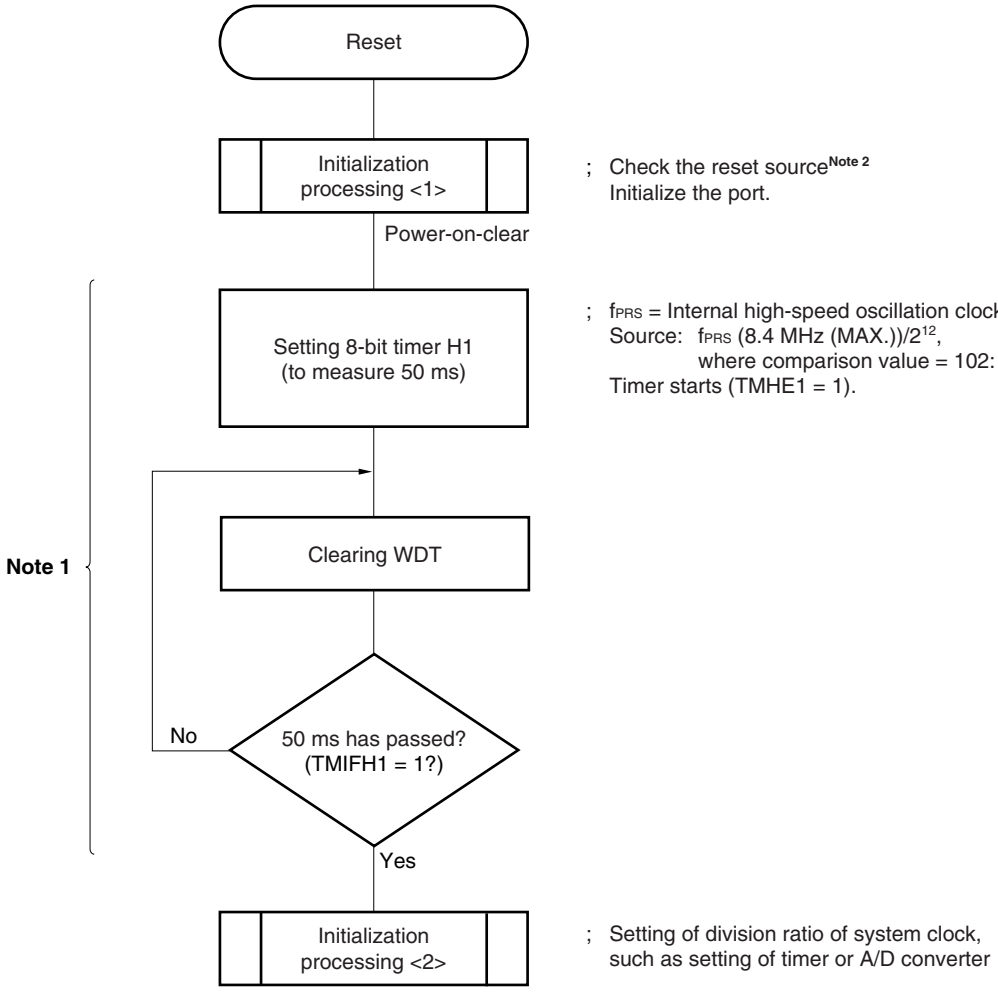
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 24-3. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of POC detection voltage

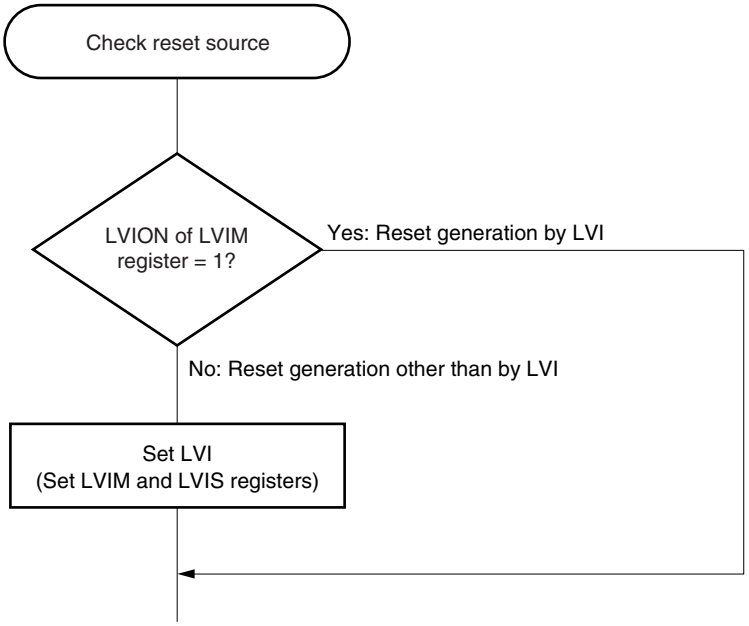


Notes 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

Figure 25-9. Example of Software Processing After Reset Release (2/2)

• Checking reset source



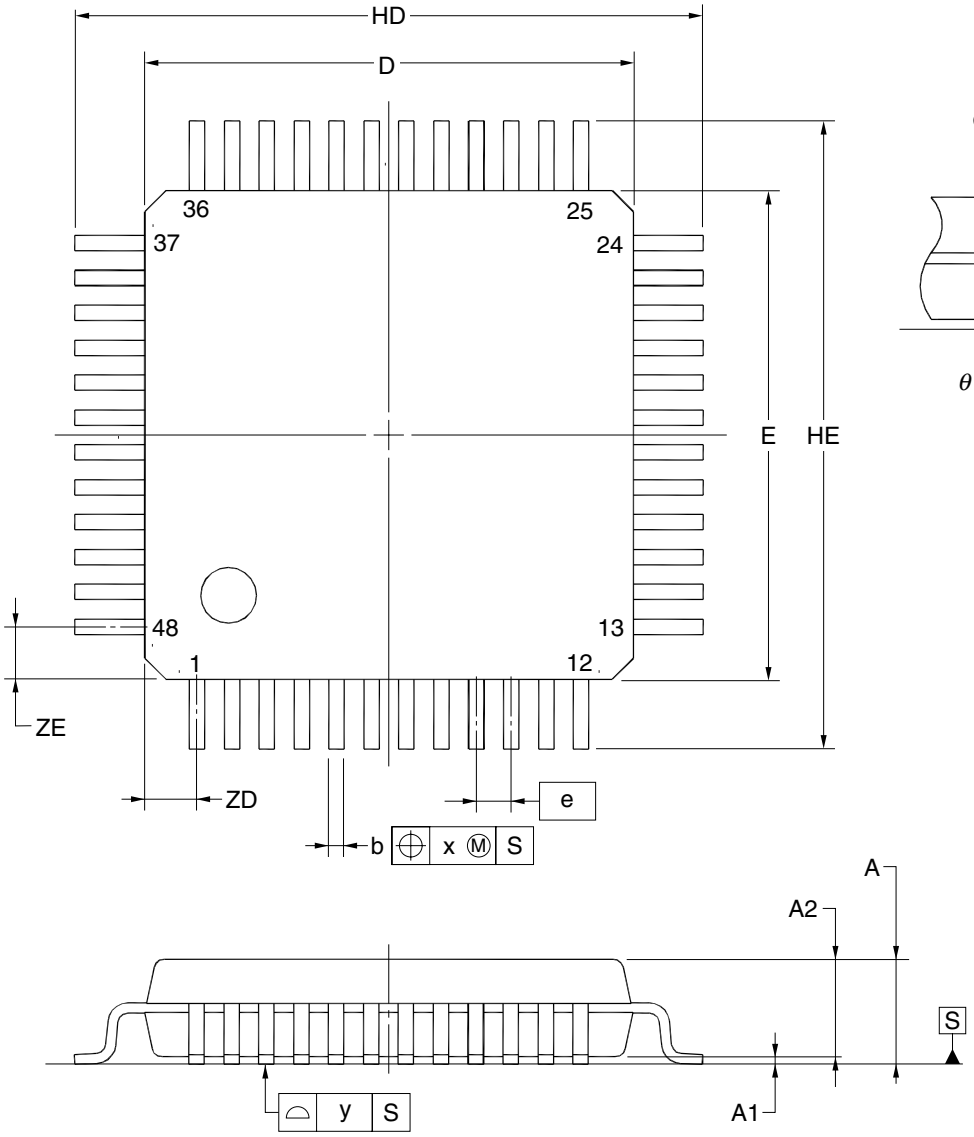
Here is an example of description of the software for setting the option bytes.

```
OPT     CSEG   AT 0080H
OPTION: DB     30H      ; Enables watchdog timer operation (illegal access detection operation),
                        ; Window open period of watchdog timer: 50%,
                        ; Overflow time of watchdog timer: 2^10/fRL,
                        ; Internal low-speed oscillator can be stopped by software.
        DB     00H      ; 1.59 V POC mode
        DB     00H      ; Reserved area
        DB     00H      ; Reserved area
        DB     00H      ; On-chip debug operation disabled
```

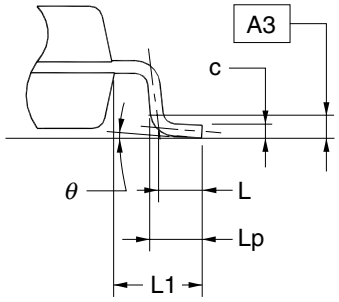
Remark Referencing of the option byte is performed during reset processing. For the reset processing timing, see **CHAPTER 23 RESET FUNCTION**.

- μPD78F0511GA-8EU-A, 78F0512GA-8EU-A, 78F0513GA-8EU-A, 78F0514GA-8EU-A, 78F0515GA-8EU-A, 78F0515DGA-8EU-A

48-PIN PLASTIC LQFP (FINE PITCH)(7x7)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-8EU

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

(19/30)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 16	Soft	Serial interface CSI10, CSI11	SOTB1n: Transmit buffer register 1n	Do not access SOTB1n when CSOT1n = 1 (during serial communication).	p. 492 ☐
				In the slave mode, transmission/reception is started when data is written to SOTB11 with a low level input to the $\overline{SSI11}$ pin. For details on the transmission/reception operation, see 16.4.2 (2) Communication operation.	p. 492 ☐
			CSIM10: Serial operation mode register 10	Be sure to clear bit 5 to 0.	p. 493 ☐
			CSIC10: Serial clock selection register 10	Do not write to CSIC10 while CSIE10 = 1 (operation enabled).	p. 496 ☐
				To use P10/$\overline{SCK10}$/TxD0 and P12/SO10 as general-purpose ports, set CSIC10 in the default status (00H).	p. 496 ☐
				The phase type of the data clock is type 1 after reset.	p. 496 ☐
			CSIC11: Serial clock selection register 11	Do not write to CSIC11 while CSIE11 = 1 (operation enabled).	p. 498 ☐
				To use P02/SO11 and P04/$\overline{SCK11}$ as general-purpose ports, set CSIC11 in the default status (00H).	p. 498 ☐
				The phase type of the data clock is type 1 after reset.	p. 498 ☐
			3-wire serial I/O mode	Take relationship with the other party of communication when setting the port mode register and port register.	p. 500 ☐
			Communication operation	Do not access the control register and data register when CSOT1n = 1 (during serial communication).	p. 503 ☐
				When using serial interface CSI11, wait for the duration of at least one clock before the clock operation is started to change the level of the $\overline{SSI11}$ pin in the slave mode; otherwise, malfunctioning may occur.	p. 503 ☐
			SO1n output	If a value is written to CSIE1n, TRMD1n, DAP1n, and DIR1n, the output value of SO1n changes.	p. 511 ☐
Chapter 17	Soft	Serial interface CSIA0	SIOA0: Serial I/O shift register 0	A communication operation is started by writing to SIOA0. Consequently, when transmission is disabled (bit 3 (TXEA0) of CSIMA0 = 0), write dummy data to the SIOA0 register to start the communication operation, and then perform a receive operation.	p. 515 ☐
				Do not write data to SIOA0 while the automatic transmit/receive function is operating.	p. 515 ☐
			CSIMA0: Serial operation mode specification register 0	When CSIAE0 = 0, the buffer RAM cannot be accessed.	p. 516 ☐
				When CSIAE0 is changed from 1 to 0, the registers and bits mentioned in Note above are asynchronously initialized. To set CSIAE0 = 1 again, be sure to re-set the initialized registers.	p. 516 ☐
				When CSIAE0 is re-set to 1 after CSIAE0 is changed from 1 to 0, it is not guaranteed that the value of the buffer RAM will be retained.	p. 516 ☐
			CSIS0: Serial status register 0	Be sure to clear bit 7 to 0.	p. 517 ☐
				During transfer (TSF0 = 1), rewriting serial operation mode specification register 0 (CSIMA0), serial status register 0 (CSIS0), divisor selection register 0 (BRGCA0), automatic data transfer address point specification register 0 (ADTP0), automatic data transfer interval specification register 0 (ADTI0), and serial I/O shift register 0 (SIOA0) are prohibited. However, these registers can be read and re-written to the same value. In addition, the buffer RAM can be rewritten during transfer.	p. 518 ☐
			CSIT0: Serial trigger register 0	Even if ATSTP0 or ATSTA0 is set to 1, automatic transfer cannot be started/stopped until 1-byte transfer is complete.	p. 519 ☐
				ATSTP0 and ATSTA0 change to 0 automatically after the interrupt signal INTACSI is generated.	p. 519 ☐
				After automatic data transfer is stopped, the data address when the transfer stopped is stored in automatic data transfer address count register 0 (ADTC0). However, since no function to restart automatic data transfer is incorporated, when transfer is stopped by setting ATSTP0 = 1, start automatic data transfer by setting ATSTA0 to 1 after re-setting the registers.	p. 519 ☐