Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0545agc-gad-ax

- On-chip 10-bit resolution A/D converter (AV_{REF} = 2.3 to 5.5 V)
- On-chip multiplier/divider (16 bits × 16 bits, 32 bits/16 bits), key interrupt function, clock output/buzzer output controller, I/O ports, timer, and serial interface
- Power supply voltage
  - Standard products, (A) grade products: V_{DD} = 1.8 to 5.5 V
  - (A2) grade products: V_{DD} = 2.7 to 5.5 V
- Operating ambient temperature
  - Standard products, (A) grade products: T_A = –40 to +85°C
  - (A2) grade products: T_A = –40 to +125°C

Remark The functions mounted depend on the product. See **1.7 Block Diagram** and **1.8 Outline of Functions**.

1.3 Applications

- Automotive equipment (compatible with (A) and (A2) grade products)
  - System control for body electricals (power windows, keyless entry reception, etc.)
  - Sub-microcontrollers for control
- Car audio
- AV equipment, home audio
- PC peripheral equipment (keyboards, etc.)
- Household electrical appliances
  - Air conditioners
  - Microwave ovens, electric rice cookers
- Industrial equipment
  - Pumps
  - Vending machines
  - FA (Factory Automation)

1.4 Ordering Information

[Part Number]

μPD78F05xy X X XX (X) - XXX - XX

	Semiconductor	
A	Lead-free	Product contains no lead in any area
AX, G		Product contains no lead in any area (Terminal finish is Ni/Pd/Au plating)

	Quality Grade
None	Standard (T_A = −40 to +85°C)
(A), A	Special (T_A = −40 to +85°C)
(A2), A2	Special (T_A = −40 to +125°C)

		Package Type
50y (KB2)	MC-5A4	30-pin plastic SSOP (7.62 mm (300))
	MC-CAB	
	FC-AA3	36-pin plastic FLGA (4x4)
51y (KC2)	MC-GAA	38-pin plastic SSOP (7.62 mm (300))
	GB-UES	44-pin plastic LQFP (10x10)
	GB-GAF	
	GA-8EU	48-pin plastic LQFP (fine pitch) (7x7)
	GA-GAM	
52y (KD2)	GB-UET	52-pin plastic LQFP (10x10)
	GB-GAG	
53y (KE2)	GB-UEU	64-pin plastic LQFP (fine pitch) (10x10)
	GB-GAH	
	GC-UBS	64-pin plastic LQFP (14x14)
	GC-GAL	
	GK-UET	64-pin plastic LQFP (12x12)
	GK-GAJ	
	GA-9EV	64-pin plastic TQFP (fine pitch) (7x7)
	GA-HAB	
	FC-AA1	64-pin plastic FLGA (5x5)
	F1-AA2	64-pin plastic FBGA (4x4)
54y (KF2)	GC-UBT	80-pin plastic LQFP (14x14)
	GC-GAD	
	GK-8EU	80-pin plastic LQFP (fine pitch) (12x12)
	GK-GAK	

	Product Type
None	Conventional-specification products
A	Expanded-specification products

	On-chip Debug Function
None	Not mounted
D	Mounted

	High-speed RAM Capacity	Expansion RAM Capacity	Flash Memory Capacity
5x0	512 bytes	–	8 KB
5x1	768 bytes	–	16 KB
5x2	1 KB	–	24 KB
5x3	1 KB	–	32 KB
5x4	1 KB	1 KB	48 KB
5x5	1 KB	2 KB	60 KB
5x6	1 KB	4 KB	96 KB
5x7	1 KB	6 KB	128 KB

	Product Type
F	Flash memory version

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by Renesas Electronics to know the specification of quality grade on the devices and its recommended applications.

(d) SI11

This is a serial data input pin of serial interface CSI11.

(e) SO11

This is a serial data output pin of serial interface CSI11.

(f) $\overline{\text{SCK11}}$

This is a serial clock I/O pin of serial interface CSI11.

(g) $\overline{\text{SSI11}}$

This is a chip select input pin of serial interface CSI11.

2.2.2 P10 to P17 (port 1)

P10 to P17 function as an I/O port. These pins also function as pins for external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2		78K0/KF2
				Products whose flash memory is less than 32 KB	Products whose flash memory is at least 48 KB	
P10/$\overline{\text{SCK10}}$/TxD0	√					
P11/SI10/RxD0	√					
P12/SO10	√					
P13/TxD6	√					
P14/RxD6	√					
P15/TOH0	√					
P16/TOH1/INTP5	√					
P17/TI50/TO50	√					

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

(a) SI10

This is a serial data input pin of serial interface CSI10.

(b) SO10

This is a serial data output pin of serial interface CSI10.

(c) V_{DD} and EV_{DD}

V_{DD} is the positive power supply pin for P121 to P124 and other than ports[Note].

EV_{DD} is the positive power supply pin for ports other than P20 to P27 and P121 to P124.

Always make EV_{DD} the same potential as V_{DD}.

Note With products that are not mounted with an EV_{DD} pin, use V_{DD} as a positive power supply pin other than P20 to P27.

(d) V_{SS} and EV_{SS}

V_{SS} is the ground potential pin for P121 to P124 and other than ports.

EV_{SS} is the ground potential pin for ports other than P20 to P27 and P121 to P124.

Always make EV_{SS} the same potential as V_{SS}.

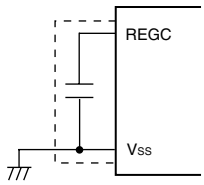
Note With products that are not mounted with an EV_{SS} pin, use V_{SS} as a ground potential pin other than P20 to P27.

2.2.13 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

2.2.14 REGC

This is the pin for connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF).



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

2.2.15 FLMD0

This is a pin for setting flash memory programming mode.

Connect FLMD0 to EV_{SS} or V_{SS} in the normal operation mode.

In flash memory programming mode, connect this pin to the flash memory programmer.

CHAPTER 5 PORT FUNCTIONS

5.1 Port Functions

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

Table 5-1. Pin I/O Buffer Power Supplies (AV_{REF}, V_{DD})

- 78K0/KB2: 30-pin plastic SSOP (7.62 mm (300))
- 78K0/KC2: 38-pin plastic SSOP (7.62 mm (300)), 44-pin plastic LQFP (10x10), 48-pin plastic LQFP (fine pitch) (7x7)
- 78K0/KD2: 52-pin plastic LQFP (10x10)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27
V_{DD}	Pins other than P20 to P27

Table 5-2. Pin I/O Buffer Power Supplies (AV_{REF}, EV_{DD}, V_{DD})

- 78K0/KB2: 36-pin plastic FLGA (4x4)
- 78K0/KE2: 64-pin plastic LQFP (fine pitch) (10x10), 64-pin plastic LQFP (14x14), 64-pin plastic LQFP (12x12), 64-pin plastic TQFP (fine pitch) (7x7), 64-pin plastic FLGA (5x5) , 64-pin plastic FBGA (4x4)
- 78K0/KF2: 80-pin plastic LQFP (14x14), 80-pin plastic LQFP (fine pitch) (12x12)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27
EV_{DD}	Port pins other than P20 to P27 and P121 to P124
V_{DD}	• P121 to P124 • Non-port pins

78K0/Kx2 microcontrollers are provided with digital I/O ports, which enable variety of control operations. The functions of each port are shown in Table 5-3.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

Table 5-3. Port Functions (1/3)

KB2	KC2	KD2	KES	KF2	Function Name	I/O	Function	After Reset	Alternate Function
√	√	√	√	√	P00	I/O	Port 0. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
√	√	√	√	√	P01				TI010/TO00
–	–	Note 1	Note 2	√	P02				SO11
–	–	Note 1	Note 2	√	P03				SI11
–	–	–	Note 2	√	P04				$\overline{\text{SCK11}}$
–	–	–	Note 2	√	P05				TI001/$\overline{\text{SSI11}}$
–	–	–	Note 2	√	P06				TI011/TO01
√	√	√	√	√	P10	I/O	Port 1. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK10}}$/TxD0
√	√	√	√	√	P11				SI10/RxD0
√	√	√	√	√	P12				SO10
√	√	√	√	√	P13				TxD6
√	√	√	√	√	P14				RxD6
√	√	√	√	√	P15				TOH0
√	√	√	√	√	P16				TOH1/INTP5
√	√	√	√	√	P17				TI50/TO50
√	√	√	√	√	P20	I/O	Port 2. I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0
√	√	√	√	√	P21				ANI1
√	√	√	√	√	P22				ANI2
√	√	√	√	√	P23				ANI3
–	√	√	√	√	P24				ANI4
–	√	√	√	√	P25				ANI5
–	Note 3	√	√	√	P26				ANI6
–	Note 3	√	√	√	P27				ANI7
√	√	√	√	√	P30	I/O	Port 3. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Analog input	INTP1
√	√	√	√	√	P31				INTP2/ OCD1A Note 4
√	√	√	√	√	P32				INTP3/ OCD1B Note 4
√	√	√	√	√	P33				TI51/TO51/ INTP4

Notes 1. The 78K0/KD2 products are only provided with port functions (P02 and P03) and not alternate functions.

2. The 78K0/KE2 products whose flash memory is less than 32 KB are only provided with port functions (P02 to P06) and not alternate functions. The 78K0/KE2 products whose flash memory is at least 48 KB are provided with port functions (P02 to P06) and alternate functions.

3. This is not mounted onto 38-pin products of the 78K0/KC2. For the 38-pin products, be sure to set bits 6 and 7 of PM2 to “1” and bits 6 and 7 of P2 to “0”.

4. OCD1A and OCD1B are provided to the products with an on-chip debug function (μPD78F05xxD and 78F05xxDA) only.

Remark √: Mounted, –: Not mounted

(3) Example of setting procedure when stopping the internal high-speed oscillation clock

The internal high-speed oscillation clock can be stopped in the following two ways.

- Executing the STOP instruction to set the STOP mode
- Setting RSTOP to 1 and stopping the internal high-speed oscillation clock

(a) To execute a STOP instruction

<1> Setting of peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, see **CHAPTER 22 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed. To operate the CPU immediately after the STOP mode has been released, set MCM0 to 0, switch the CPU clock to the internal high-speed oscillation clock, and check that RSTS is 1.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and internal high-speed oscillation clock is stopped.

(b) To stop internal high-speed oscillation clock by setting RSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the internal high-speed oscillation clock.

When CLS = 0 and MCS = 0, the internal high-speed oscillation clock is supplied to the CPU, so change the CPU clock to a clock other than the internal high-speed oscillation clock.

- 78K0/KB2

MCS	CPU Clock Status
0	Internal high-speed oscillation clock
1	High-speed system clock

- 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

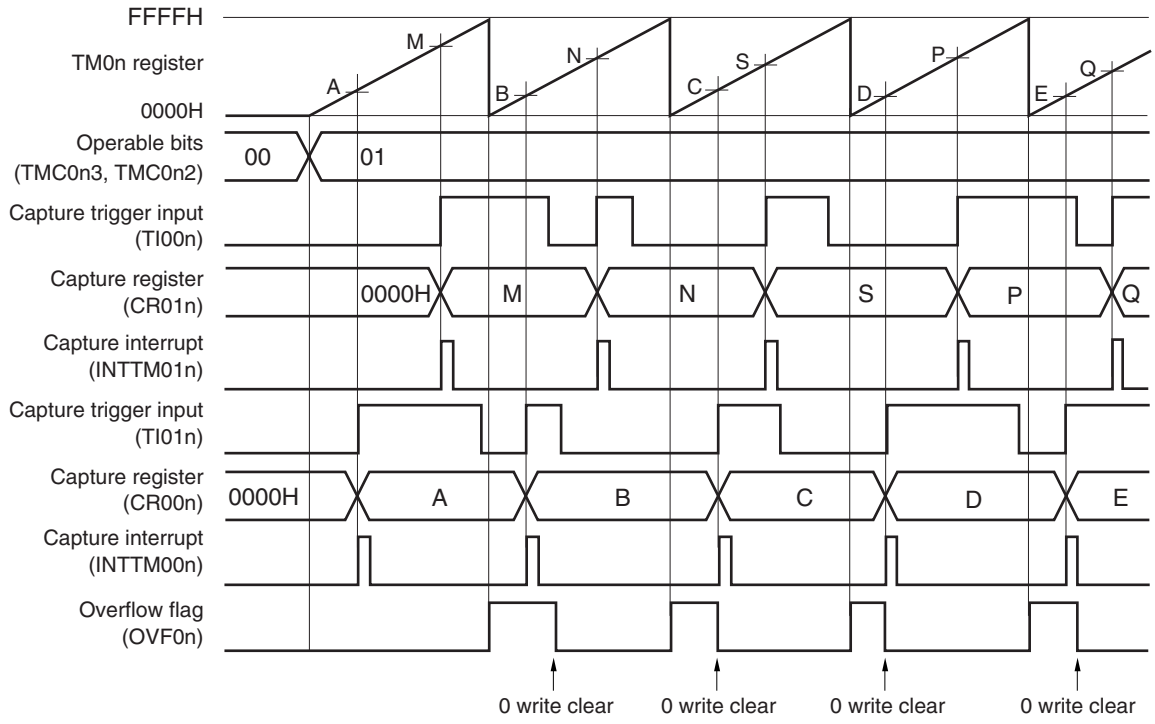
<2> Stopping the internal high-speed oscillation clock (RCM register)

When RSTOP is set to 1, internal high-speed oscillation clock is stopped.

Caution Be sure to confirm that MCS = 1 or CLS = 1 when setting RSTOP to 1. In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock.

Figure 7-42. Timing Example of Free-Running Timer Mode (CR00n: Capture Register, CR01n: Capture Register) (1/2)

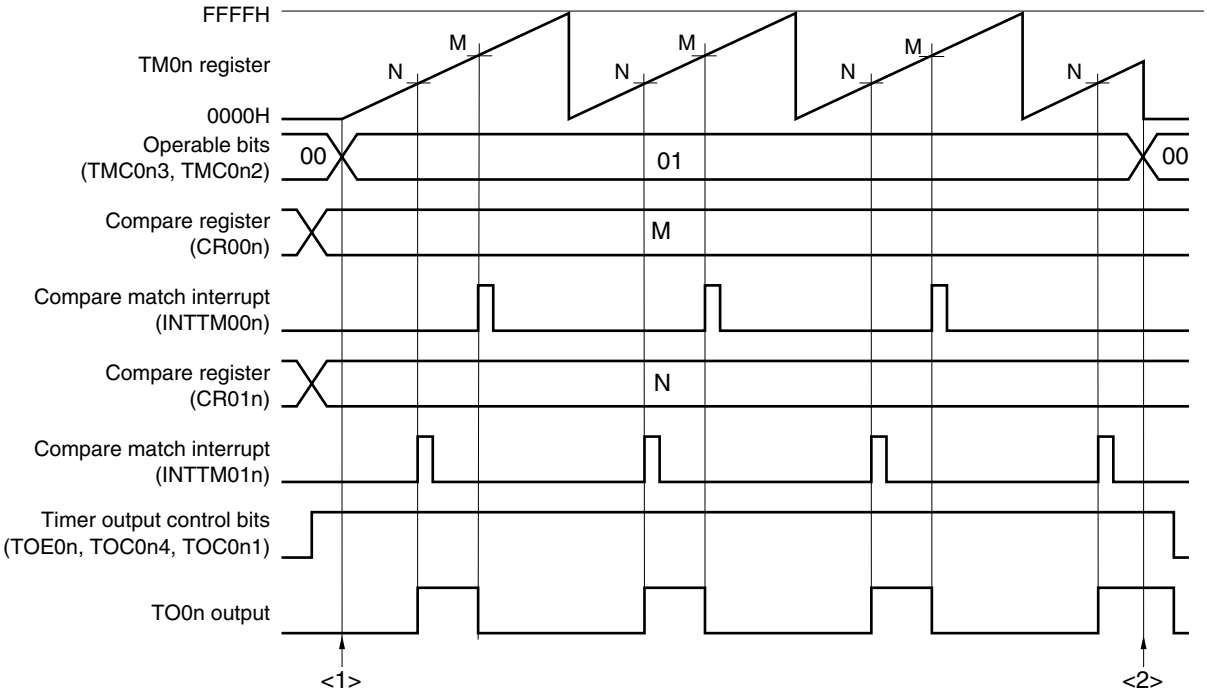
(a) TOC0n = 13H, PRM0n = 50H, CRC0n = 05H, TMC0n = 04H



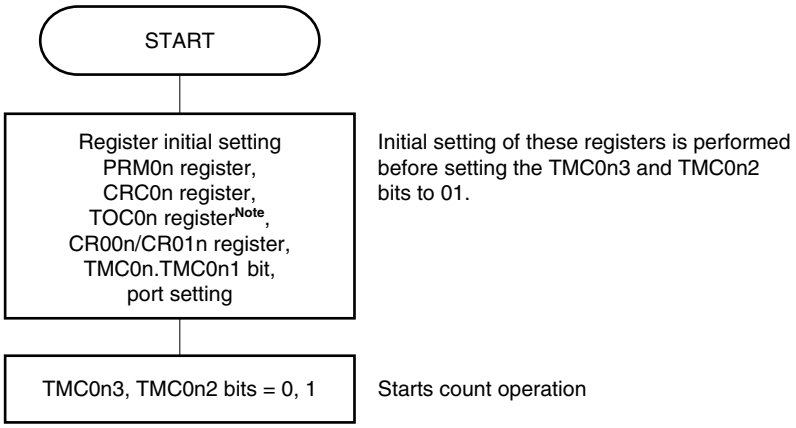
This is an application example where the count values that have been captured at the valid edges of separate capture trigger signals are stored in separate capture registers in the free-running timer mode.
The count value is captured to CR01n when the valid edge of the TI00n pin input is detected and to CR00n when the valid edge of the TI01n pin input is detected.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

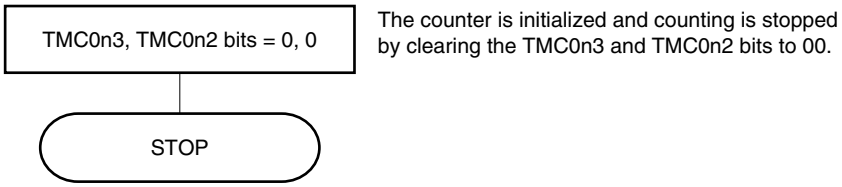
Figure 7-44. Example of Software Processing in Free-Running Timer Mode



<1> Count operation start flow



<2> Count operation stop flow



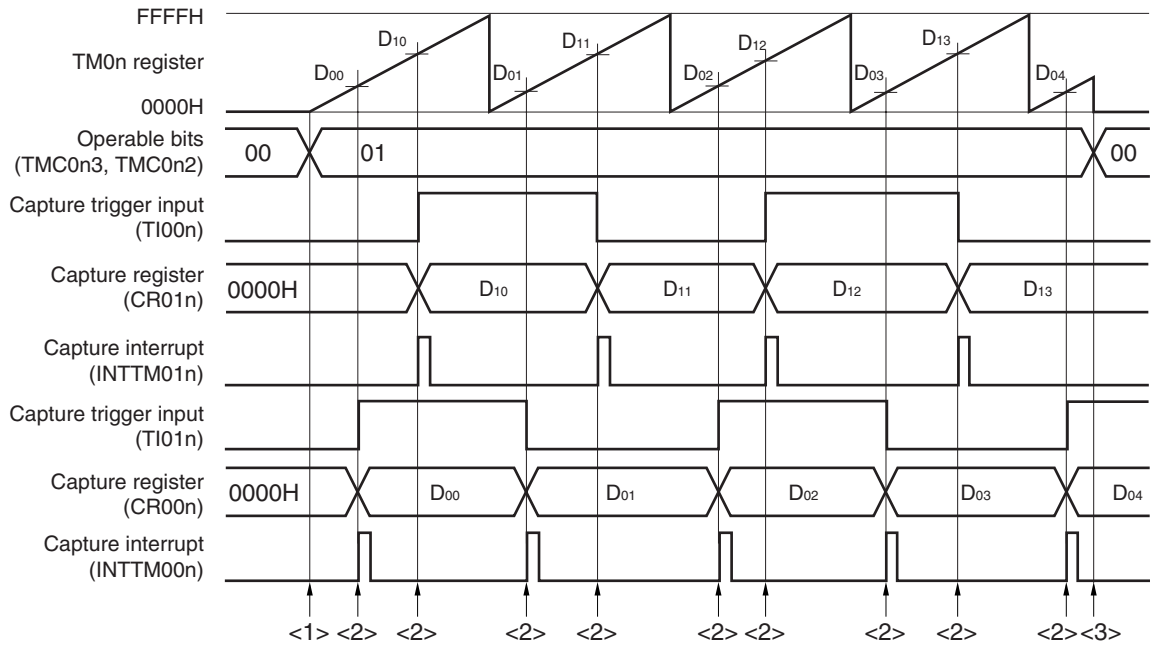
Note Care must be exercised when setting TOC0n. For details, see **7.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

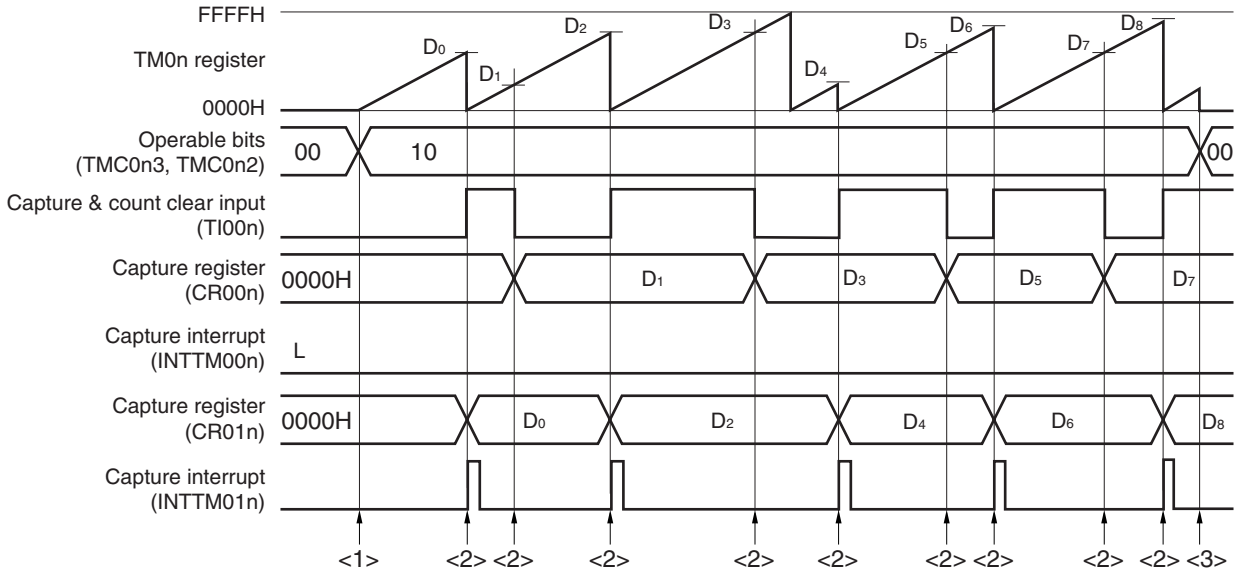
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-57. Example of Software Processing for Pulse Width Measurement (1/2)

(a) Example of free-running timer mode



(b) Example of clear & start mode entered by TI00n pin valid edge

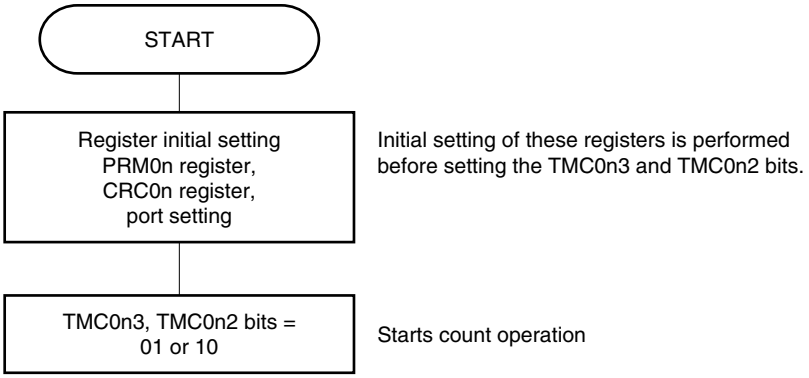


Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

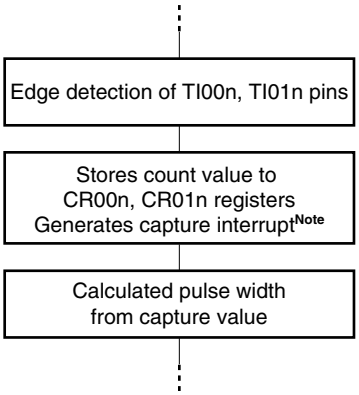
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-57. Example of Software Processing for Pulse Width Measurement (2/2)

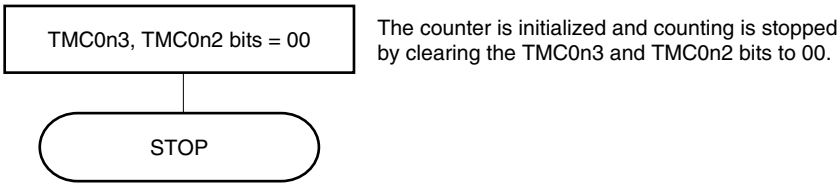
<1> Count operation start flow



<2> Capture trigger input flow



<3> Count operation stop flow



Note The capture interrupt signal (INTTM00n) is not generated when the reverse-phase edge of the TI00n pin input is selected to the valid edge of CR00n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

Caution When data is read from ADCR and ADCRH, a wait cycle is generated. Do not read data from ADCR and ADCRH when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 36 CAUTIONS FOR WAIT.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. Make this pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

The signal input to ANI0 to ANI7 is converted into a digital signal, based on the voltage applied across AV_{REF} and AV_{SS}.

(10) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always use this pin at the same potential as that of the V_{SS} pin even when the A/D converter is not used.

(11) A/D converter mode register (ADM)

This register is used to set the conversion time of the analog input signal to be converted, and to start or stop the conversion operation.

(12) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 pins to analog input of A/D converter or digital I/O of port.

(13) Analog input channel specification register (ADS)

This register is used to specify the port that inputs the analog voltage to be converted into a digital signal.

(14) Port mode register 2 (PM2)

This register switches the ANI0/P20 to ANI7/P27 pins to input or output.

Remark ANI0 to ANI3: 78K0/KB2
ANI0 to ANI5: 38-pin products of the 78K0/KC2
ANI0 to ANI7: Products other than above

Notes 1. The frequency that can be used for the peripheral hardware clock (f_{PRS}) differs depending on the power supply voltage and product specifications.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD)	Expanded-specification Products (μPD78F05xxA and 78F05xxDA)
4.0 V ≤ V_{DD} ≤ 5.5 V	f_{PRS} ≤ 20 MHz	f_{PRS} ≤ 20 MHz
2.7 V ≤ V_{DD} < 4.0 V	f_{PRS} ≤ 10 MHz	
1.8 V ≤ V_{DD} < 2.7 V (Standard products and (A) grade products only)	f_{PRS} ≤ 5 MHz	f_{PRS} ≤ 5 MHz

(The values shown in the table above are those when $f_{PRS} = f_{XH}$ (XSEL = 1).)

2. Set the serial clock to satisfy the following conditions.

Supply Voltage	Conventional-specification Products (μPD78F05xx and 78F05xxD) and Expanded-specification Products (μPD78F05xxA and 78F05xxDA)		
	Standard Products	(A) Grade Products	(A2) Grade Products
4.0 V ≤ V_{DD} ≤ 5.5 V	Serial clock ≤ 6.25 MHz	Serial clock ≤ 5 MHz	Serial clock ≤ 5 MHz
2.7 V ≤ V_{DD} < 4.0 V	Serial clock ≤ 4 MHz	Serial clock ≤ 2.5 MHz	Serial clock ≤ 2.5 MHz
1.8 V ≤ V_{DD} < 2.7 V	Serial clock ≤ 2 MHz	Serial clock ≤ 1.66 MHz	–

3. Do not start communication with the external clock from the $\overline{SCK10}$ pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. Do not write to CSIC10 while CSIE10 = 1 (operation enabled).

2. To use P10/$\overline{SCK10}$/TxD0 and P12/SO10 as general-purpose ports, set CSIC10 in the default status (00H).

3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock frequency

18.2 Configuration of Serial Interface IIC0

Serial interface IIC0 includes the following hardware.

Table 18-1. Configuration of Serial Interface IIC0

Item	Configuration
Registers	IIC shift register 0 (IIC0) Slave address register 0 (SVA0)
Control registers	IIC control register 0 (IICC0) IIC status register 0 (IICS0) IIC flag register 0 (IICF0) IIC clock selection register 0 (IICCL0) IIC function expansion register 0 (IICX0) Port mode register 6 (PM6) Port register 6 (P6)

(1) IIC shift register 0 (IIC0)

IIC0 is used to convert 8-bit serial data to 8-bit parallel data and vice versa in synchronization with the serial clock.

IIC0 can be used for both transmission and reception.

The actual transmit and receive operations can be controlled by writing and reading operations to IIC0.

Cancel the wait state and start data transfer by writing data to IIC0 during the wait period.

IIC0 is set by an 8-bit memory manipulation instruction.

Reset signal generation clears IIC0 to 00H.

Figure 18-3. Format of IIC Shift Register 0 (IIC0)

Address: FFA5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IIC0								

Cautions 1. Do not write data to IIC0 during data transfer.

2. Write or read IIC0 only during the wait period. Accessing IIC0 in a communication state other than during the wait period is prohibited. When the device serves as the master, however, IIC0 can be written only once after the communication trigger bit (STT0) is set to 1.

<R> **3. When communication is reserved, write data to the IIC0 register after the interrupt triggered by a stop condition is detected.**

(2) Slave address register 0 (SVA0)

<R> This register stores seven bits of local addresses {A6, A5, A4, A3, A2, A1, A0} when in slave mode.

This register can be set by an 8-bit memory manipulation instruction.

However, rewriting to this register is prohibited while STD0 = 1 (while the start condition is detected).

Reset signal generation clears SVA0 to 00H.

Figure 18-4. Format of Slave Address Register 0 (SVA0)

Address: FFA7H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVA0								0Note

Note Bit 0 is fixed to 0.

Figure 18-6. Format of IIC Status Register 0 (IICS0) (2/3)

COI0	Detection of matching addresses
0	Addresses do not match.
1	Addresses match.

Condition for clearing (COI0 = 0)	Condition for setting (COI0 = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL0 = 1 (exit from communications) • When IICE0 changes from 1 to 0 (operation stop) • Reset	• When the received address matches the local address (slave address register 0 (SVA0)) (set at the rising edge of the eighth clock).

TRC0	Detection of transmit/receive status
0	Receive status (other than transmit status). The SDA0 line is set for high impedance.
1	Transmit status. The value in the SO0 latch is enabled for output to the SDA0 line (valid starting at the falling edge of the first byte's ninth clock).

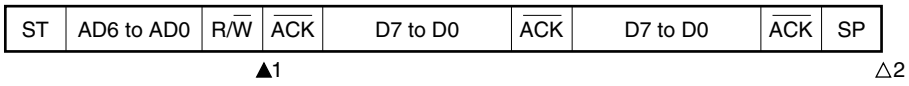
Condition for clearing (TRC0 = 0)	Condition for setting (TRC0 = 1)
<Both master and slave> • When a stop condition is detected • Cleared by LREL0 = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Cleared by WREL0 = 1[Note] (wait cancel) • When the ALD0 bit changes from 0 to 1 (arbitration loss) • Reset • When not used for communication (MSTS0, EXC0, COI0 = 0) <Master> • When "1" is output to the first byte's LSB (transfer direction specification bit) <Slave> • When a start condition is detected • When "0" is input to the first byte's LSB (transfer direction specification bit)	<Master> • When a start condition is generated • When 0 (master transmission) is output to the LSB (transfer direction specification bit) of the first byte (during address transfer) <Slave> • When 1 (slave transmission) is input to the LSB (transfer direction specification bit) of the first byte from the master (during address transfer)

<R>

Note When bit 3 (TRC0) of the IIC status register 0 (IICS0) is set to 1 (transmission status), bit 5 (WREL0) of the IIC control register 0 (IICC0) is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while TRC0 bit is 1 (transmission status) by writing to the IIC shift register.

Remark LREL0: Bit 6 of IIC control register 0 (IICC0)
IICE0: Bit 7 of IIC control register 0 (IICC0)

(b) When arbitration loss occurs during transmission of extension code



▲1: IICS0 = 0110×010B

Sets LREL0 = 1 by software

△2: IICS0 = 00000001B

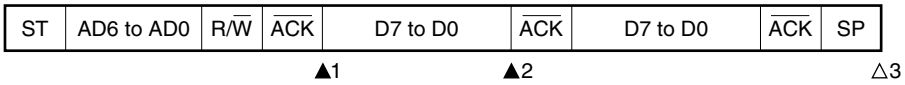
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(c) When arbitration loss occurs during transmission of data

(i) When WTIM0 = 0



▲1: IICS0 = 10001110B

▲2: IICS0 = 01000000B

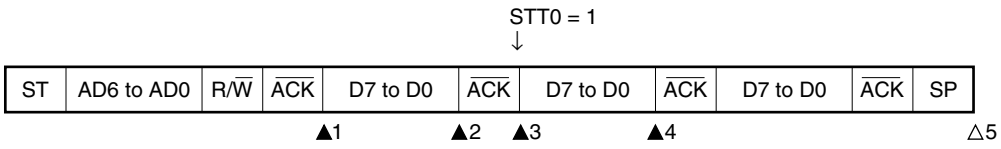
△3: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

(f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

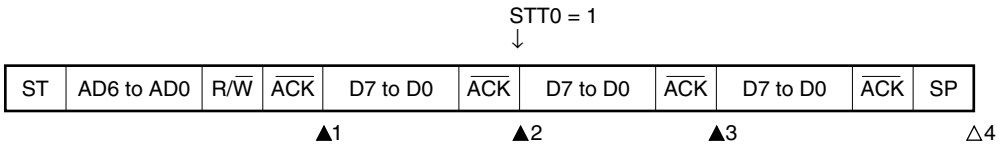
(i) When WTIM0 = 0



▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000×000B (Sets WTIM0 to 1)
▲3: IICS0 = 1000×100B (Clears WTIM0 to 0)
▲4: IICS0 = 01000000B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000×100B (Sets STT0 to 1)
▲3: IICS0 = 01000100B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

DC Characteristics (2/4)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high (products whose flash memory is at least 48 KB)[Note 1]	V_{IH1}	P02, P12, P13, P15, P40 to P47, P50 to P57, P64 to P67, P121 to P124, P144, P145, EXCLK, EXCLKS		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P03 to P06, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140 to P143, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH4}	P60 to P63		0.7V_{DD}		6.0	V
Input voltage, high (products whose flash memory is less than 32 KB)[Note 2]	V_{IH1}	P02 to P06, P12, P13, P15, P40 to P43, P50 to P53, P121 to P124, EXCLK, EXCLKS		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140, P141, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH4}	P60 to P63		0.7V_{DD}		6.0	V
Input voltage, low (products whose flash memory is at least 48 KB)[Note 1]	V_{IL1}	P02, P12, P13, P15, P40 to P47, P50 to P57, P60 to P67, P121 to P124, P144, P145, EXCLK, EXCLKS		0		0.3V_{DD}	V
	V_{IL2}	P00, P01, P03 to P06, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140 to P143, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Input voltage, low (products whose flash memory is less than 32 KB)[Note 2]	V_{IL1}	P02 to P06, P12, P13, P15, P40 to P43, P50 to P53, P60 to P63, P121 to P124, EXCLK, EXCLKS		0		0.3V_{DD}	V
	V_{IL2}	P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70 to P77, P120, P140, P141, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OH2} = –100 μA	V_{DD} – 0.5			V
		P121 to P124	I_{OH2} = –100 μA	V_{DD} – 0.5			V

Notes 1. Supported products: 78K0/KD2 and 78K0/KE2 whose flash memory is at least 48 KB, and 78K0/KF2

2. Supported products: 78K0/KD2 and 78K0/KE2 whose flash memory is less than 32 KB, 78K0/KB2, and 78K0/KC2

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

LVI Circuit Characteristics (T_A = –40 to +85°C, $V_{POC} \le V_{DD} = EV_{DD} \le 5.5$ V, $AV_{REF} \le V_{DD}$, $V_{SS} = EV_{SS}$ = 0 V)

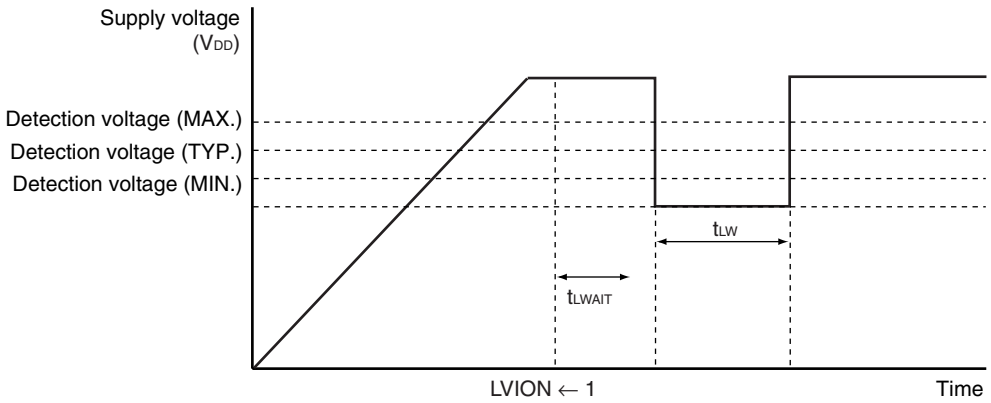
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.14	4.24	4.34	V
		V_{LVI1}		3.99	4.09	4.19	V
		V_{LVI2}		3.83	3.93	4.03	V
		V_{LVI3}		3.68	3.78	3.88	V
		V_{LVI4}		3.52	3.62	3.72	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.06	3.16	3.26	V
		V_{LVI8}		2.91	3.01	3.11	V
		V_{LVI9}		2.75	2.85	2.95	V
		V_{LVI10}		2.60	2.70	2.80	V
		V_{LVI11}		2.45	2.55	2.65	V
		V_{LVI12}		2.29	2.39	2.49	V
		V_{LVI13}		2.14	2.24	2.34	V
		V_{LVI14}		1.98	2.08	2.18	V
		V_{LVI15}		1.83	1.93	2.03	V
	External input pin[Note 1]	EXLVI	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note 2]		t_{LWAIT}		10			μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

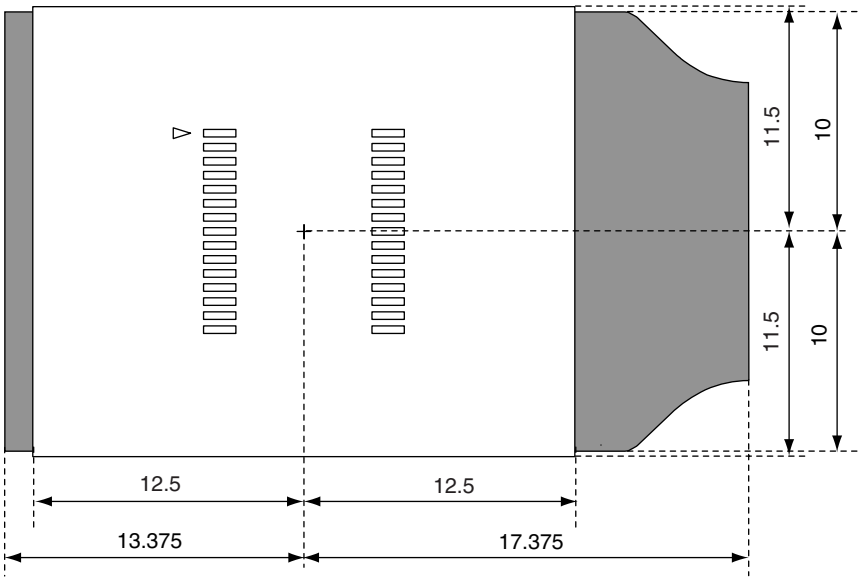
LVI Circuit Timing



APPENDIX B NOTES ON TARGET SYSTEM DESIGN

This chapter shows areas on the target system where component mounting is prohibited and areas where there are component mounting height restrictions when the QB-78K0KX2 is used.

Figure B-1. For 30-Pin MC Package



□ : Exchange adapter area: Components up to 17.45 mm in height can be mounted[Note]

■ : Emulation probe tip area: Components up to 24.45 mm in height can be mounted[Note]

Note Height can be adjusted by using space adapters (each adds 2.4 mm)