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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0546agc-gad-ax

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuits and the recommended connections of unused pins.
See **Figure 2-1** for the configuration of the I/O circuit of each type.

Remark The pins mounted depend on the product. See **1.5 Ordering Information (Top View)** and **2.1 Pin Function List**.

Table 2-3. Pin I/O Circuit Types (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000	5-AQ	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P01/TI010/TO00			
P02/SO11	5-AG		
P03/SI11	**Note 1**		
P04/$\overline{SCK11}$			
P05/TI001/$\overline{SSI11}$			
P06/TI011/TO01			
P10/$\overline{SCK10}$/TxD0	5-AQ		
P11/SI10/RxD0			
P12/SO10	5-AG		
P13/TxD6			
P14/RxD6	5-AQ		
P15/TOH0	5-AG		
P16/TOH1/INTP5	5-AQ		
P17/TI50/TO50			
ANI0/P20 to ANI7/P27[Note 2]	11-G		< Digital input setting and analog input setting> Independently connect to AV_{REF} or AV_{SS} via a resistor. <Digital output setting> Leave open.

Notes 1. "5-AG" type: 78K0/KE2 whose flash memory is less than 32 KB and 78K0/KD2
"5-AQ" type: 78K0/KE2 whose flash memory is at least 48 KB and 78K0/KF2
(Products other than the above are not mounted with P03 to P06.)

2. ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Table 5-3. Port Functions (3/3)

KB2	KC2	KD2	KES	KF2	Function Name	I/O	Function	After Reset	Alternate Function
√	√	√	√	√	P120	I/O	Port 12. I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
√	√	√	√	√	P121				X1/OCD0A Note 3
√	√	√	√	√	P122				X2/EXCLK/ OCD0B Note 3
–	√	√	√	√	P123				XT1
–	√	√	√	√	P124				XT2/EXCLKS
–	Note 1	√	√	√	P130	Output	Port 13. Output-only port.	Output port	–
–	Note 1	√	√	√	P140	I/O	Port 14. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCL/INTP6
–	–	–	Note 2	√	P141				BUZ/BUSY0/ INTP7
–	–	–	–	√	P142				$\overline{\text{SCKA0}}$
–	–	–	–	√	P143				SIA0
–	–	–	–	√	P144				SOA0
–	–	–	–	√	P145				STB0

Notes 1. This is not mounted onto 38-pin and 44-pin products of the 78K0/KC2.

2. The 78K0/KE2 products are not provided with the BUSY0 input function.

3. OCD0A and OCD0B are provided to the products with an on-chip debug function (μPD78F05xxD and 78F05xxDA) only.

Remark √: Mounted, –: Not mounted

Figure 5-43. Format of Pull-up Resistor Option Register (78K0/KF2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00	FF30H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40	FF34H	00H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	FF35H	00H	R/W
PU6	PU67	PU66	PU65	PU64	0	0	0	0	FF36H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	FF37H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	FF3CH	00H	R/W
PU14	0	0	PU145	PU144	PU143	PU142	PU141	PU140	FF3EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 7, 12, 14; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

(4) A/D port configuration register (ADPC)

This register switches the P20/ANI0 to P27/ANI7 pins to digital I/O of port or analog input of A/D converter.

ADPC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark P20/ANI0 to P23/ANI3 pins: 78K0/KB2
P20/ANI0 to P25/ANI5 pins: 38-pin products of 78K0/KC2
P20/ANI0 to P27/ANI7 pins: Products other than above

6.6.5 Clocks supplied to CPU and peripheral hardware

The following table shows the relation among the clocks supplied to the CPU and peripheral hardware, and setting of registers.

Table 6-4. Clocks Supplied to CPU and Peripheral Hardware, and Register Setting (78K0/KB2)

Supplied Clock		XSEL	MCM0	EXCLK
Clock Supplied to CPU	Clock Supplied to Peripheral Hardware			
Internal high-speed oscillation clock		0	×	×
Internal high-speed oscillation clock	X1 clock	1	0	0
	External main system clock	1	0	1
X1 clock		1	1	0
External main system clock		1	1	1

Remarks 1. The 78K0/KB2 is not provided with a subsystem clock.

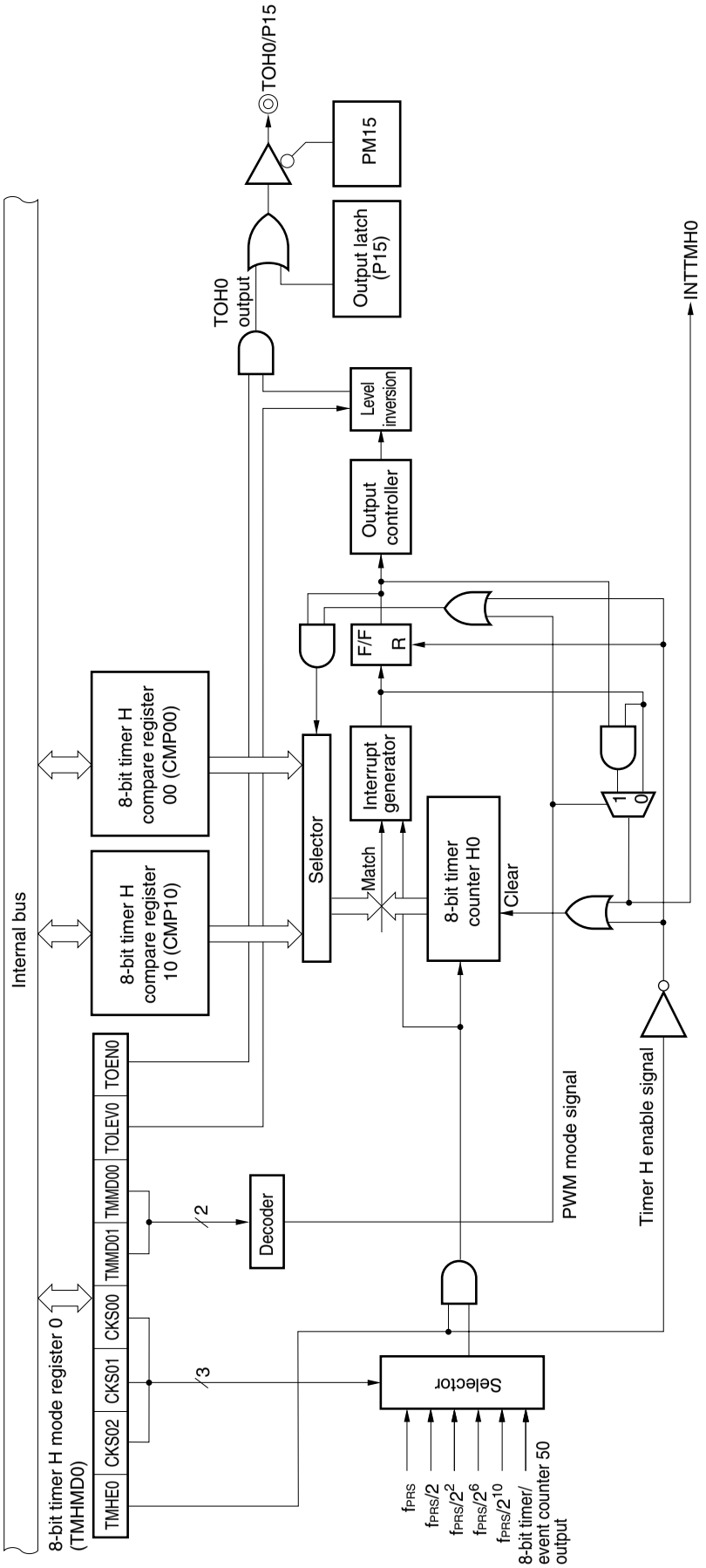
2. XSEL: Bit 2 of the main clock mode register (MCM)
MCM0: Bit 0 of MCM
EXCLK: Bit 7 of the clock operation mode select register (OSCCTL)
×: don't care

Table 6-5. Clocks Supplied to CPU and Peripheral Hardware, and Register Setting (78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2)

Supplied Clock		XSEL	CSS	MCM0	EXCLK
Clock Supplied to CPU	Clock Supplied to Peripheral Hardware				
Internal high-speed oscillation clock		0	0	×	×
Internal high-speed oscillation clock	X1 clock	1	0	0	0
	External main system clock	1	0	0	1
X1 clock		1	0	1	0
External main system clock		1	0	1	1
Subsystem clock	Internal high-speed oscillation clock	0	1	×	×
	X1 clock	1	1	0	0
		1	1	1	0
	External main system clock	1	1	0	1
		1	1	1	1

Remark XSEL: Bit 2 of the main clock mode register (MCM)
CSS: Bit 4 of the processor clock control register (PCC)
MCM0: Bit 0 of MCM
EXCLK: Bit 7 of the clock operation mode select register (OSCCTL)
×: don't care

Figure 9-1. Block Diagram of 8-Bit Timer H0



Notes 2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V ≤ V_{DD} < 2.7 V, the setting of CKS02 = CKS01 = CKS00 = 0 (count clock: f_{PRS}) is prohibited.

3. This is settable only if 4.0 V ≤ V_{DD} ≤ 5.5 V.

4. Note the following points when selecting the TM50 output as the count clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Cautions 1. When TMHE0 = 1, setting the other bits of TMHMD0 is prohibited. However, TMHMD0 can be refreshed (the same value is written).

2. In the PWM output mode, be sure to set the 8-bit timer H compare register 10 (CMP10) when starting the timer count operation (TMHE0 = 1) after the timer count operation was stopped (TMHE0 = 0) (be sure to set again even if setting the same value to CMP10).

3. The actual TOH0/P15 pin output is determined depending on PM15 and P15, besides TOH0 output.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

<10> By performing the procedures above, an arbitrary carrier clock is obtained. To stop the count operation, clear TMHE1 to 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the carrier clock output cycle and duty are as follows.

- Carrier clock output cycle = (N + M + 2)/f_{CNT}
- Duty = High-level width/carrier clock output width = (M + 1)/(N + M + 2)

Cautions 1. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

2. Set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

3. Set the values of the CMP01 and CMP11 registers in a range of 01H to FFH.

4. The set value of the CMP11 register can be changed while the timer counter is operating. However, it takes the duration of three operating clocks (signal selected by the CKS12 to CKS10 bits of the TMHMD1 register) since the value of the CMP11 register has been changed until the value is transferred to the register.

5. Be sure to set the RMC1 bit before the count operation is started.

Remarks 1. For the setting of the output pin, see **9.3 (3) Port mode register 1 (PM1)**.

2. For how to enable the INTTMH1 signal interrupt, see **CHAPTER 20 INTERRUPT FUNCTIONS**.

CHAPTER 12 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

	78K0/KB2	78K0/KC2	78K0/KD2	78K0/KE2	78K0/KF2
Clock output	–	38/44 pins: – 48 pins: √	√		
Buzzer output	–			√	

Remark √: Mounted, –: Not mounted

12.1 Functions of Clock Output/Buzzer Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs. The clock selected with the clock output selection register (CKS) is output.

In addition, the buzzer output is intended for square-wave output of buzzer frequency selected with CKS.

Figure 12-1 and 12-2 show the block diagram of clock output/buzzer output controller.

Figure 12-1. Block Diagram of Clock Output/Buzzer Output Controller (78K0/KD2, 48-pin Products of 78K0/KC2)

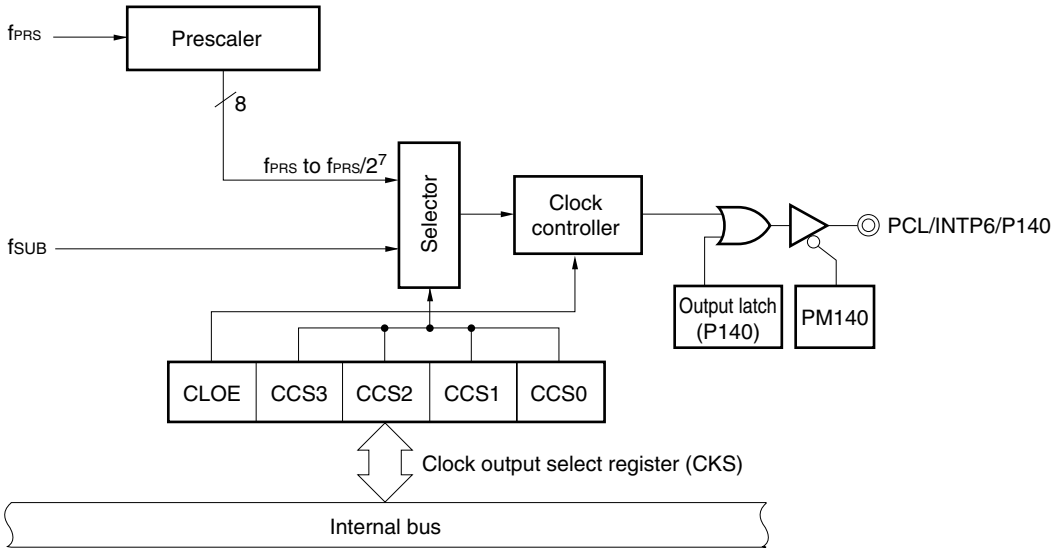


Table 13-2. A/D Conversion Time Selection (Conventional-specification Products (μPD78F05xx and 78F05xxD))

(1) 2.7 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 0)

A/D Converter Mode Register (ADM)					Conversion Time Selection				Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz[Note]	
0	0	0	0	0	264/f_{PRS}	Setting prohibited	26.4 μs	13.2 μs[Note]	f_{PRS}/12
0	0	1	0	0	176/f_{PRS}		17.6 μs	8.8 μs[Note]	f_{PRS}/8
0	1	0	0	0	132/f_{PRS}		13.2 μs	6.6 μs[Note]	f_{PRS}/6
0	1	1	0	0	88/f_{PRS}		8.8 μs[Note]	Setting prohibited	f_{PRS}/4
1	0	0	0	0	66/f_{PRS}	33.0 μs	6.6 μs[Note]		f_{PRS}/3
1	0	1	0	0	44/f_{PRS}	22.0 μs	Setting prohibited		f_{PRS}/2
Other than above					Setting prohibited				

Note This can be set only when 4.0 V ≤ AV_{REF} ≤ 5.5 V.

(2) 2.3 V ≤ AV_{REF} < 2.7 V (LV0 = 1)

A/D Converter Mode Register (ADM)					Conversion Time Selection			Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	
0	0	0	0	1	480/f_{PRS}	Setting prohibited	Setting prohibited	f_{PRS}/12
0	0	1	0	1	320/f_{PRS}		64.0 μs	f_{PRS}/8
0	1	0	0	1	240/f_{PRS}		48.0 μs	f_{PRS}/6
0	1	1	0	1	160/f_{PRS}		32.0 μs	f_{PRS}/4
1	0	0	0	1	120/f_{PRS}	60.0 μs	Setting prohibited	f_{PRS}/3
1	0	1	0	1	80/f_{PRS}	40.0 μs	Setting prohibited	f_{PRS}/2
Other than above					Setting prohibited			

Cautions 1. Set the conversion times with the following conditions.

- **4.0 V ≤ AV_{REF} ≤ 5.5 V: f_{AD} = 0.6 to 3.6 MHz**
- **2.7 V ≤ AV_{REF} < 4.0 V: f_{AD} = 0.6 to 1.8 MHz**
- **2.3 V ≤ AV_{REF} < 2.7 V: f_{AD} = 0.6 to 1.48 MHz (Standard products and (A) grade products only)**

2. When rewriting FR2 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.

3. Change LV0 from the default value, when 2.3 V ≤ AV_{REF} < 2.7 V.

4. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{PRS}: Peripheral hardware clock frequency

Figure 15-5. Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (2/2)

PS61	PS60	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL6	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL6	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

ISRM6	Enables/disables occurrence of reception completion interrupt in case of error
0	“INTSRE6” occurs in case of error (at this time, INTSR6 does not occur).
1	“INTSR6” occurs in case of error (at this time, INTSRE6 does not occur).

Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE6) of asynchronous serial interface reception error status register 6 (ASIS6) is not set and the error interrupt does not occur.

Cautions
1. **To start the transmission, set POWER6 to 1 and then set TXE6 to 1. To stop the transmission, clear TXE6 to 0, and then clear POWER6 to 0.**
2. **To start the reception, set POWER6 to 1 and then set RXE6 to 1. To stop the reception, clear RXE6 to 0, and then clear POWER6 to 0.**
3. **Set POWER6 to 1 and then set RXE6 to 1 while a high level is input to the RxD6 pin. If POWER6 is set to 1 and RXE6 is set to 1 while a low level is input, reception is started.**
4. **TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.**
5. **Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.**
6. **Clear the TXE6 and RXE6 bits to 0 before rewriting the PS61, PS60, and CL6 bits.**
7. **Fix the PS61 and PS60 bits to 0 when used in LIN communication operation.**
8. **Clear TXE6 to 0 before rewriting the SL6 bit. Reception is always performed with “the number of stop bits = 1”, and therefore, is not affected by the set value of the SL6 bit.**
9. **Make sure that RXE6 = 0 when rewriting the ISRM6 bit.**

15.4.2 Asynchronous serial interface (UART) mode

In this mode, data of 1 byte is transmitted/received following a start bit, and a full-duplex operation can be performed.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Registers used

- Asynchronous serial interface operation mode register 6 (ASIM6)
- Asynchronous serial interface reception error status register 6 (ASIS6)
- Asynchronous serial interface transmission status register 6 (ASIF6)
- Clock selection register 6 (CKSR6)
- Baud rate generator control register 6 (BRGC6)
- Asynchronous serial interface control register 6 (ASICL6)
- Input switch control register (ISC)
- Port mode register 1 (PM1)
- Port register 1 (P1)

The basic procedure of setting an operation in the UART mode is as follows.

<1> Set the CKSR6 register (see **Figure 15-8**).
<2> Set the BRGC6 register (see **Figure 15-9**).
<3> Set bits 0 to 4 (ISRM6, SL6, CL6, PS60, PS61) of the ASIM6 register (see **Figure 15-5**).
<4> Set bits 0 and 1 (TXDLV6, DIR6) of the ASICL6 register (see **Figure 15-10**).
<5> Set bit 7 (POWER6) of the ASIM6 register to 1.
<6> Set bit 6 (TXE6) of the ASIM6 register to 1. → Transmission is enabled.
Set bit 5 (RXE6) of the ASIM6 register to 1. → Reception is enabled.
<7> Write data to transmit buffer register 6 (TXB6). → Data transmission is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 15-2. Relationship Between Register Settings and Pins

POWER6	TXE6	RXE6	PM13	P13	PM14	P14	UART6 Operation	Pin Function	
								TxD6/P13	RxD6/P14
0	0	0	×Note	×Note	×Note	×Note	Stop	P13	P14
1	0	1	×Note	×Note	1	×	Reception	P13	RxD6
	1	0	0	1	×Note	×Note	Transmission	TxD6	P14
	1	1	0	1	1	×	Transmission/ reception	TxD6	RxD6

Note Can be set as port function.

Remark ×: don't care
POWER6: Bit 7 of asynchronous serial interface operation mode register 6 (ASIM6)
TXE6: Bit 6 of ASIM6
RXE6: Bit 5 of ASIM6
PM1×: Port mode register
P1×: Port output latch

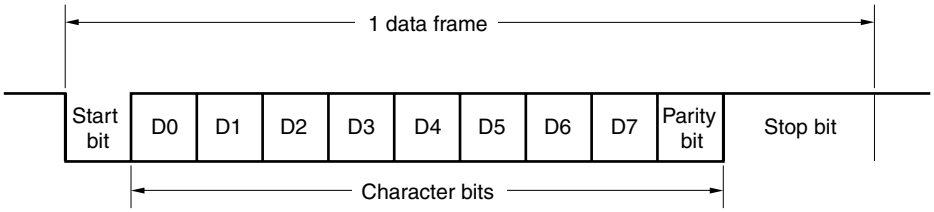
(2) Communication operation

(a) Format and waveform example of normal transmit/receive data

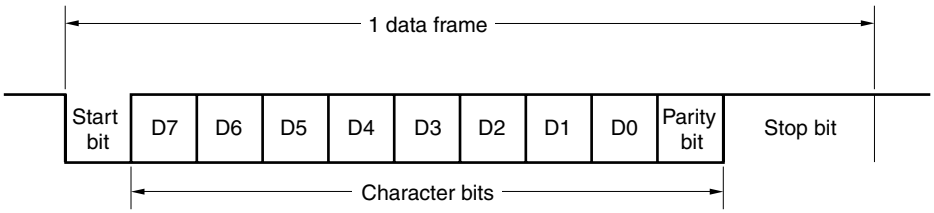
Figures 15-13 and 15-14 show the format and waveform example of the normal transmit/receive data.

Figure 15-13. Format of Normal UART Transmit/Receive Data

1. LSB-first transmission/reception



2. MSB-first transmission/reception



One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 6 (ASIM6).

Whether data is communicated with the LSB or MSB first is specified by bit 1 (DIR6) of asynchronous serial interface control register 6 (ASICL6).

Whether the TxD6 pin outputs normal or inverted data is specified by bit 0 (TXDLV6) of ASICL6.

Table 16-2. Relationship Between Register Settings and Pins (2/2)

(b) Serial interface CSI11

CSIE11	TRMD11	SSE11	PM03	P03	PM02	P02	PM04	P04	PM05	P05	CSI11 Operation	Pin Function			
												SI11/ P03	SO11/ P02	$\overline{\text{SCK11}}$/ P04	$\overline{\text{SSI11}}$/ TI001/P05
0	0	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Stop	P03	P02Note 2	P04Note 3	TI001/ P05
1	0	0	1	×	×Note 1	×Note 1	1	×	×Note 1	×Note 1	Slave reception Note 4	SI11	P02Note 2	$\overline{\text{SCK11}}$ (input) Note 4	TI001/ P05
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	×Note 1	×Note 1	0	0	1	×	×Note 1	×Note 1	Slave transmission Note 4	P03	SO11	$\overline{\text{SCK11}}$ (input) Note 4	TI001/ P05
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	1	×	0	0	1	×	×Note 1	×Note 1	Slave transmission/ reception Note 4	SI11	SO11	$\overline{\text{SCK11}}$ (input) Note 4	TI001/ P05
		1							1	×					$\overline{\text{SSI11}}$
1	0	0	1	×	×Note 1	×Note 1	0	1	×Note 1	×Note 1	Master reception	SI11	P02Note 2	$\overline{\text{SCK11}}$ (output)	TI001/ P05
1	1	0	×Note 1	×Note 1	0	0	0	1	×Note 1	×Note 1	Master transmission	P03	SO11	$\overline{\text{SCK11}}$ (output)	TI001/ P05
1	1	0	1	×	0	0	0	1	×Note 1	×Note 1	Master transmission/ reception	SI11	SO11	$\overline{\text{SCK11}}$ (output)	TI001/ P05

Notes 1. Can be set as port function.

2. To use P02/SO11 as general-purpose port, set the serial clock selection register 11 (CSIC11) in the default status (00H).

3 To use P04/$\overline{\text{SCK11}}$ as port pins, clear CKP11 to 0.

4 To use the slave mode, set CKS112, CKS111, and CKS110 to 1, 1, 1.

Remark ×: don't care

CSIE11: Bit 7 of serial operation mode register 11 (CSIM11)

TRMD11: Bit 6 of CSIM11

CKP11: Bit 4 of serial clock selection register 11 (CSIC11)

CKS112, CKS111, CKS110: Bits 2 to 0 of CSIC11

PM0×: Port mode register

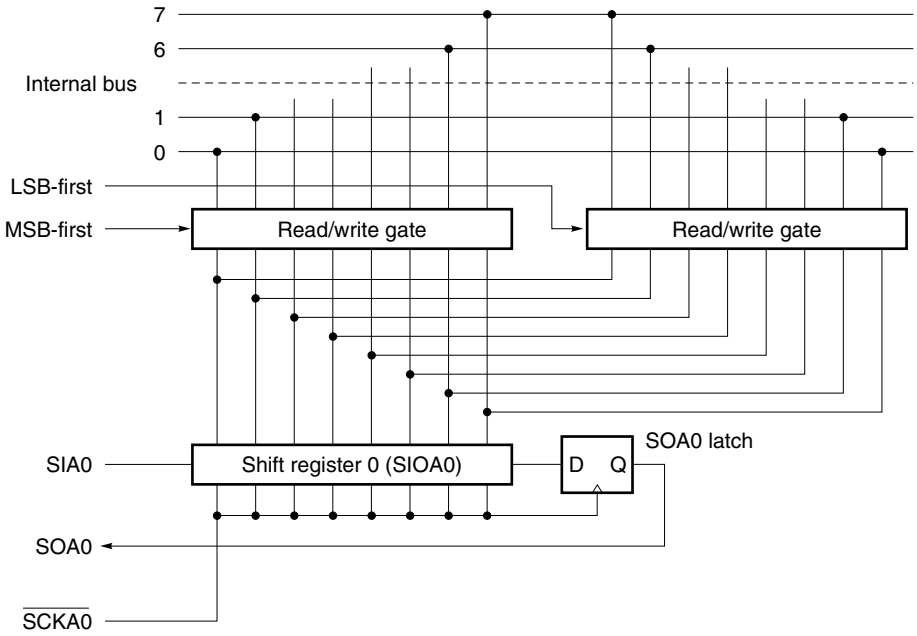
P0×: Port output latch

(c) Switching MSB/LSB as start bit

Figure 17-12 shows the configuration of serial I/O shift register 0 (SIOA0) and the internal bus. As shown in the figure, MSB/LSB can be read/written in reverse form.

Switching MSB/LSB as the start bit can be specified using bit 1 (DIR0) of serial operation mode specification register 0 (CSIMA0).

Figure 17-12. Transfer Bit Order Switching Circuit



Start bit switching is realized by switching the bit order for data written to SIOA0. The SIOA0 shift order remains unchanged.

Thus, switching between MSB-first and LSB-first must be performed before writing data to the shift register.

(d) Communication start

Serial communication is started by setting communication data to serial I/O shift register 0 (SIOA0) when the following two conditions are satisfied.

- Serial interface CSIA0 operation control bit (CSIAE0) = 1
- Serial communication is not in progress

Caution If CSIAE0 is set to 1 after data is written to SIOA0, communication does not start.

Upon termination of 8-bit communication, serial communication automatically stops and the interrupt request flag (ACSIIF) is set.

Figure 20-10. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KE2)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	SREMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK010	TMMK000	TMMK50	TMMKH0	TMMKH1	DUALMK0 CSIMK10 STMK0	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	PMK7	PMK6	WTMK	KRMK	TMMK51	WTIMK	SRMK0	ADMK

Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
MK1H	1	1	1	1	TMMK011[Note]	TMMK001[Note]	CSIMK11[Note]	IICMK0 DMUMK[Note]

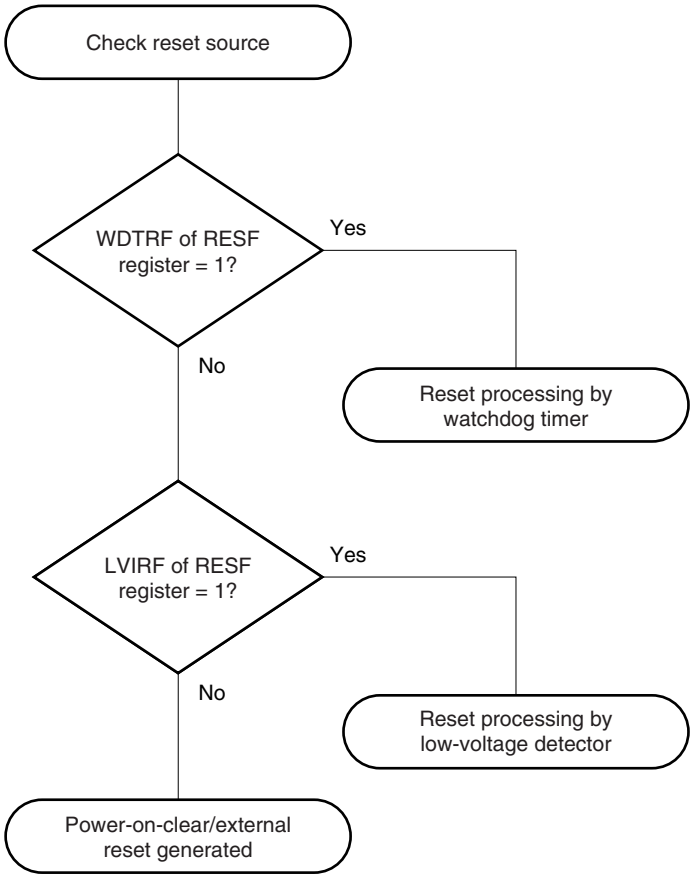
XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note Products whose flash memory is at least 48 KB only.

Caution Be sure to set bits 1 to 7 of MK1H to 1 for the products whose flash memory is less than 32 KB. Be sure to set bits 4 to 7 of MK1H to 1 for the products whose flash memory is at least 48 KB.

Figure 24-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source



Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	−10	mA
		Total of all pins −80 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	−25	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P64 to P67, P70 to P77	−55	mA
		Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
		Per pin	P121 to P124	−1	mA
		Total of all pins		−4	mA
Output current, low	I_{OL}	Per pin	P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P120, P130, P140 to P145	30	mA
		Total of all pins 200 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	60	mA
			P05, P06, P10 to P17, P30 to P33, P50 to P57, P60 to P67, P70 to P77	140	mA
		Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
		Per pin	P121 to P124	4	mA
		Total of all pins		10	mA
Operating ambient temperature	T_A			−40 to +125	°C
Storage temperature	T_{stg}			−65 to +150	°C

Cautions 1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

DC Characteristics (1/4)

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V			−1.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			−1.0	mA
		Total of P00 to P04, P40 to P47, P120, P130, P140 to P145[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			−6.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−4.0	mA
		Total of P05, P06, P10 to P17, P30 to P33, P50 to P57, P64 to P67, P70 to P77[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			−10.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−8.0	mA
		Total of all the pins above[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			−14.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−12.0	mA
	I_{OH2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			−0.1	mA
		Per pin for P121 to P124				−0.1	mA
Output current, low[Note 2]	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30 to P33, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P120, P130, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V			4.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			2.0	mA
		Per pin for P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V			8.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			2.0	mA
		Total of P00 to P04, P40 to P47, P120, P130, P140 to P145[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			10.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			8.0	mA
		Total of P05, P06, P10 to P17, P30 to P33, P50 to P57, P60 to P67, P70 to P77[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			16.0	mA
		Total of all the pins above[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			24.0	mA
	I_{OL2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			0.4	mA
		Per pin for P121 to P124				0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

3. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(50 × 0.01) = −14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution at the beginning of this chapter.

AC Characteristics

(1) Basic operation (1/2)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

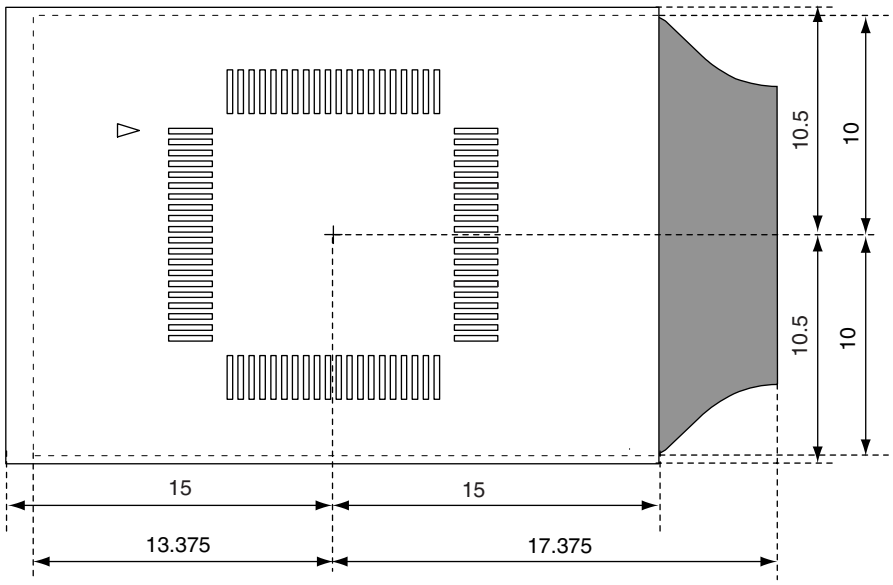
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	Conventional-specification Products (μPD78F05xx (A2))	4.0 V ≤ V_{DD} ≤ 5.5 V	0.1		32	μs
				2.7 V ≤ V_{DD} < 4.0 V	0.2		32	μs
			Expanded-specification Products (μPD78F05xxA (A2))	2.7 V ≤ V_{DD} ≤ 5.5 V	0.1		32	μs
		Subsystem clock (f_{SUB}) operation[Note 1]			114	122	125	μs
Peripheral hardware clock frequency	f_{PRS}	f_{PRS} = f_{XH} (XSEL = 1)	Conventional-specification Products (μPD78F05xx (A2))	4.0 V ≤ V_{DD} ≤ 5.5 V			20	MHz
				2.7 V ≤ V_{DD} < 4.0 V			10	MHz
			Expanded-specification Products (μPD78F05xxA (A2))	4.0 V ≤ V_{DD} ≤ 5.5 V			20	MHz
				2.7 V ≤ V_{DD} < 4.0 V [Note 2]			20	MHz
		f_{PRS} = f_{RH} (XSEL = 0)		2.7 V ≤ V_{DD} ≤ 5.5 V	7.6		8.4	MHz
External main system clock frequency	f_{EXCLK}	Conventional-specification Products (μPD78F05xx(A2))		4.0 V ≤ V_{DD} ≤ 5.5 V	1.0[Note 3]		20.0	MHz
				2.7 V ≤ V_{DD} < 4.0 V	1.0[Note 3]		10.0	MHz
		Expanded-specification Products (μPD78F05xxA(A2))		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0[Note 3]		20.0	MHz
External main system clock input high-level width, low-level width	t_{EXCLKH}, t_{EXCLKL}	Conventional-specification Products (μPD78F05xx(A2))		4.0 V ≤ V_{DD} ≤ 5.5 V	24			ns
				2.7 V ≤ V_{DD} < 4.0 V	48			ns
		Expanded-specification Products (μPD78F05xxA(A2))		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns

Notes 1. The 78K0/KB2 is not provided with a subsystem clock.

2. Characteristics of the main system clock frequency. Set the division clock to be set by a peripheral function to f_{XH}/2 (10 MHz) or less. The multiplier/divider, however, can operate on f_{XH} (20 MHz).

3. 2.0 MHz (MIN.) when using UART6 during on-board programming.

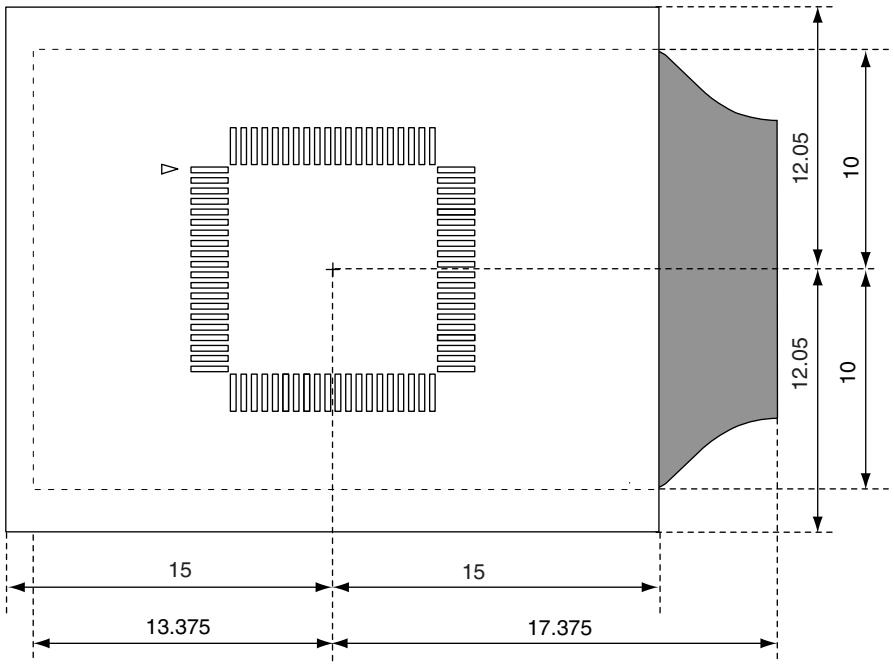
Figure B-10. For 64-Pin GK Package



□ : Exchange adapter area: Components up to 17.45 mm in height can be mounted[Note]
■ : Emulation probe tip area: Components up to 24.45 mm in height can be mounted[Note]

Note Height can be adjusted by using space adapters (each adds 2.4 mm)

Figure B-11. For 80-Pin GC Package



□ : Exchange adapter area: Components up to 17.45 mm in height can be mounted[Note]
■ : Emulation probe tip area: Components up to 24.45 mm in height can be mounted[Note]

Note Height can be adjusted by using space adapters (each adds 2.4 mm)