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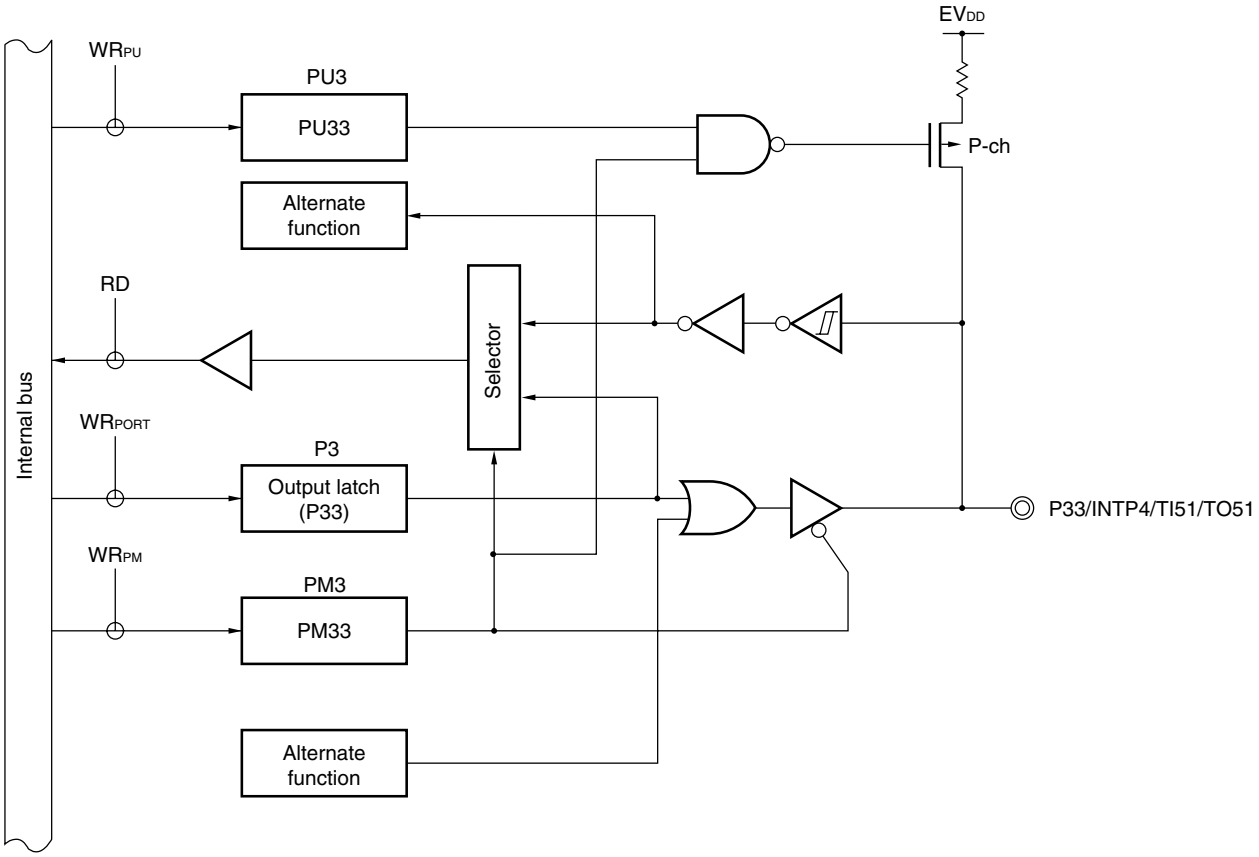
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0547agk-gak-ax

Figure 5-14. Block Diagram of P33

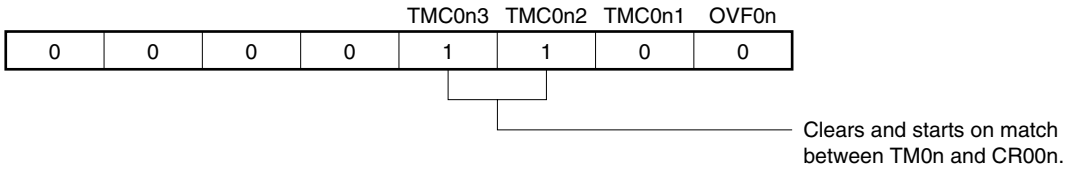


P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

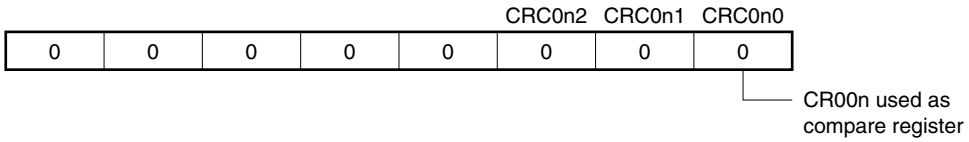
Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 7-22. Example of Register Settings for Square-Wave Output Operation

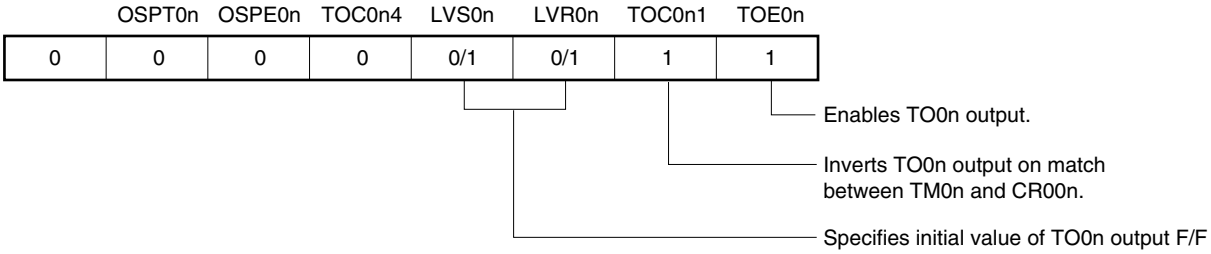
(a) 16-bit timer mode control register 0n (TMC0n)



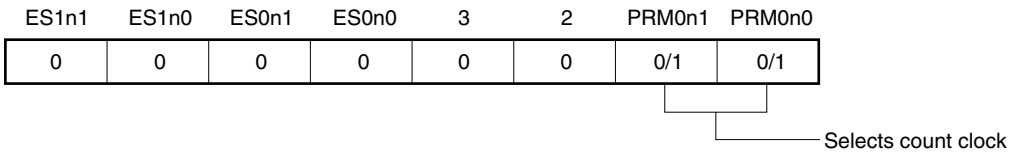
(b) Capture/compare control register 0n (CRC0n)



(c) 16-bit timer output control register 0n (TOC0n)



(d) Prescaler mode register 0n (PRM0n)



(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

If M is set to CR00n, the interval time is as follows.

- Square wave frequency = 1 / [2 × (M + 1) × Count clock cycle]

Setting CR00n to 0000H is prohibited.

(g) 16-bit capture/compare register 01n (CR01n)

Usually, CR01n is not used for the square-wave output function. However, a compare match interrupt (INTTM01n) is generated when the set value of CR01n matches the value of TM0n.

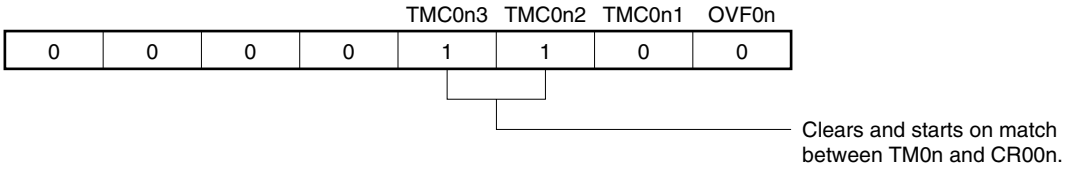
Therefore, mask the interrupt request by using the interrupt mask flag (TMMK01n).

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

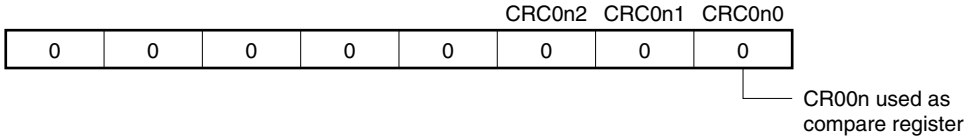
n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-25. Example of Register Settings in External Event Counter Mode (1/2)

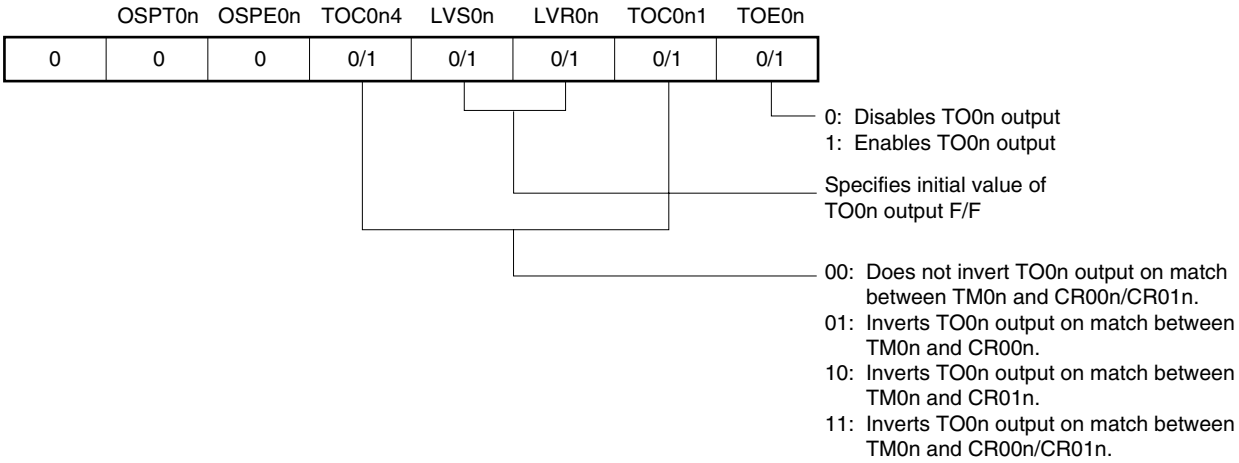
(a) 16-bit timer mode control register 0n (TMC0n)



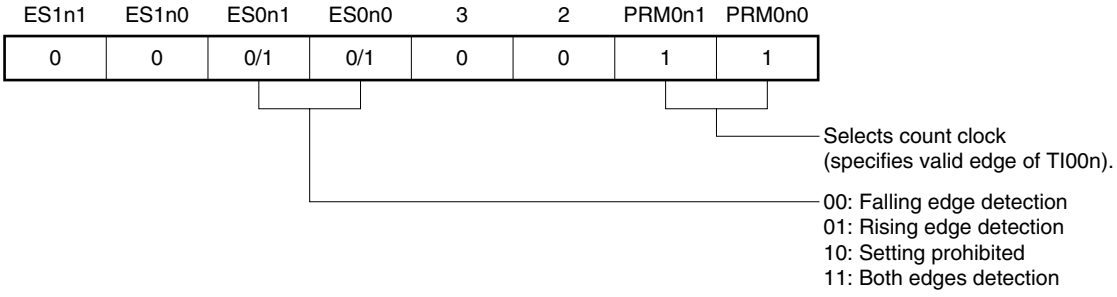
(b) Capture/compare control register 0n (CRC0n)



(c) 16-bit timer output control register 0n (TOC0n)



(d) Prescaler mode register 0n (PRM0n)

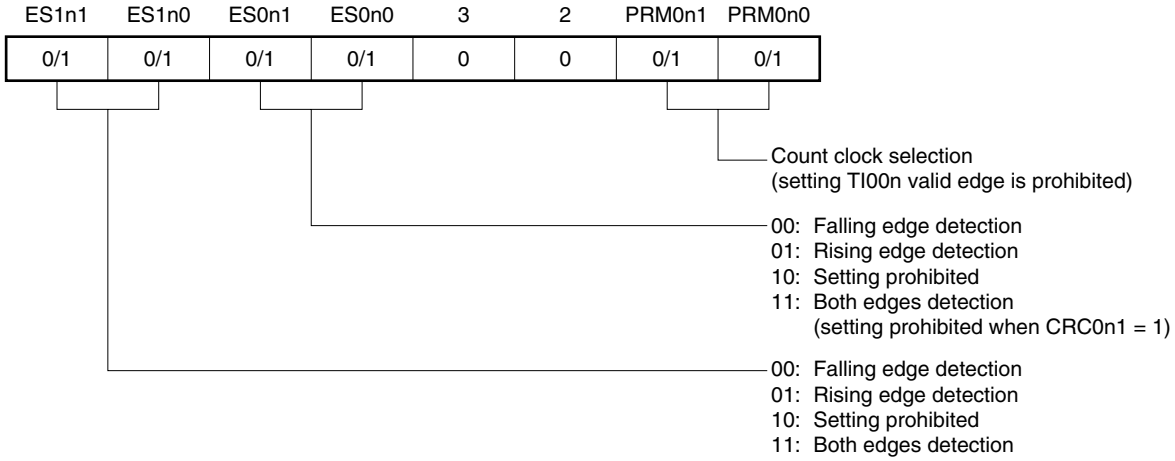


Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Figure 7-35. Example of Register Settings in Clear & Start Mode Entered by TI00n Pin Valid Edge Input (2/2)

(d) Prescaler mode register 0n (PRM0n)



(e) 16-bit timer counter 0n (TM0n)

By reading TM0n, the count value can be read.

(f) 16-bit capture/compare register 00n (CR00n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM00n) is generated. The count value of TM0n is not cleared.

To use this register as a capture register, select either the TI00n or TI01n pin[Note] input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR00n.

Note The timer output (TO0n) cannot be used when detection of the valid edge of the TI01n pin is used.

(g) 16-bit capture/compare register 01n (CR01n)

When this register is used as a compare register and when its value matches the count value of TM0n, an interrupt signal (INTTM01n) is generated. The count value of TM0n is not cleared.

When this register is used as a capture register, the TI00n pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM0n is stored in CR01n.

Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

Caution Do not change the count clock and interval time (by setting bits 4 to 7 (WTM4 to WTM7) of WTM) during watch timer operation.

Remarks 1. f_W: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

10.4 Watch Timer Operations

10.4.1 Watch timer operation

The watch timer generates an interrupt request signal (INTWT) at a specific time interval by using the peripheral hardware clock or subsystem clock.

When bit 0 (WTM0) and bit 1 (WTM1) of the watch timer operation mode register (WTM) are set to 1, the count operation starts. When these bits are cleared to 0, the 5-bit counter is cleared and the count operation stops.

When the interval timer is simultaneously operated, zero-second start can be achieved only for the watch timer by clearing WTM1 to 0. In this case, however, the 11-bit prescaler is not cleared. Therefore, an error up to $2^9 \times 1/fw$ seconds occurs in the first overflow (INTWT) after zero-second start.

The interrupt request is generated at the following time intervals.

Table 10-4. Watch Timer Interrupt Time

WTM3	WTM2	Interrupt Time Selection	When Operated at f_{SUB} = 32.768 kHz (WTM7 = 1)	When Operated at f_{PRS} = 2 MHz (WTM7 = 0)	When Operated at f_{PRS} = 5 MHz (WTM7 = 0)	When Operated at f_{PRS} = 10 MHz (WTM7 = 0)	When Operated at f_{PRS} = 20 MHz (WTM7 = 0)
0	0	$2^{14}/fw$	0.5 s	1.05 s	0.419 s	0.210 s	0.105 s
0	1	$2^{13}/fw$	0.25 s	0.52 s	0.210 s	0.105 s	52.5 ms
1	0	$2^5/fw$	977 μs	2.05 ms	819 μs	410 μs	205 μs
1	1	$2^4/fw$	488 μs	1.02 ms	410 μs	205 μs	102 μs

Remarks 1. fw: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

10.4.2 Interval timer operation

The watch timer operates as interval timer which generates interrupt request signals (INTWTI) repeatedly at an interval of the preset count value.

The interval time can be selected with bits 4 to 6 (WTM4 to WTM6) of the watch timer operation mode register (WTM).

When bit 0 (WTM0) of the WTM is set to 1, the count operation starts. When this bit is set to 0, the count operation stops.

Table 10-5. Interval Timer Interval Time

WTM6	WTM5	WTM4	Interval Time	When Operated at f_{SUB} = 32.768 kHz (WTM7 = 1)	When Operated at f_{PRS} = 2 MHz (WTM7 = 0)	When Operated at f_{PRS} = 5 MHz (WTM7 = 0)	When Operated at f_{PRS} = 10 MHz (WTM7 = 0)	When Operated at f_{PRS} = 20 MHz (WTM7 = 0)
0	0	0	$2^4/fw$	488 μs	1.02 ms	410 μs	205 μs	102 μs
0	0	1	$2^5/fw$	977 μs	2.05 ms	820 μs	410 μs	205 μs
0	1	0	$2^6/fw$	1.95 ms	4.10 ms	1.64 ms	820 μs	410 μs
0	1	1	$2^7/fw$	3.91 ms	8.20 ms	3.28 ms	1.64 ms	820 μs
1	0	0	$2^8/fw$	7.81 ms	16.4 ms	6.55 ms	3.28 ms	1.64 ms
1	0	1	$2^9/fw$	15.6 ms	32.8 ms	13.1 ms	6.55 ms	3.28 ms
1	1	0	$2^{10}/fw$	31.3 ms	65.5 ms	26.2 ms	13.1 ms	6.55 ms
1	1	1	$2^{11}/fw$	62.5 ms	131.1 ms	52.4 ms	26.2 ms	13.1 ms

Remarks 1. fw: Watch timer clock frequency ($f_{PRS}/2^7$ or f_{SUB})

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{SUB}: Subsystem clock frequency

12.4 Operations of Clock Output/Buzzer Output Controller

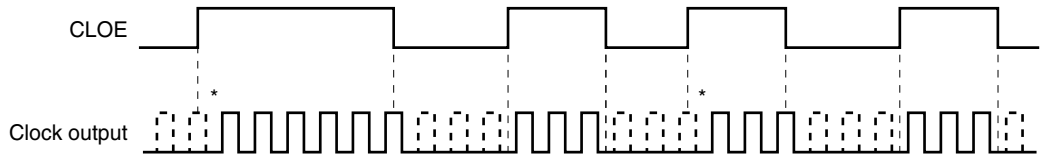
12.4.1 Operation as clock output

The clock pulse is output as the following procedure.

<1> Select the clock pulse output frequency with bits 0 to 3 (CCS0 to CCS3) of the clock output selection register (CKS) (clock pulse output in disabled status).
<2> Set bit 4 (CLOE) of CKS to 1 to enable clock output.

Remark The clock output controller is designed not to output pulses with a small width during output enable/disable switching of the clock output. As shown in Figure 12-6, be sure to start output from the low period of the clock (marked with * in the figure). When stopping output, do so after the high-level period of the clock.

Figure 12-6. Remote Control Output Application Example



12.4.2 Operation as buzzer output

The buzzer frequency is output as the following procedure.

<1> Select the buzzer output frequency with bits 5 and 6 (BCS0, BCS1) of the clock output selection register (CKS) (buzzer output in disabled status).
<2> Set bit 7 (BZOE) of CKS to 1 to enable buzzer output.

(1) Receive buffer register 0 (RXB0)

This 8-bit register stores parallel data converted by receive shift register 0 (RXS0).

Each time 1 byte of data has been received, new receive data is transferred to this register from receive shift register 0 (RXS0).

If the data length is set to 7 bits the receive data is transferred to bits 0 to 6 of RXB0 and the MSB of RXB0 is always 0.

If an overrun error (OVE0) occurs, the receive data is not transferred to RXB0.

RXB0 can be read by an 8-bit memory manipulation instruction. No data can be written to this register.

Reset signal generation and POWER0 = 0 set this register to FFH.

(2) Receive shift register 0 (RXS0)

This register converts the serial data input to the RxD0 pin into parallel data.

RXS0 cannot be directly manipulated by a program.

(3) Transmit shift register 0 (TXS0)

This register is used to set transmit data. Transmission is started when data is written to TXS0, and serial data is transmitted from the TxD0 pins.

TXS0 can be written by an 8-bit memory manipulation instruction. This register cannot be read.

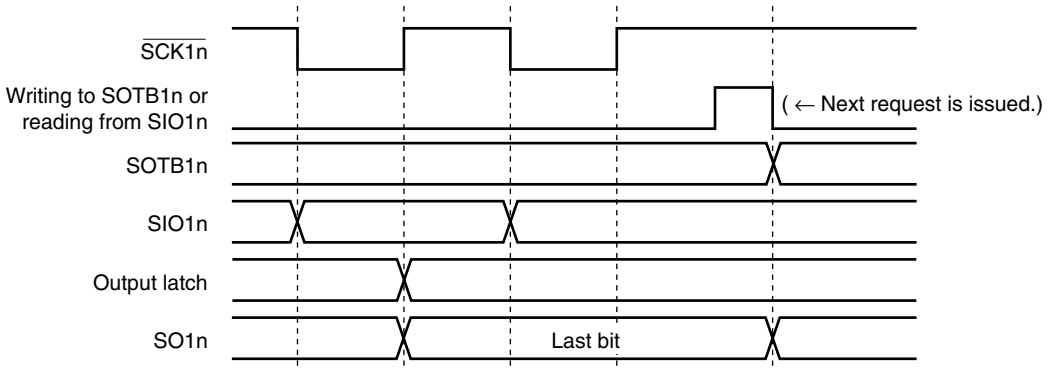
Reset signal generation, POWER0 = 0, and TXE0 = 0 set this register to FFH.

Cautions 1. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

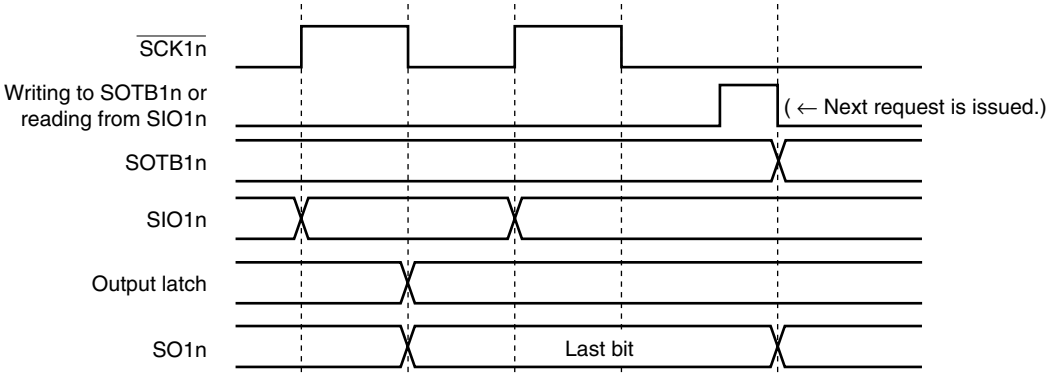
2. Do not write the next transmit data to TXS0 before the transmission completion interrupt signal (INTST0) is generated.

Figure 16-12. Output Value of SO1n Pin (Last Bit) (2/2)

(c) Type 2: CKP1n = 0, DAP1n = 1



(d) Type 4: CKP1n = 1, DAP1n = 1



Remark n = 0: 78K0/KE2 products whose flash memory is less than 32 KB, and 78K0/KB2, 78K0/KC2, 78K0/KD2 products

n = 0, 1: 78K0/KE2 products whose flash memory is at least 48 KB, and 78K0/KF2 products

(b) Automatic transmission mode

In this mode, the specified data is transmitted in 8-bit unit.

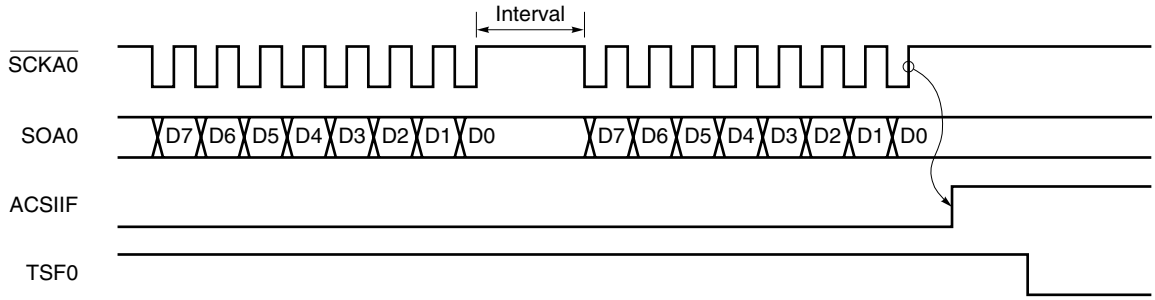
Serial communication is started when bit 0 (ATSTA0) of serial trigger register 0 (CSIT0) is set to 1 while bit 7 (CSIAE0), bit 6 (ATE0), and bit 3 (TXEA0) of serial operation mode specification register 0 (CSIMA0) are set to 1.

When the final byte has been transmitted, an interrupt request flag (ACSIIF) is set. The termination of automatic transmission can also be judged by bit 0 (TSF0) of serial status register 0 (CSIS0).

If a receive operation, busy control and strobe control are not executed, the SIA0/P143, BUSY0/BUZ/INTP7/P141, and STB0/P145 pins can be used as normal I/O port pins.

Figure 17-17 shows the example of the automatic transmission mode operation timing, and Figure 17-18 shows the operation flowchart.

Figure 17-17. Example of Automatic Transmission Mode Operation Timing



Cautions 1. Because, in the automatic transmission mode, the automatic transmit/receive function reads data from the internal buffer RAM after 1-byte transmission, an interval is inserted until the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the interval is dependent upon the value of automatic data transfer interval specification register 0 (ADTI0) and the set values of bits 5 and 4 (STBE0, BUSYE0) of serial status register 0 (CSIS0) (see (5) Automatic transmit/receive interval time).

2. If an access to the buffer RAM by the CPU conflicts with an access to the buffer RAM by serial interface CSIA0 during the interval period, the interval time specified by automatic data transfer interval specification register 0 (ADTI0) may be extended.

Remark ACSIIF: Interrupt request flag
TSF0: Bit 0 of serial status register 0 (CSIS0)

18.5.14 Communication reservation

(1) When communication reservation function is enabled (bit 0 (IICRSV) of IIC flag register 0 (IICF0) = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released when bit 6 (LREL0) of IIC control register 0 (IICC0) was set to 1).

If bit 1 (STT0) of IICC0 is set to 1 while the bus is not used (after a stop condition is detected), a start condition is automatically generated and wait state is set.
If an address is written to IIC shift register 0 (IIC0) after bit 4 (SPIE0) of IICC0 was set to 1, and it was detected by generation of an interrupt request signal (INTIIC0) that the bus was released (detection of the stop condition), then the device automatically starts communication as the master. Data written to IIC0 before the stop condition is detected is invalid.
When STT0 has been set to 1, the operation mode (as start condition or as communication reservation) is determined according to the bus status.

- If the bus has been released ..... a start condition is generated
- If the bus has not been released (standby mode)..... communication reservation

Check whether the communication reservation operates or not by using MSTS0 bit (bit 7 of IIC status register 0 (IICS0)) after STT0 bit is set to 1 and the wait time elapses.
The wait periods, which should be set via software, are listed in Table 18-6.

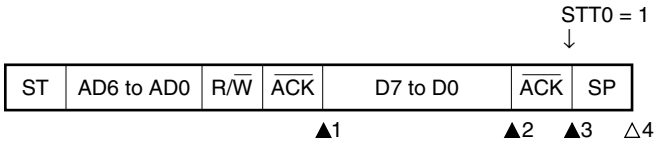
Table 18-6. Wait Periods

CLX0	SMC0	CL01	CL00	Wait Period
0	0	0	0	46 clocks
0	0	0	1	86 clocks
0	0	1	0	172 clocks
0	0	1	1	34 clocks
0	1	0	0	30 clocks
0	1	0	1	
0	1	1	0	60 clocks
0	1	1	1	12 clocks
1	1	0	0	18 clocks
1	1	0	1	
1	1	1	0	36 clocks

Figure 18-20 shows the communication reservation timing.

(g) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

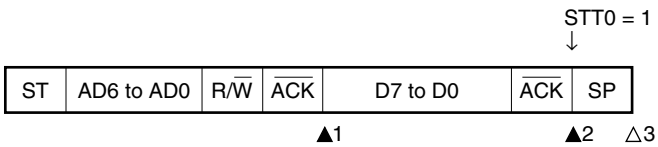
(i) When WTIM0 = 0



▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000×000B (Sets WTIM0 to 1)
▲3: IICS0 = 1000××00B (Sets STT0 to 1)
△4: IICS0 = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1

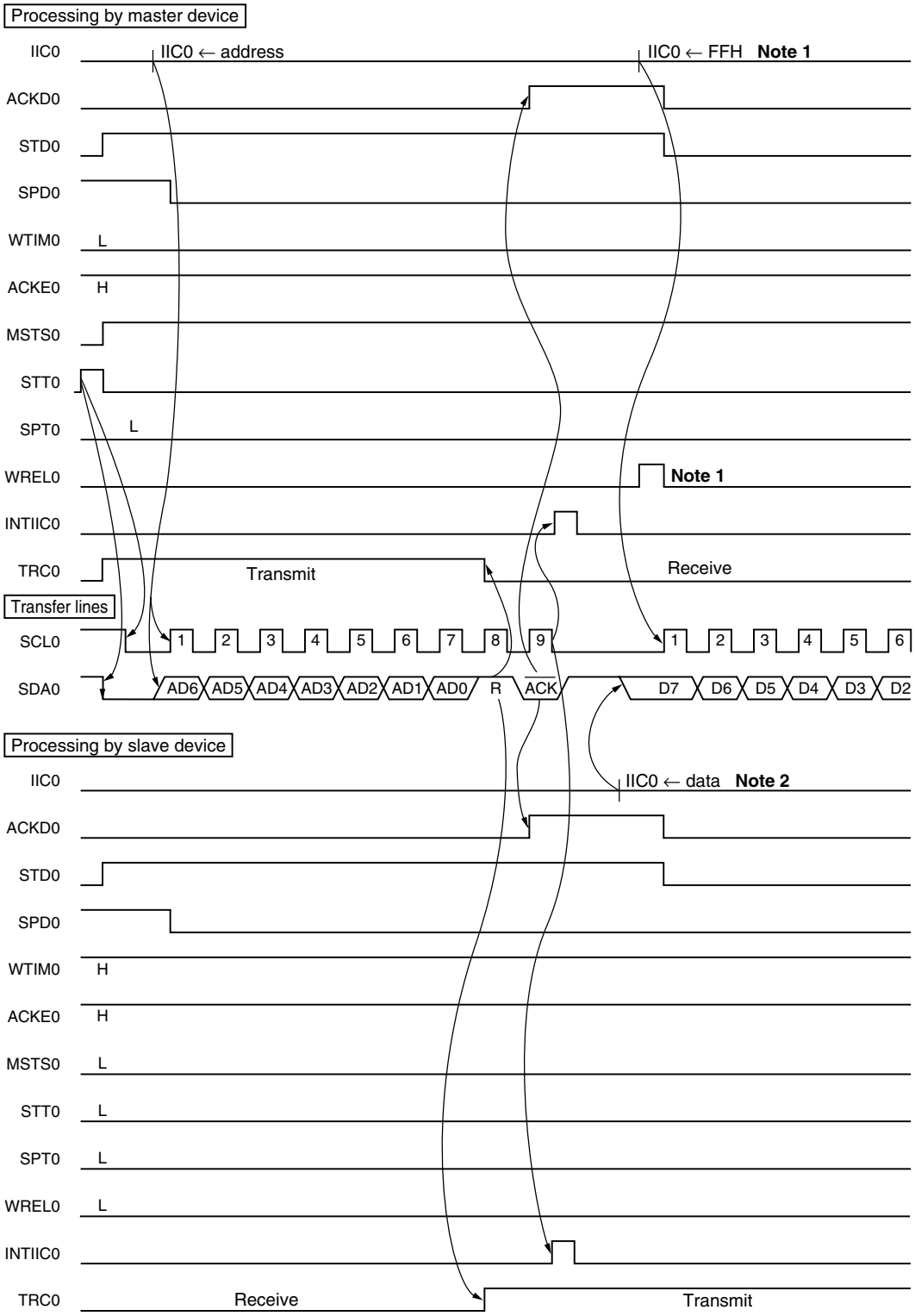


▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000××00B (Sets STT0 to 1)
△3: IICS0 = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 18-28. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address

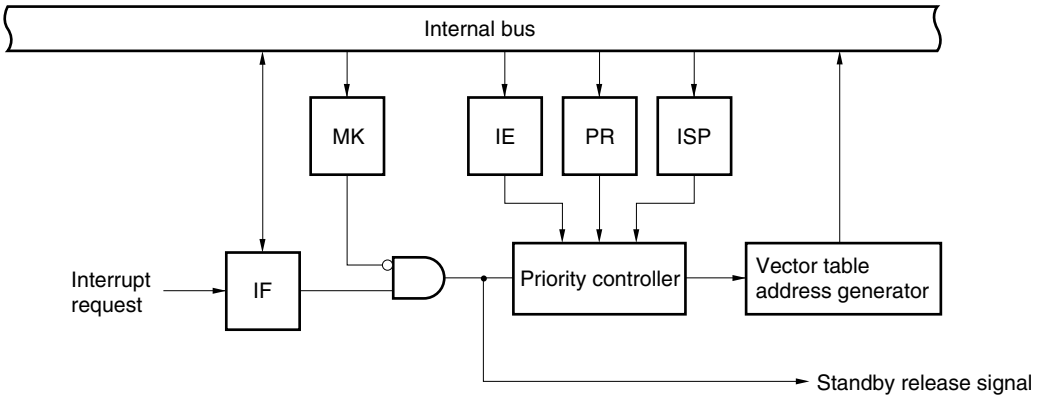


Notes 1. To cancel master wait, write “FFH” to IIC0 or set WREL0.

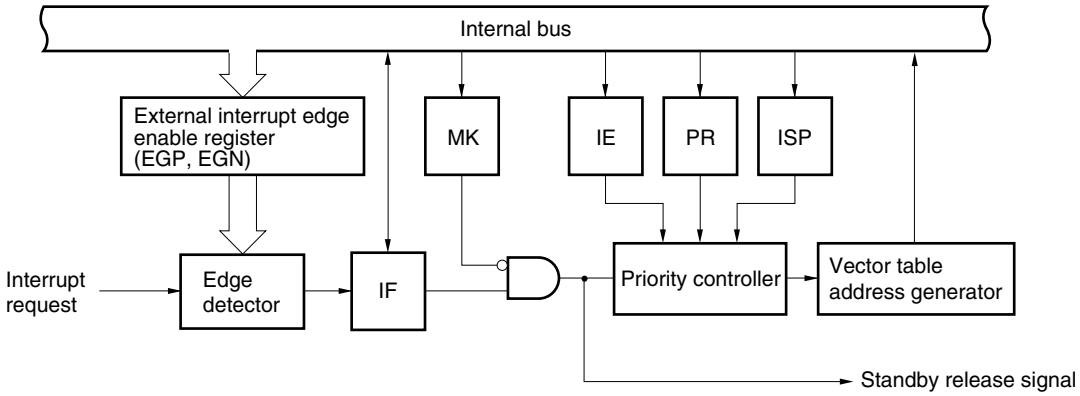
2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

Figure 20-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal maskable interrupt



(B) External maskable interrupt (INTPn)



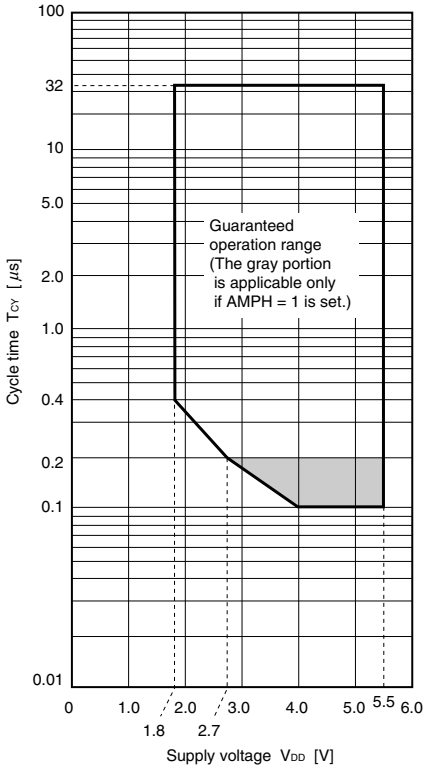
Remark n = 0 to 5: 78K0/KB2, 38-pin and 44-pin products of 78K0/KC2
n = 0 to 6: 78K0/KD2, 48-pin products of 78K0/KC2
n = 0 to 7: 78K0/KE2, 78K0/KF2

IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

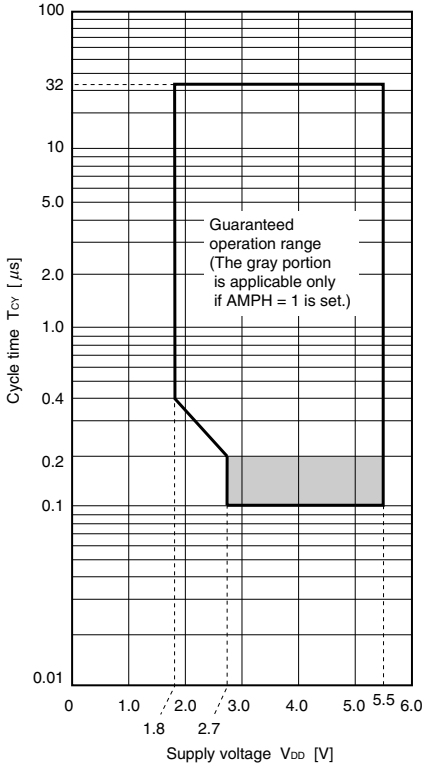
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

T_{CY} vs. V_{DD} (Main System Clock Operation)

<1> Conventional-specification Products (μPD78F05xx, 78F05xxD)



<2> Expanded-specification Products (μPD78F05xxA, 78F05xxDA)



(2) Non-port functions

Port		78K0/KB2	78K0/KC2			78K0/KD2	78K0/KE2	78K0/KF2
		30/36 Pins	38 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
Power supply, ground		V_{DD}, EV_{DD}[Note 1], V_{SS}, EV_{SS}[Note 1], AV_{REF}, AV_{SS}	V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, V_{SS}, EV_{SS}, AV_{REF}, AV_{SS}	
Regulator		REGC						
Reset		$\overline{\text{RESET}}$						
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK, EXCLKS					
Writing to flash memory		FLMD0						
Interrupt		INTP0 to INTP5			INTP0 to INTP6		INTP0 to INTP7	
Key interrupt		–	KR0, KR1	KR0 to KR3		KR0 to KR7		
Timer	TM00	TI000, TI010, TO00						
	TM01	–					TI001[Note 2], TI011[Note 2], TO01[Note 2]	
	TM50	TI50, TO50						
	TM51	TI51, TO51						
	TMH0	TOH0						
	TMH1	TOH1						
Serial interface	UART0	RxD0, TxD0						
	UART6	RxD6, TxD6						
	IIC0	SCL0, SDA0	SCL0, SDA0, EXSCL0					
	CSI10	$\overline{\text{SCK10}}$, SI10, SO10						
	CSI11	–					$\overline{\text{SCK11}}$[Note 2], SI11[Note 2], SO11[Note 2], $\overline{\text{SSI11}}$[Note 2]	
	CSIA0	–						$\overline{\text{SCKA0}}$, SIA0, SOA0, BUSY0, STB0
A/D converter		ANI0 to ANI3	ANI0 to ANI5	ANI0 to ANI7				
Clock output		–			PCL			
Buzzer output		–					BUZ	
Low-voltage detector (LVI)		EXLVI						

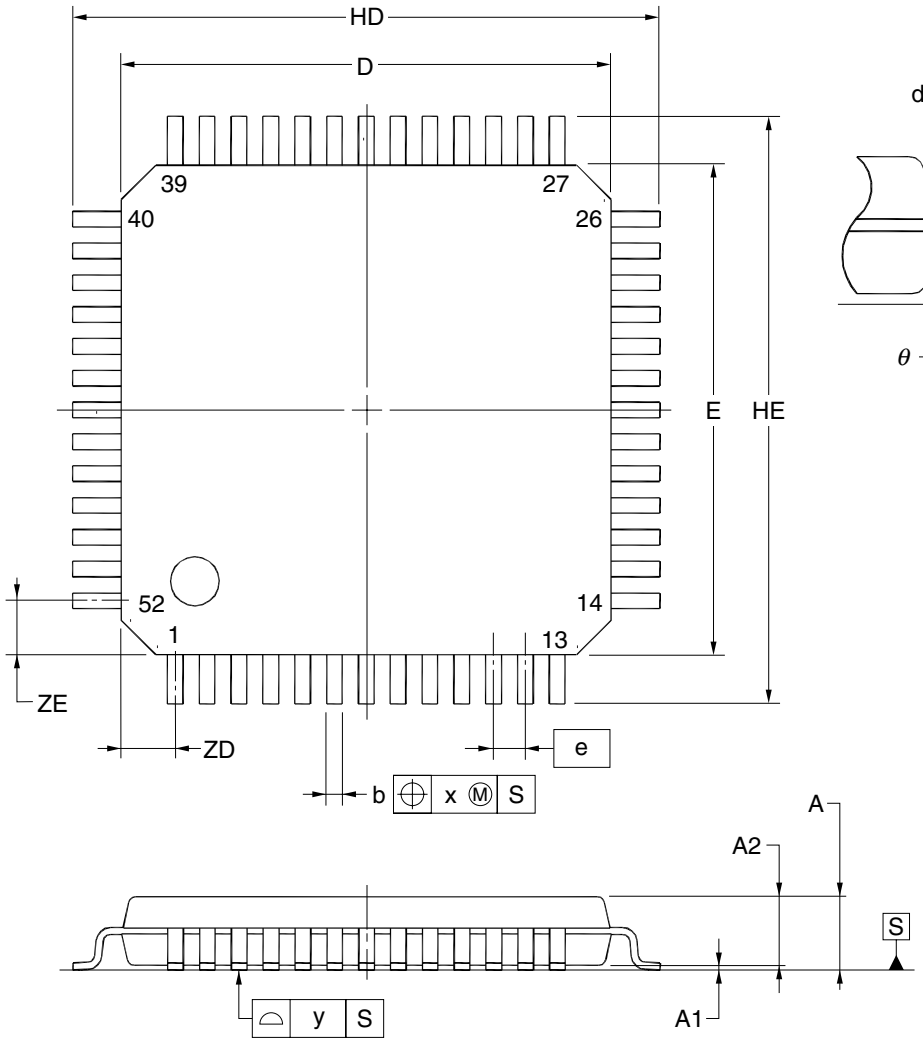
Notes 1. This is not mounted onto 30-pin products.

2. This is not mounted onto the 78K0/KE2 products whose flash memory is less than 32 KB.

34.3 78K0/KD2

- μPD78F0521GB-UET-A, 78F0522GB-UET-A, 78F0523GB-UET-A, 78F0524GB-UET-A, 78F0525GB-UET-A, 78F0526GB-UET-A, 78F0527GB-UET-A, 78F0527DGB-UET-A

52-PIN PLASTIC LQFP(10x10)



(UNIT:mm)

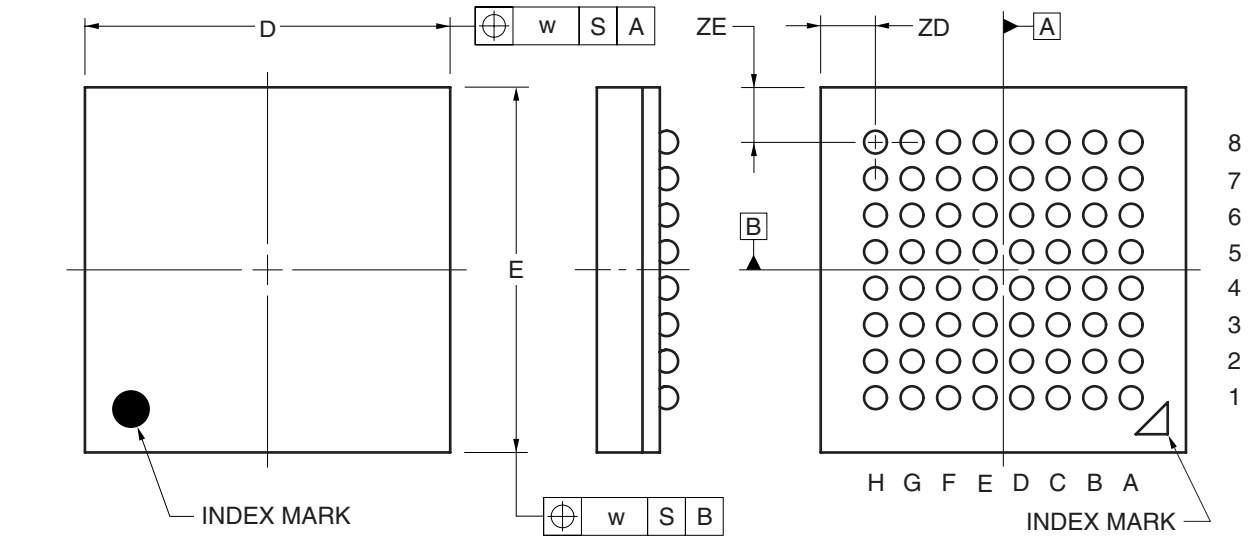
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.10
ZE	1.10

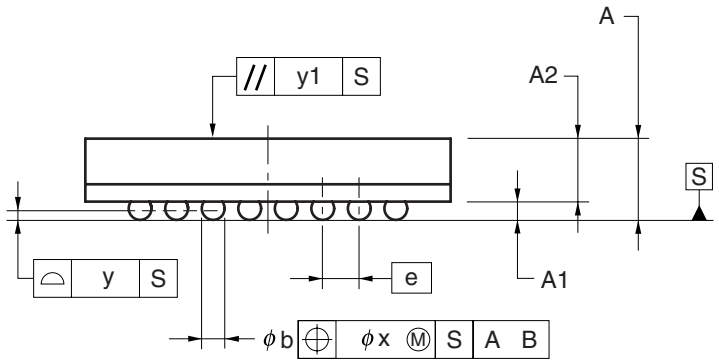
P52GB-65-UET-1

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

- μPD78F0531AF1-AA2-A, 78F0532AF1-AA2-A, 78F0533AF1-AA2-A, 78F0534AF1-AA2-A, 78F0535AF1-AA2-A, 78F0536AF1-AA2-A, 78F0537AF1-AA2-A, 78F0537DAF1-AA2-A

64-PIN PLASTIC FBGA (4x4)





(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

P64F1-40-AA2

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 6	Soft	Clock generator	OSCCTL: Clock operation mode select register	Set AMPH before setting the peripheral functions after a reset release. The value of AMPH can be changed only once after a reset release. When the high-speed system clock (X1 oscillation) is selected as the CPU clock, supply of the CPU clock is stopped for 4.06 to 16.12 μs after AMPH is set to 1. When the high-speed system clock (external clock input) is selected as the CPU clock, supply of the CPU clock is stopped for the duration of 160 external clocks after AMPH is set to 1.	pp. 230, 231 ☐
				If the STOP instruction is executed when AMPH = 1, supply of the CPU clock is stopped for 4.06 to 16.12 μs after the STOP mode is released when the internal high-speed oscillation clock is selected as the CPU clock, or for the duration of 160 external clocks when the high-speed system clock (external clock input) is selected as the CPU clock. When the high-speed system clock (X1 oscillation) is selected as the CPU clock, the oscillation stabilization time is counted after the STOP mode is released.	pp. 230, 231 ☐
				To change the value of EXCLK and OSCSEL, be sure to confirm that bit 7 (MSTOP) of the main OSC control register (MOC) is 1 (the X1 oscillator stops or the external clock from the EXCLK pin is disabled).	pp. 230, 231 ☐
				Be sure to clear bits 1 to 5 to 0. (78K0/KB2)	pp. 230, 231 ☐
			PCC: Processor clock control register	Be sure to clear bits 1 to 3 to 0. (78K0/KC2 to 78K0/KF2)	p. 232 ☐
				Be sure to clear bits 3 and 7 to “0”. (78K0/KC2 to 78K0/KF2)	p. 233 ☐
				The peripheral hardware clock (f_{PRS}) is not divided when the division ratio of the PCC is set.	pp. 232, 233 ☐
				Confirm that bit 5 (CLS) of the processor clock control register (PCC) is 0 (CPU is operating with main system clock) when changing the current values of XTSTART, EXCLKS, and OSCSELS.	p. 234 ☐
			RCM: Internal oscillation mode register	When setting RSTOP to 1, be sure to confirm that the CPU operates with a clock other than the internal high-speed oscillation clock. Specifically, set under either of the following conditions. <1> 78K0/KB2 • When MCS = 1 (when CPU operates with the high-speed system clock) <2> 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2 • When MCS = 1 (when CPU operates with the high-speed system clock) • When CLS = 1 (when CPU operates with the subsystem clock) In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock before setting RSTOP to 1.	p. 235 ☐
			MOC: Main OSC control register	When setting MSTOP to 1, be sure to confirm that the CPU operates with a clock other than the high-speed system clock. Specifically, set under either of the following conditions. <1> 78K0/KB2 • When MCS = 0 (when CPU operates with the internal high-speed oscillation clock) <2> 78K0/KC2, 78K0/KD2, 78K0/KE2, and 78K0/KF2 • When MCS = 0 (when CPU operates with the internal high-speed oscillation clock) • When CLS = 1 (when CPU operates with the subsystem clock) In addition, stop peripheral hardware that is operating on the high-speed system clock before setting MSTOP to 1.	p. 236 ☐
				Do not clear MSTOP to 0 while bit 6 (OSCSEL) of the clock operation mode select register (OSCCTL) is 0 (I/O port mode).	p. 236 ☐
				The peripheral hardware cannot operate when the peripheral hardware clock is stopped. To resume the operation of the peripheral hardware after the peripheral hardware clock has been stopped, initialize the peripheral hardware.	p. 236 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 35	Hard	Recommended soldering conditions	μPD78F05xxD	The μPD78F05xxD has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.	pp. 912, 913 ☐
			–	Do not use different soldering methods together (except for partial heating).	pp. 914, 916 ☐
			μPD78F05xxDA	The μPD78F05xxDA has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.	pp. 915, 916
Chapter 36	Soft	Wait	–	When the peripheral hardware clock (f_{PRS}) is stopped, do not access the registers listed above using an access method in which a wait request is issued.	p. 918 ☐