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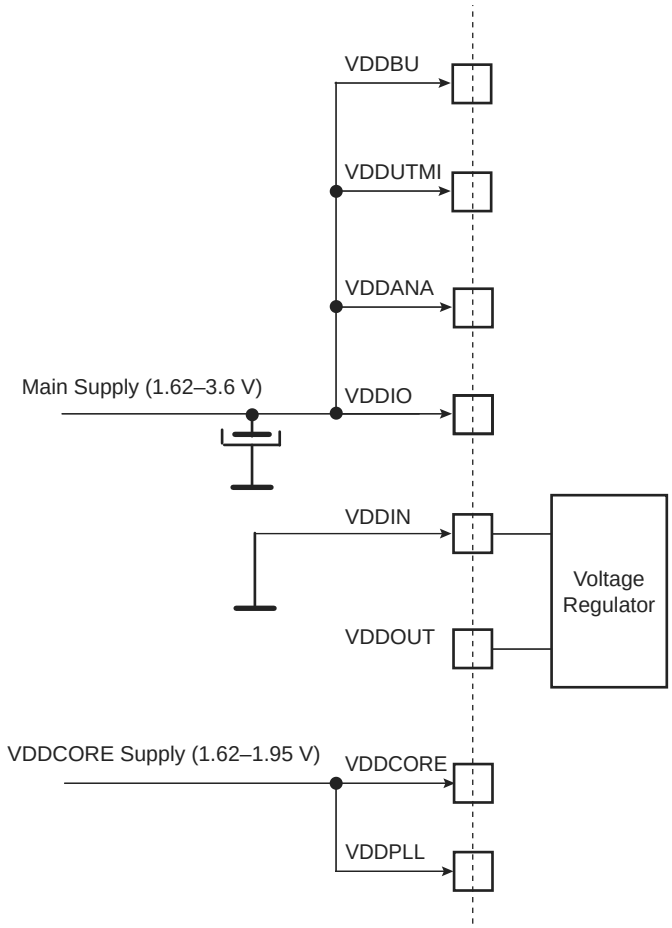
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	57
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 4x10b, 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atsam3u1ca-au

Figure 5-3. Core Externally Supplied



Note: Restrictions:
With Main Supply < 2.0 V, USB and ADC are not usable.
With Main Supply ≥ 2.4V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

12.19.5 Interrupt Clear-pending Registers

The ICPR0 register removes the pending state from interrupts, and show which interrupts are pending. See:

- the register summary in Table 12-27 on page 149 for the register attributes
- Table 12-28 on page 150 for which interrupts are controlled by each register.

The bit assignments are:

31	30	29	28	27	26	25	24
CLRPEND							

23	22	21	20	19	18	17	16
CLRPEND							

15	14	13	12	11	10	9	8
CLRPEND							

7	6	5	4	3	2	1	0
CLRPEND							

- **CLRPEND**

Interrupt clear-pending bits.

Write:

0 = no effect.

1 = removes pending state an interrupt.

Read:

0 = interrupt is not pending.

1 = interrupt is pending.

Writing 1 to an ICPR bit does not affect the active state of the corresponding interrupt.

12.22.4 MPU Region Base Address Register

The RBAR defines the base address of the MPU region selected by the RNR, and can update the value of the RNR. See the register summary in Table 12-35 on page 195 for its attributes.

Write RBAR with the VALID bit set to 1 to change the current region number and update the RNR. The bit assignments are:

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	N
ADDR							

N-1	6	5	4	3	2	1	0
Reserved			VALID	REGION			

- **ADDR**

Region base address field. The value of N depends on the region size. For more information see “The ADDR field”.

- **VALID**

MPU Region Number valid bit:

Write:

0 = RNR not changed, and the processor:

updates the base address for the region specified in the RNR

ignores the value of the REGION field

1 = the processor:

updates the value of the RNR to the value of the REGION field

updates the base address for the region specified in the REGION field.

Always reads as zero.

- **REGION**

MPU region field:

For the behavior on writes, see the description of the VALID field.

On reads, returns the current region number, as specified by the RNR.

12.22.4.1 The ADDR field

The ADDR field is bits[31:N] of the RBAR. The region size, as specified by the SIZE field in the RASR, defines the value of N:

$$N = Log_2(\text{Region size in bytes}),$$

If the region size is configured to 4GB, in the RASR, there is no valid ADDR field. In this case, the region occupies the complete memory map, and the base address is 0x00000000.

The base address is aligned to the size of the region. For example, a 64KB region must be aligned on a multiple of 64KB, for example, at 0x00010000 or 0x00020000.

18.5 Supply Controller (SUPC) User Interface

The User Interface of the Supply Controller is part of the System Controller User Interface.

18.5.1 System Controller (SYSC) User Interface

Table 18-1. System Controller Registers

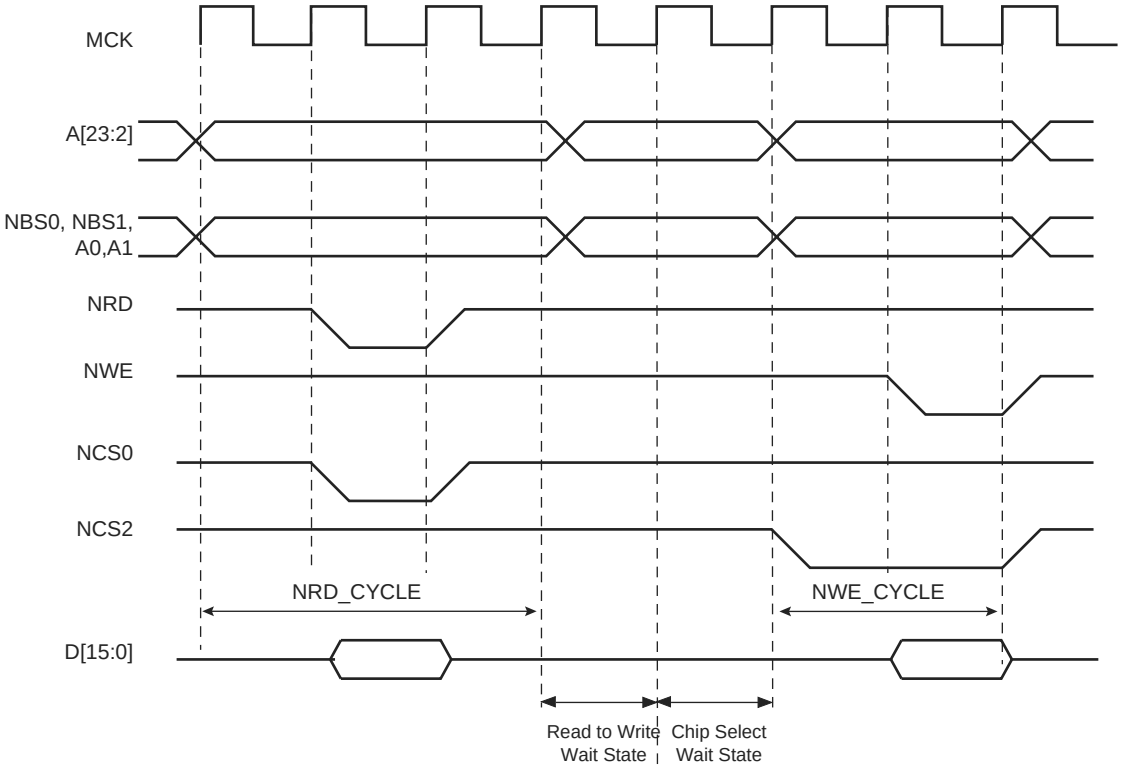
Offset	System Controller Peripheral	Name
0x00-0x0c	Reset Controller	RSTC
0x10-0x2C	Supply Controller	SUPC
0x30-0x3C	Real Time Timer	RTT
0x50-0x5C	Watchdog Tiler	WDT
0x60-0x7C	Real Time Clock	RTC
0x90-0xDC	General Purpose Backup Register	GPBR

18.5.2 Supply Controller (SUPC) User Interface

Table 18-2. Register Mapping

Offset	Register	Name	Access	Reset
0x00	Supply Controller Control Register	SUPC_CR	Write-only	N/A
0x04	Supply Controller Supply Monitor Mode Register	SUPC_SMMR	Read-write	0x0000_0000
0x08	Supply Controller Mode Register	SUPC_MR	Read-write	0x0000_5A00
0x0C	Supply Controller Wake Up Mode Register	SUPC_WUMR	Read-write	0x0000_0000
0x10	Supply Controller Wake Up Inputs Register	SUPC_WUIR	Read-write	0x0000_0000
0x14	Supply Controller Status Register	SUPC_SR	Read-only	0x0000_0800
0x18	Reserved			

Figure 24-13. Chip Select Wait State between a Read Access on NCS0 and a Write Access on NCS2



25.5.7 Transmit Next Pointer Register

Name: PERIPH_TNPR

Access: Read-write

31	30	29	28	27	26	25	24
TXNPTR							
23	22	21	20	19	18	17	16
TXNPTR							
15	14	13	12	11	10	9	8
TXNPTR							
7	6	5	4	3	2	1	0
TXNPTR							

- **TXNPTR: Transmit Next Pointer**

TXNPTR contains next transmit buffer address.

When a half duplex peripheral is connected to the PDC, RXNPTR = TXNPTR.

27.13 Register Write Protection

To prevent any single software error from corrupting PMC behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the PMC Write Protection Mode Register (PMC_WPMR).

If a write access to a write-protected register is detected, the WPVS bit in the PMC Write Protection Status Register (PMC_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS bit is automatically cleared after reading the PMC_WPSR.

The following registers can be write-protected:

- “PMC System Clock Enable Register”
- “PMC System Clock Disable Register”
- “PMC Peripheral Clock Enable Register”
- “PMC Peripheral Clock Disable Register”
- “PMC UTMI Clock Configuration Register”
- “PMC Clock Generator Main Oscillator Register”
- “PMC Clock Generator PLLA Register”
- “PMC Programmable Clock Register”
- “PMC Fast Startup Mode Register”
- “PMC Fast Startup Polarity Register”

29.7.8 PIO Controller Input Filter Disable Register

Name: PIO_IFDR

Address: 0x400E0C24 (PIOA), 0x400E0E24 (PIOB), 0x400E1024 (PIOC)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in “PIO Write Protect Mode Register”.

- **P0-P31: Input Filter Disable**

0 = No effect.

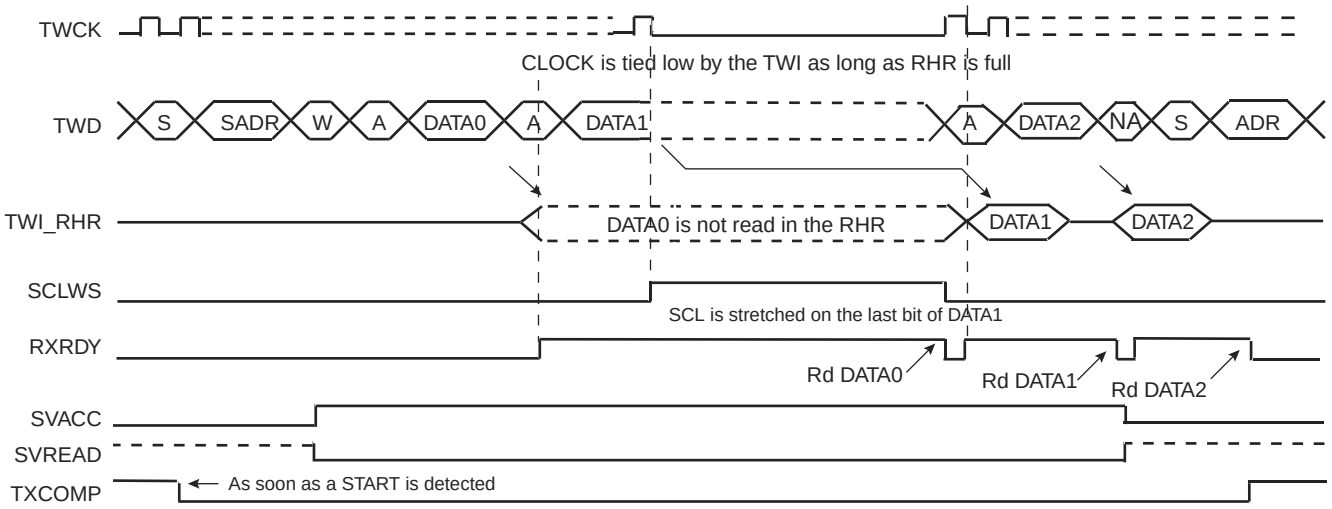
1 = Disables the input glitch filter on the I/O line.

Clock Synchronization in Write Mode

The clock is tied low if the shift register and the TWI_RHR is full. If a STOP or REPEATED_START condition was not detected, it is tied low until TWI_RHR is read.

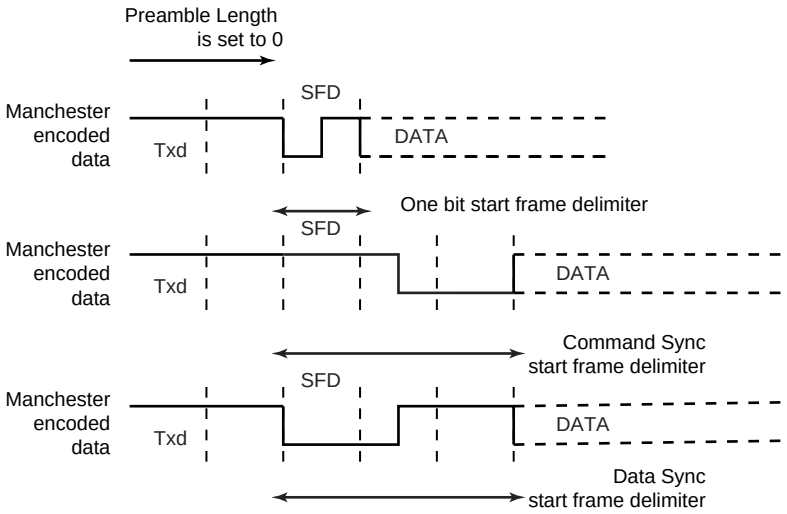
Figure 32-29 on page 650 describes the clock synchronization in Read mode.

Figure 32-29. Clock Synchronization in Write Mode



Notes:
1. At the end of the read sequence, TXCOMP is set after a STOP or after a REPEATED_START + an address different from SADR.
2. SCLWS is automatically set when the clock synchronization mechanism is started and automatically reset when the mechanism is finished.

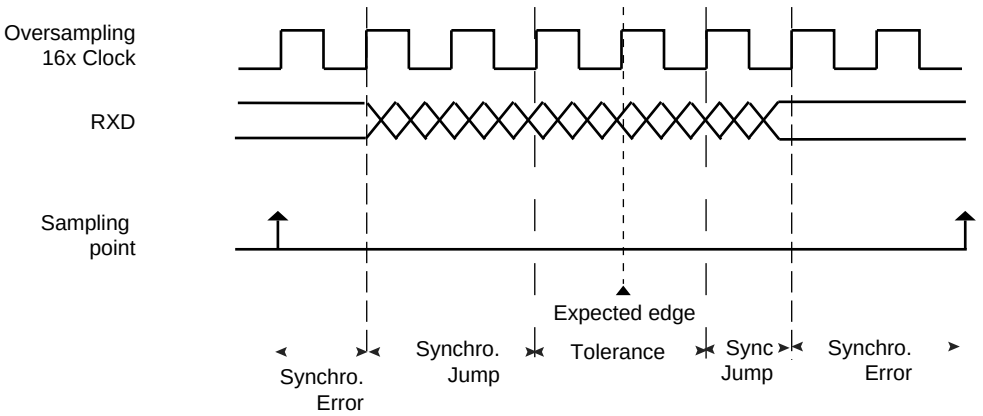
Figure 34-10. Start Frame Delimiter



Drift Compensation

Drift compensation is available only in 16X oversampling mode. An hardware recovery system allows a larger clock drift. To enable the hardware system, the bit in the USART_MAN register must be set. If the RXD edge is one 16X clock cycle from the expected edge, this is considered as normal jitter and no corrective actions is taken. If the RXD event is between 4 and 2 clock cycles before the expected edge, then the current period is shortened by one clock cycle. If the RXD event is between 2 and 3 clock cycles after the expected edge, then the current period is lengthened by one clock cycle. These intervals are considered to be drift and so corrective actions are automatically taken.

Figure 34-11. Bit Resynchronization



34.7.3.3 Asynchronous Receiver

If the USART is programmed in asynchronous operating mode (SYNC = 0), the receiver oversamples the RXD input line. The oversampling is either 16 or 8 times the Baud Rate clock, depending on the OVER bit in the Mode Register (US_MR).

The receiver samples the RXD line. If the line is sampled during one half of a bit time to 0, a start bit is detected and data, parity and stop bits are successively sampled on the bit rate clock.

If the oversampling is 16, (OVER to 0), a start is detected at the eighth sample to 0. Then, data bits, parity bit and stop bit are sampled on each 16 sampling clock cycle. If the oversampling is 8 (OVER to 1), a start bit is detected at the fourth sample to 0. Then, data bits, parity bit and stop bit are sampled on each 8 sampling clock cycle.

34.8.8 USART Transmit Holding Register

Name: US_THR

Address: 0x4009001C (0), 0x4009401C (1), 0x4009801C (2), 0x4009C01C (3)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TXSYNH	–	–	–	–	–	–	TXCHR

7	6	5	4	3	2	1	0
TXCHR							

- **TXCHR: Character to be Transmitted**

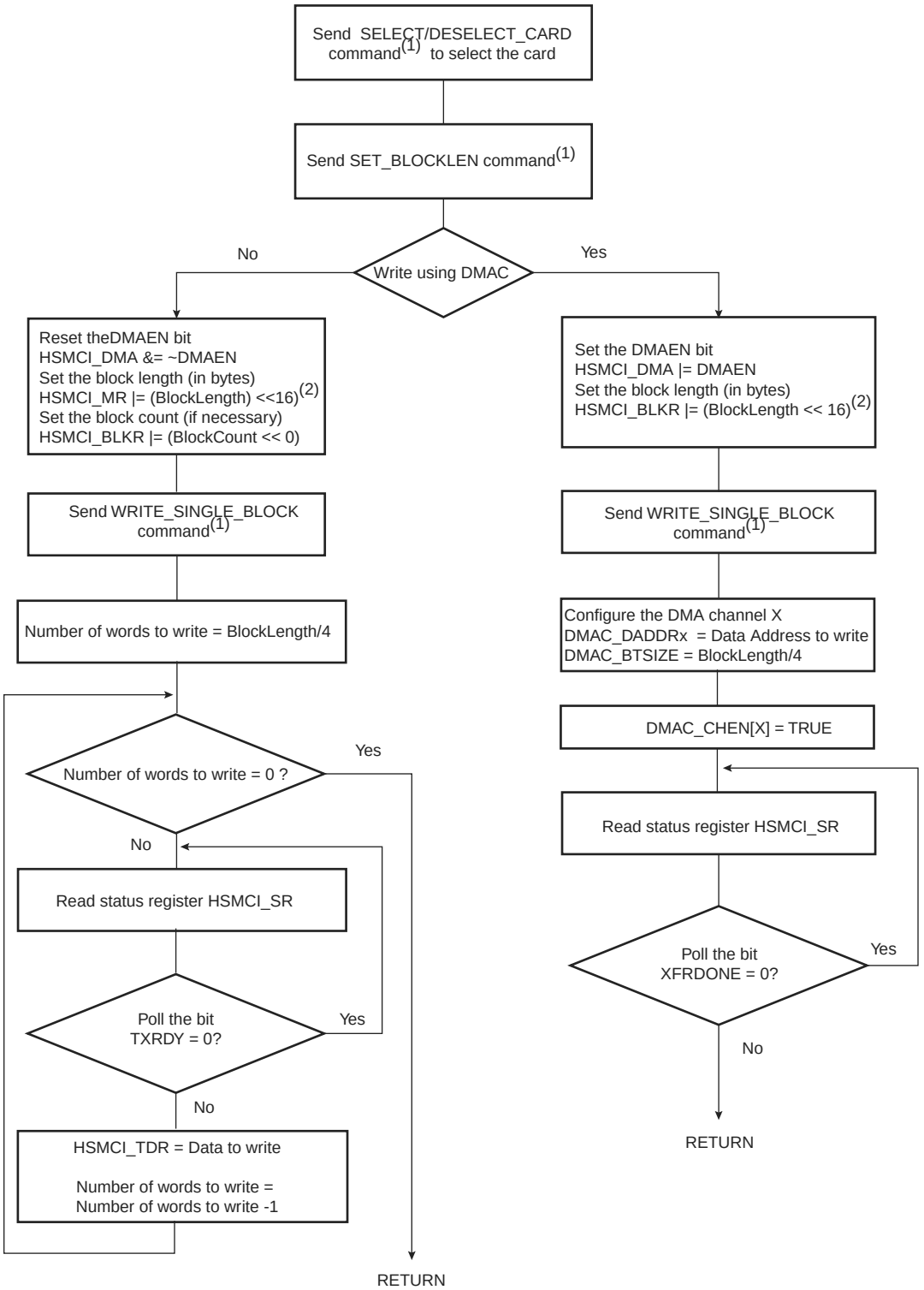
Next character to be transmitted after the current character if TXRDY is not set.

- **TXSYNH: Sync Field to be transmitted**

0: The next character sent is encoded as a data. Start Frame Delimiter is DATA SYNC.

1: The next character sent is encoded as a command. Start Frame Delimiter is COMMAND SYNC.

Figure 36-9. Write Functional Flow Diagram



Note: 1. It is assumed that this command has been correctly sent (see Figure 36-7).
2. This field is also accessible in the HSMCI Block Register (HSMCI_BLKR).

The following flowchart (Figure 36-10) shows how to manage read multiple block and write multiple block transfers with the DMA Controller. Polling or interrupt method can be used to wait for the end of write according to the contents of the Interrupt Mask Register (HSMCI_IMR).

36.14.8 HSMCI Completion Signal Timeout Register

Name: HSMCI_CSTOR

Address: 0x4000001C

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	CSTOMUL			CSTOCYC			

This register can only be written if the WPEN bit is cleared in “HSMCI Write Protect Mode Register” on page 860.

- **CSTOCYC: Completion Signal Timeout Cycle Number**

These fields determine the maximum number of Master Clock cycles that the HSMCI waits between two data block transfers. Its value is calculated by (CSTOCYC x Multiplier).

- **CSTOMUL: Completion Signal Timeout Multiplier**

These fields determine the maximum number of Master Clock cycles that the HSMCI waits between two data block transfers. Its value is calculated by (CSTOCYC x Multiplier).

These fields determine the maximum number of Master Clock cycles that the HSMCI waits between the end of the data transfer and the assertion of the completion signal. The data transfer comprises data phase and the optional busy phase. If a non-DATA ATA command is issued, the HSMCI starts waiting immediately after the end of the response until the completion signal.

Multiplier is defined by CSTOMUL as shown in the following table:

Value	Name	Description
0	1	CSTOCYC x 1
1	16	CSTOCYC x 16
2	128	CSTOCYC x 128
3	256	CSTOCYC x 256
4	1024	CSTOCYC x 1024
5	4096	CSTOCYC x 4096
6	65536	CSTOCYC x 65536
7	1048576	CSTOCYC x 1048576

If the data time-out set by CSTOCYC and CSTOMUL has been exceeded, the Completion Signal Time-out Error flag (CSTOE) in the HSMCI Status Register (HSMCI_SR) rises.

37.2 Embedded Characteristics

- 4 Channels
- Common Clock Generator Providing Thirteen Different Clocks
  - A Modulo n Counter Providing Eleven Clocks
  - Two Independent Linear Dividers Working on Modulo n Counter Outputs
- Independent Channels
  - Independent 16-bit Counter for Each Channel
  - Independent Complementary Outputs with 12-bit Dead-Time Generator (Also Called Dead-Band or Non-Overlapping Time) for Each Channel
  - Independent Enable Disable Command for Each Channel
  - Independent Clock Selection for Each Channel
  - Independent Period, Duty-Cycle and Dead-Time for Each Channel
  - Independent Double Buffering of Period, Duty-Cycle and Dead-Times for Each Channel
  - Independent Programmable Selection of The Output Waveform Polarity for Each Channel
  - Independent Programmable Center or Left Aligned Output Waveform for Each Channel
  - Independent Output Override for Each Channel
- Synchronous Channel Mode
  - Synchronous Channels Share the Same Counter
  - Mode to Update the Synchronous Channels Registers after a Programmable Number of Periods
  - Synchronous Channels Supports Connection of one Peripheral DMA Controller Channel (PDC) Which Offers Buffer Transfer Without Processor Intervention To Update Duty-Cycle Registers
- 2 Independent Events Lines Intended to Synchronize ADC Conversions
- 8 Comparison Units Intended to Generate Interrupts, Pulses on Event Lines and PDC Transfer Requests
- 4 Programmable Fault Inputs Providing an Asynchronous Protection of PWM Outputs
  - User Driven through PIO inputs
  - PMC Driven when Crystal Oscillator Clock Fails
  - ADC Controller Driven through Configurable Comparison Function
- Write-Protect Registers

An endpoint handles all transactions related to the type of transfer for which it has been configured.

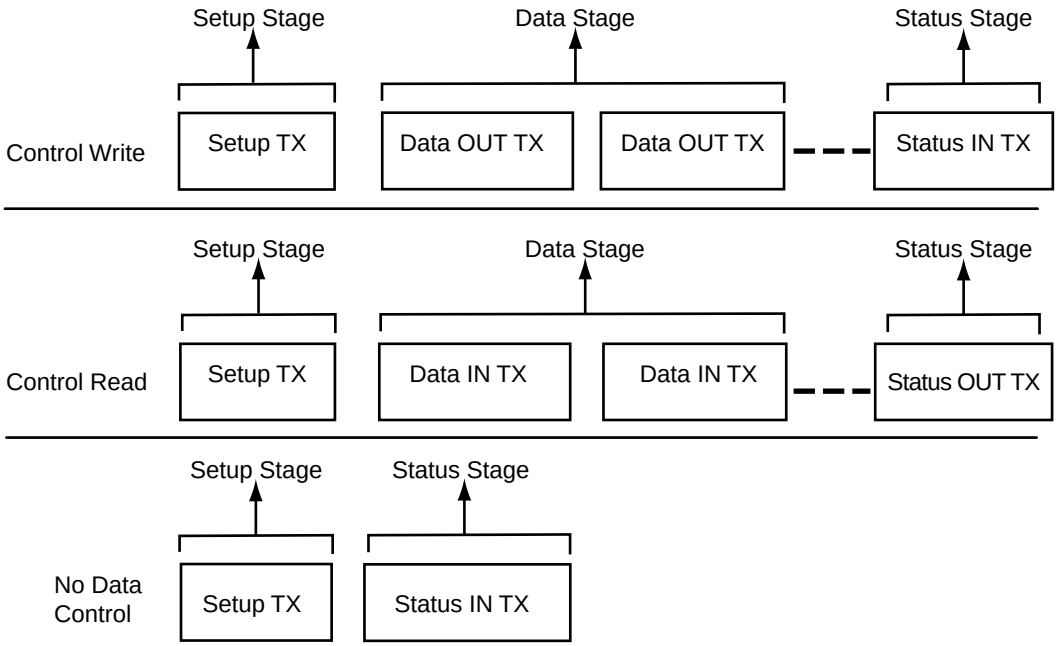
38.6.4 USB V2.0 High Speed BUS Transactions

Each transfer results in one or more transactions over the USB bus.

There are five kinds of transactions flowing across the bus in packets:

1. Setup Transaction
2. Data IN Transaction
3. Data OUT Transaction
4. Status IN Transaction
5. Status OUT Transaction

Figure 38-3. Control Read and Write Sequences



A status IN or OUT transaction is identical to a data IN or OUT transaction.

38.6.5 Endpoint Configuration

The endpoint 0 is always a control endpoint, it must be programmed and active in order to be enabled when the End Of Reset interrupt occurs.

To configure the endpoints:

- Fill the configuration register (UDPHS_EPTCFG) with the endpoint size, direction (IN or OUT), type (CTRL, Bulk, IT, ISO) and the number of banks.
- Fill the number of transactions (NB_TRANS) for isochronous endpoints.

Note: For control endpoints the direction has no effect.

- Verify that the EPT_MAPD flag is set. This flag is set if the endpoint size and the number of banks are correct compared to the FIFO maximum capacity and the maximum number of allowed banks.
- Configure control flags of the endpoint and enable it in UDPHS_EPTCTLENBx according to “UDPHS Endpoint Control Register” on page 987.

Control endpoints can generate interrupts and use only 1 bank.

- **ERR_OVFLW: Overflow Error Interrupt Disable**

0 = no effect.

1 = disable Overflow Error Interrupt.

- **RX_BK_RDY: Received OUT Data Interrupt Disable**

0 = no effect.

1 = disable Received OUT Data Interrupt.

- **TX_COMPLT: Transmitted IN Data Complete Interrupt Disable**

0 = no effect.

1 = disable Transmitted IN Data Complete Interrupt.

- **TX_PK_RDY/ERR_TRANS: TX Packet Ready/Transaction Error Interrupt Disable**

0 = no effect.

1 = disable TX Packet Ready/Transaction Error Interrupt.

- **RX_SETUP/ERR_FL_ISO: Received SETUP/Error Flow Interrupt Disable**

0 = no effect.

1 = disable RX_SETUP/Error Flow ISO Interrupt.

- **STALL_SNT/ERR_CRISO/ERR_NBTRA: Stall Sent/ISO CRC Error/Number of Transaction Error Interrupt Disable**

0 = no effect.

1 = disable Stall Sent/Error CRC ISO/Error Number of Transaction Interrupt.

- **NAK_IN/ERR_FLUSH: NAKIN/bank flush error Interrupt Disable**

0 = no effect.

1 = disable NAKIN/ Bank Flush Error Interrupt.

- **NAK_OUT: NAKOUT Interrupt Disable**

0 = no effect.

1 = disable NAKOUT Interrupt.

- **BUSY_BANK: Busy Bank Interrupt Disable**

0 = no effect.

1 = disable Busy Bank Interrupt.

- **SHRT_PCKT: Short Packet Interrupt Disable**

For OUT endpoints:

0 = no effect.

1 = disable Short Packet Interrupt.

For IN endpoints:

Never automatically add a zero length packet at end of DMA transfer.

40.6.1 ADC12B Control Register

Name: ADC12B_CR

Address: 0x400A8000

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	START	SWRST

- **SWRST: Software Reset**

0 = No effect.

1 = Resets the ADC12B simulating a hardware reset.

- **START: Start Conversion**

0 = No effect.

1 = Begins analog-to-digital conversion.

42.3.1.2 Configuration B

- All power supplies OFF, except VDDBU and VDDIO
- Supply Monitor on VDDUTMI is disabled
- RTC ON, RTT ON
- 32 kHz Crystal Oscillator used
- FWUP pin = VDDBU
- Wake-up pins WKUP0–15 = VDDIO
- Current measurement on AMP1 and on AMP2

Figure 42-5. Measurement Setup

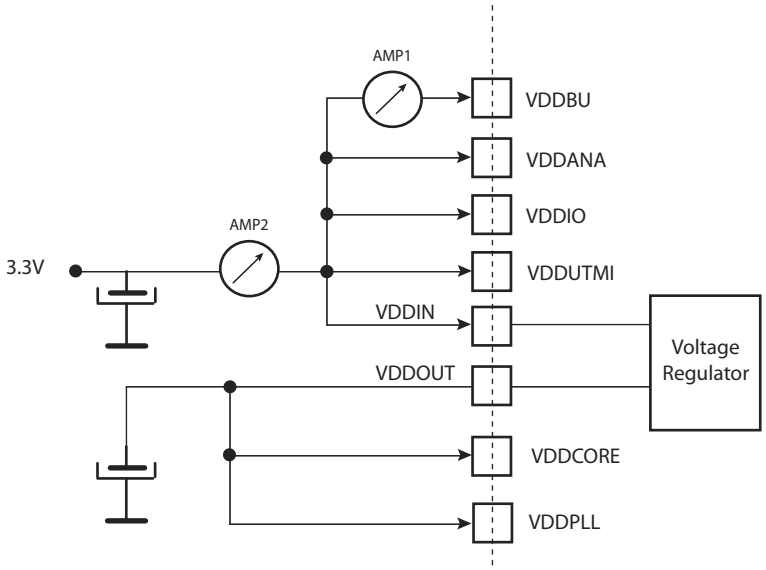


Table 42-9. Power Consumption for Backup Mode Configuration B

Conditions	VDDBU Consumption (AMP1)	Total Consumption (AMP2)	Unit
VDDBU = 3.3V @ 25°C	3.0	3.06	µA
VDDBU = 3.0V @ 25°C	2.7	2.75	
VDDBU = 2.5V @ 25°C	2.2	2.25	
VDDBU = 1.8V @ 25°C	1.6	1.64	

Table 47-1. SAM3U Datasheet Rev. 6430G Revision History (Continued)

Doc. Date	Changes
31-Mar-15	Section 42. ”Electrical Characteristics” (cont’d) Updated Figure 42-11 ”XIN32 Clock Timing” Table 42-21, “3 to 20 MHz Crystal Oscillator Characteristics”: updated values for parameter “External capacitor on XIN and XOUT”; added parameter “Allowed Crystal Capacitance Load”; deleted all footnotes Updated Figure 42-13 ”XIN Clock Timing” Updated Section 42.4.9 ”Crystal Oscillators Design Consideration Information” Table 42-25, “PLLA Characteristics”: updated min/max values for parameters “Input Frequency” and “Output Frequency” Table 42-25, “PLLA Characteristics”: added max value for Current Consumption (Standby mode) Table 42-28, “Static Power Consumption”: corrected VDDUTMII to VDDUTMI Table 42-29, “Dynamic Power Consumption”: corrected VDDUTMII to VDDUTMI Deleted section 43.6.5 “USB High Speed Design Guidelines” Table 42-30, “Analog Power Supply Characteristics”: changed VDDIN to VDDANA Table 42-32, “External Voltage Reference Input”: changed VDDIN to VDDANA Updated Section 42.7.1 ”Static Performance Characteristics” Table 42-33, “INL, DNL, 12-bit mode, VDDANA Supply Voltage Conditions”: changed VDDIN to VDDANA Table 42-34, “Gain Error, Offset Error, 12-bit Mode, VDDANA Supply Voltage Conditions(1)”: changed VDDIN to VDDANA Inserted heading Section 42.7.2 ”Dynamic Performance Characteristics” and updated content Replaced section “Track and Hold Time versus Source Output Impedance” with Section 42.7.2.1 ”Sample and Hold Time versus Source Output Impedance” Table 42-39, “Analog Inputs”: in footnote, changed VDDIN to VDDANA Restored Section 42.8 ”10-bit Successive Approximation Register (SAR) ADC Characteristics” (content was inadvertently removed in version 6430F of this datasheet) Section 42.9.3.1 ”Maximum SPI Frequency”: updated content under ”Master Write Mode” and ”Master Read Mode” Table 42-49, “SSC Timings”: updated parameters SSC_4 and SSC_7; deleted footnote “Timings SSC4 and SSC7 depend on...” Section 42.9 ”AC Characteristics”: removed Figure 43-27. “USART SPI Master Mode”, Figure 43-28. “USART SPI Slave mode (Mode 1 or 2)”, Figure 43-29. “USART SPI Slave mode (Mode 0 or 3)”, and Table 43-49. “USART SPI Timings” Table 42-54, “Two-wire Serial Bus Requirements”: in bottom row, replaced duplicated parameter “Hold Time (repeated) START Condition” with new parameter “Bus free time between a STOP and START condition” Section 42.9.8 ”Embedded Flash Characteristics”: in first paragraph, corrected “field FWS of the MC_FMR register” to “field FWS of the EEFC_FMR”; updated text and replaced two wait state tables with single Table 42-55, “Embedded Flash Wait State - VDDCORE 1.62V/1.80V”
	Section 43. ”Mechanical Characteristics” Figure 43-1 ”100-lead LQFP Package Drawing”: added notes 1 and 2 Section 43.2 ”100-ball TFBGA Package”: at end of section, added sentence “This package respects the recommendations of the NEMI User Group.” Figure 43-2 ”100-ball TFBGA Package Drawing”: corrected ‘A’ maximum dimension in inches from 0.0575 to 0.0433 Updated Table 43-4, “100-ball TFBGA Soldering Information (Substrate Level)” Updated Table 43-5, “100-ball TFBGA Device Maximum Weight” Updated Table 43-7, “100-ball TFBGA Package Reference” Section 43.3 ”144-lead LQFP Package”: at end of section, added sentence “This package respects the recommendations of the NEMI User Group.” Updated Table 43-8, “144-lead LQFP Device Maximum Weight”