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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	96
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/atmel/atsam3u1ea-au">https://www.e-xfl.com/product-detail/atmel/atsam3u1ea-au</a>

### 12.11.3.5 Examples

```
STR    R0, [R5, R1]      ; Store value of R0 into an address equal to
                          ; sum of R5 and R1
LDRSB  R0, [R5, R1, LSL #1] ; Read byte value from an address equal to
                          ; sum of R5 and two times R1, sign extended it
                          ; to a word value and put it in R0
STR    R0, [R1, R2, LSL #2] ; Stores R0 to an address equal to sum of R1
                          ; and four times R2
```

## 15.3 Functional Description

### 15.3.1 Reset Controller Overview

The Reset Controller is made up of an NRST Manager and a Reset State Manager. It runs at Slow Clock and generates the following reset signals:

- `proc_nreset`: Processor reset line. It also resets the Watchdog Timer.
- `periph_nreset`: Affects the whole set of embedded peripherals.
- `nrst_out`: Drives the NRST pin.

These reset signals are asserted by the Reset Controller, either on external events or on software action. The Reset State Manager controls the generation of reset signals and provides a signal to the NRST Manager when an assertion of the NRST pin is required.

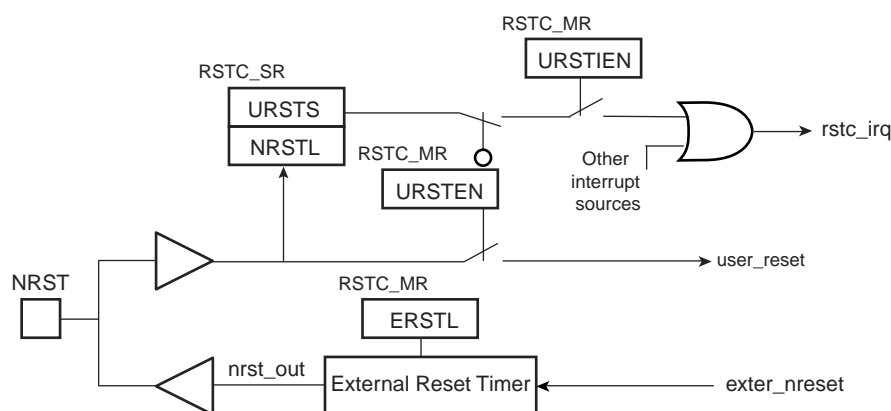
The NRST Manager shapes the NRST assertion during a programmable time, thus controlling external device resets.

The Reset Controller Mode Register (`RSTC_MR`), allowing the configuration of the Reset Controller, is powered with `VDDDBU`, so that its configuration is saved as long as `VDDDBU` is on.

### 15.3.2 NRST Manager

The NRST Manager samples the NRST input pin and drives this pin low when required by the Reset State Manager. Figure 15-2 shows the block diagram of the NRST Manager.

**Figure 15-2. NRST Manager**



#### 15.3.2.1 NRST Signal or Interrupt

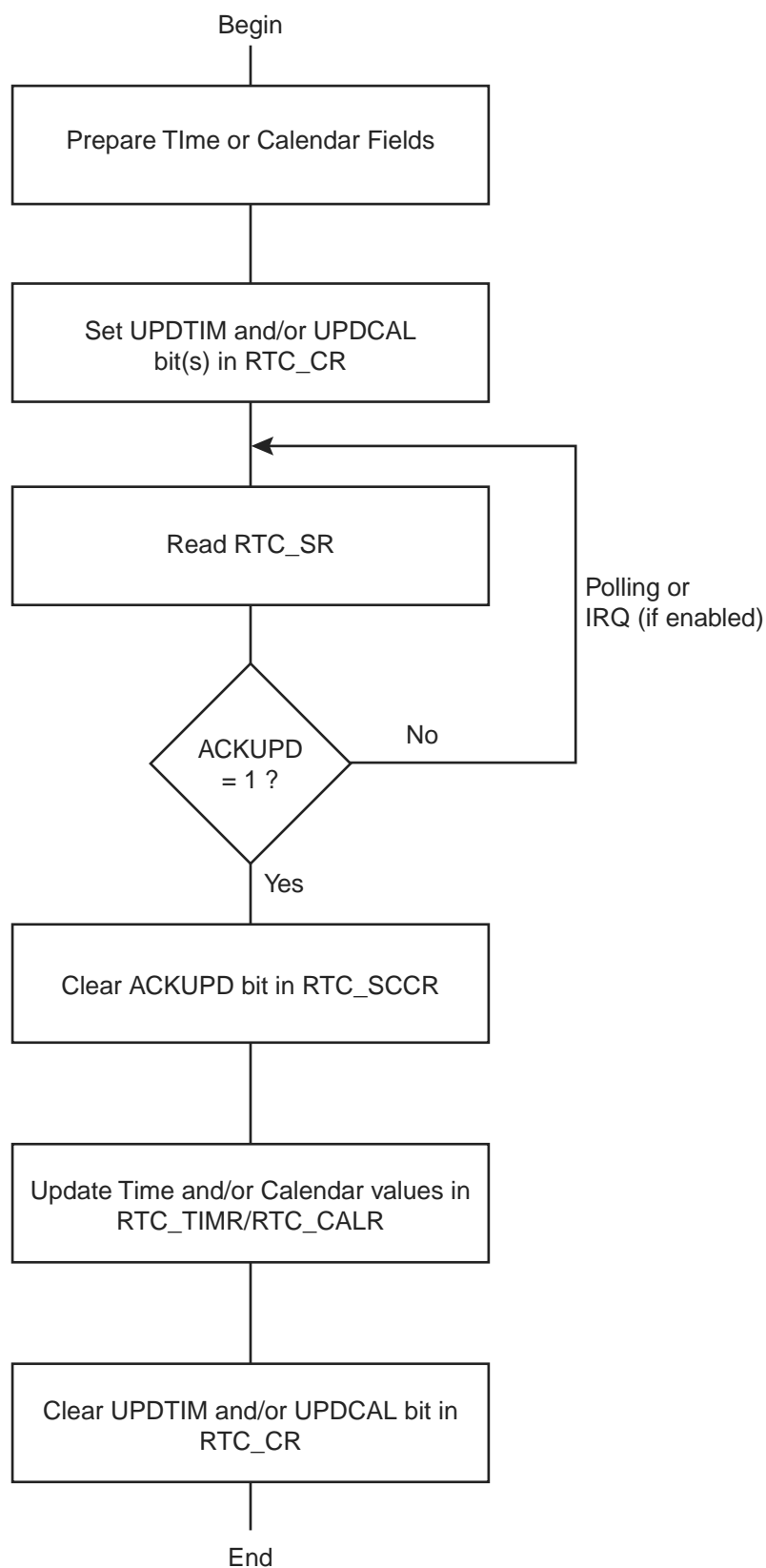
The NRST Manager samples the NRST pin at Slow Clock speed. When the line is detected low, a User Reset is reported to the Reset State Manager.

However, the NRST Manager can be programmed to not trigger a reset when an assertion of NRST occurs. Writing the bit `URSTEN` at 0 in `RSTC_MR` disables the User Reset trigger.

The level of the pin `NRST` can be read at any time in the bit `NRSTL` (NRST level) in `RSTC_SR`. As soon as the pin `NRST` is asserted, the bit `URSTS` in `RSTC_SR` is set. This bit clears only when `RSTC_SR` is read.

The Reset Controller can also be programmed to generate an interrupt instead of generating a reset. To do so, the bit `URSTIEN` in `RSTC_MR` must be written at 1.

Figure 17-2. Update Sequence



### 17.5.6 RTC Calendar Alarm Register

**Name:** RTC\_CALALR

**Address:** 0x400E1274

**Access:** Read-write

31	30	29	28	27	26	25	24
DATEEN	–	DATE					
23	22	21	20	19	18	17	16
MTHEN	–	–	MONTH				
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

This register can only be written if the WPEN bit is cleared in “RTC Write Protect Mode Register” on page 263.

- **MONTH: Month Alarm**

This field is the alarm field corresponding to the BCD-coded month counter.

- **MTHEN: Month Alarm Enable**

0 = The month-matching alarm is disabled.

1 = The month-matching alarm is enabled.

- **DATE: Date Alarm**

This field is the alarm field corresponding to the BCD-coded date counter.

- **DATEEN: Date Alarm Enable**

0 = The date-matching alarm is disabled.

1 = The date-matching alarm is enabled.

## 18.5.6 Supply Controller Wake Up Mode Register

**Name:** SUPC\_WUMR

**Address:** 0x400E121C

**Access:** Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	WKUPDBC			–	FWUPDBC		
7	6	5	4	3	2	1	0
–	–	–	–	RTCEN	RTTEN	SMEN	FWUPEN

- **FWUPEN: Force Wake Up Enable**

0 (NOT\_ENABLE) = the Force Wake Up pin has no wake up effect.

1 (ENABLE) = the Force Wake Up pin low forces the wake up of the core power supply.

- **SMEN: Supply Monitor Wake Up Enable**

0 (NOT\_ENABLE) = the supply monitor detection has no wake up effect.

1 (ENABLE) = the supply monitor detection forces the wake up of the core power supply.

- **RTTEN: Real Time Timer Wake Up Enable**

0 (NOT\_ENABLE) = the RTT alarm signal has no wake up effect.

1 (ENABLE) = the RTT alarm signal forces the wake up of the core power supply.

- **RTCEN: Real Time Clock Wake Up Enable**

0 (NOT\_ENABLE) = the RTC alarm signal has no wake up effect.

1 (ENABLE) = the RTC alarm signal forces the wake up of the core power supply.

- **FWUPDBC: Force Wake Up Debouncer Period**

Value	Name	Description
0	IMMEDIATE	Immediate, no debouncing, detected active at least on one Slow Clock edge.
1	3_SCLK	FWUP shall be low for at least 3 SLCK periods
2	32_SCLK	FWUP shall be low for at least 32 SLCK periods
3	512_SCLK	FWUP shall be low for at least 512 SLCK periods
4	4096_SCLK	FWUP shall be low for at least 4,096 SLCK periods
5	32768_SCLK	FWUP shall be low for at least 32,768 SLCK periods
6	Reserved	Reserved
7	Reserved	Reserved

## 23.5 Write Protect Registers

To prevent any single software error that may corrupt MATRIX behavior, the entire MATRIX address space from address offset 0x000 to 0x1FC can be write-protected by setting the WPEN bit in the MATRIX Write Protect Mode Register (MATRIX\_WPMR).

If a write access to anywhere in the MATRIX address space from address offset 0x000 to 0x1FC is detected, then the WPVS flag in the MATRIX Write Protect Status Register (MATRIX\_WPSR) is set and the field WPVSRC indicates in which register the write access has been attempted.

The WPVS flag is reset by writing the MATRIX Write Protect Mode Register (MATRIX\_WPMR) with the appropriate access key WPKEY.

The protected registers are:

“Bus Matrix Master Configuration Registers”

“Bus Matrix Slave Configuration Registers”

“Bus Matrix Priority Registers For Slaves”

“Bus Matrix Master Remap Control Register”

“Bus Matrix Master Remap Control Register”

#### **24.16.4.2 NFC SRAM Access Prioritization Algorithm**

When the NAND Flash Controller (NFC) is reading from or writing to the NFC SRAM, the internal memory is no longer accessible. If an NFC SRAM access occurs when the NFC performs a read or write operation then the access is discarded. The write operation is not performed. The read operation returns undefined data. If this situation is encountered, the status flag AWB located in the NFC status Register is raised and indicates that a shared resource access violation has occurred.

#### **24.16.5 NAND Flash Operations**

This section describes the software operations needed to issue commands to the NAND Flash device and perform data transfers using NFC.



## 24.18.22 SMC OCMS Register

**Name:** SMC\_OCMS

**Address:** 0x400E0110

**Access:** Read-write

**Reset:** 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	SRSE	SMSE

- **SMSE: Static Memory Controller Scrambling Enable**

0: Disable “Off Chip” Scrambling for SMC access.

1: Enable “Off Chip” Scrambling for SMC access. (If OCMS field is set to 1 in the relevant SMC\_TIMINGS register.)

- **SRSE: SRAM Scrambling Enable**

0: Disable SRAM Scrambling for SRAM access.

1: Enable SRAM Scrambling for SRAM access. (If OCMS field is set to 1 in the relevant SMC\_TIMINGS register.)

- **MOSCRCF: Main On-Chip RC Oscillator Frequency Selection**

At start-up, the Main On-Chip RC Oscillator frequency is 4 MHz.

0: The Fast RC Oscillator Frequency is at 4 MHz (default).

1: The Fast RC Oscillator Frequency is at 8 MHz.

2: The Fast RC Oscillator Frequency is at 12 MHz.

3: Reserved.

- **MOSCXTST: Main Crystal Oscillator Start-up Time**

Specifies the number of Slow Clock cycles multiplied by 8 for the Main Crystal Oscillator start-up time.

- **MOSCSEL: Main Oscillator Selection**

0: The Main On-Chip RC Oscillator is selected.

1: The Main Crystal Oscillator is selected.

- **CFDEN: Clock Failure Detector Enable**

0: The Clock Failure Detector is disabled.

1: The Clock Failure Detector is enabled.

## 29.7 Parallel Input/Output Controller (PIO) User Interface

Each I/O line controlled by the PIO Controller is associated with a bit in each of the PIO Controller User Interface registers. Each register is 32 bits wide. If a parallel I/O line is not defined, writing to the corresponding bits has no effect. Undefined bits read zero. If the I/O line is not multiplexed with any peripheral, the I/O line is controlled by the PIO Controller and PIO\_PSR returns 1 systematically.

**Table 29-2. Register Mapping**

Offset	Register	Name	Access	Reset
0x0000	PIO Enable Register	PIO_PER	Write-only	–
0x0004	PIO Disable Register	PIO_PDR	Write-only	–
0x0008	PIO Status Register	PIO_PSR	Read-only	(1)
0x000C	Reserved			
0x0010	Output Enable Register	PIO_OER	Write-only	–
0x0014	Output Disable Register	PIO_ODR	Write-only	–
0x0018	Output Status Register	PIO_OSR	Read-only	0x0000 0000
0x001C	Reserved			
0x0020	Glitch Input Filter Enable Register	PIO_IFER	Write-only	–
0x0024	Glitch Input Filter Disable Register	PIO_IFDR	Write-only	–
0x0028	Glitch Input Filter Status Register	PIO_IFSR	Read-only	0x0000 0000
0x002C	Reserved			
0x0030	Set Output Data Register	PIO_SODR	Write-only	–
0x0034	Clear Output Data Register	PIO_CODR	Write-only	
0x0038	Output Data Status Register	PIO_ODSR	Read-only or <sup>(2)</sup> Read-write	–
0x003C	Pin Data Status Register	PIO_PDSR	Read-only	(3)
0x0040	Interrupt Enable Register	PIO_IER	Write-only	–
0x0044	Interrupt Disable Register	PIO_IDR	Write-only	–
0x0048	Interrupt Mask Register	PIO_IMR	Read-only	0x00000000
0x004C	Interrupt Status Register <sup>(4)</sup>	PIO_ISR	Read-only	0x00000000
0x0050	Multi-driver Enable Register	PIO_MDER	Write-only	–
0x0054	Multi-driver Disable Register	PIO_MDDR	Write-only	–
0x0058	Multi-driver Status Register	PIO_MDSR	Read-only	0x00000000
0x005C	Reserved			
0x0060	Pull-up Disable Register	PIO_PUDR	Write-only	–
0x0064	Pull-up Enable Register	PIO_PUER	Write-only	–
0x0068	Pad Pull-up Status Register	PIO_PUSR	Read-only	0x00000000
0x006C	Reserved			

### 31.8.9 SPI Chip Select Register

**Name:** SPI\_CSRx[x=0..3]

**Address:** 0x40008030

**Access:** Read/Write

31	30	29	28	27	26	25	24
DLYBCT							
23	22	21	20	19	18	17	16
DLYBS							
15	14	13	12	11	10	9	8
SCBR							
7	6	5	4	3	2	1	0
BITS				CSAAT	CSNAAT	NCPHA	CPOL

This register can only be written if the WPEN bit is cleared in "SPI Write Protection Mode Register".

Note: SPI\_CSRx registers must be written even if the user wants to use the defaults. The BITS field will not be updated with the translated value unless the register is written.

- **CPOL: Clock Polarity**

0 = The inactive state value of SPCK is logic level zero.

1 = The inactive state value of SPCK is logic level one.

CPOL is used to determine the inactive state value of the serial clock (SPCK). It is used with NCPHA to produce the required clock/data relationship between master and slave devices.

- **NCPHA: Clock Phase**

0 = Data is changed on the leading edge of SPCK and captured on the following edge of SPCK.

1 = Data is captured on the leading edge of SPCK and changed on the following edge of SPCK.

NCPHA determines which edge of SPCK causes data to change and which edge causes data to be captured. NCPHA is used with CPOL to produce the required clock/data relationship between master and slave devices.

- **CSNAAT: Chip Select Not Active After Transfer (Ignored if CSAAT = 1)**

0 = The Peripheral Chip Select does not rise between two transfers if the SPI\_TDR is reloaded before the end of the first transfer and if the two transfers occur on the same Chip Select.

1 = The Peripheral Chip Select rises systematically after each transfer performed on the same slave. It remains active after the end of transfer for a minimal duration of:

- $\frac{DLYBCT}{MCK}$  (if DLYBCT field is different from 0)

- $\frac{DLYBCT + 1}{MCK}$  (if DLYBCT field equals 0)

- **CSAAT: Chip Select Active After Transfer**

0 = The Peripheral Chip Select Line rises as soon as the last transfer is achieved.

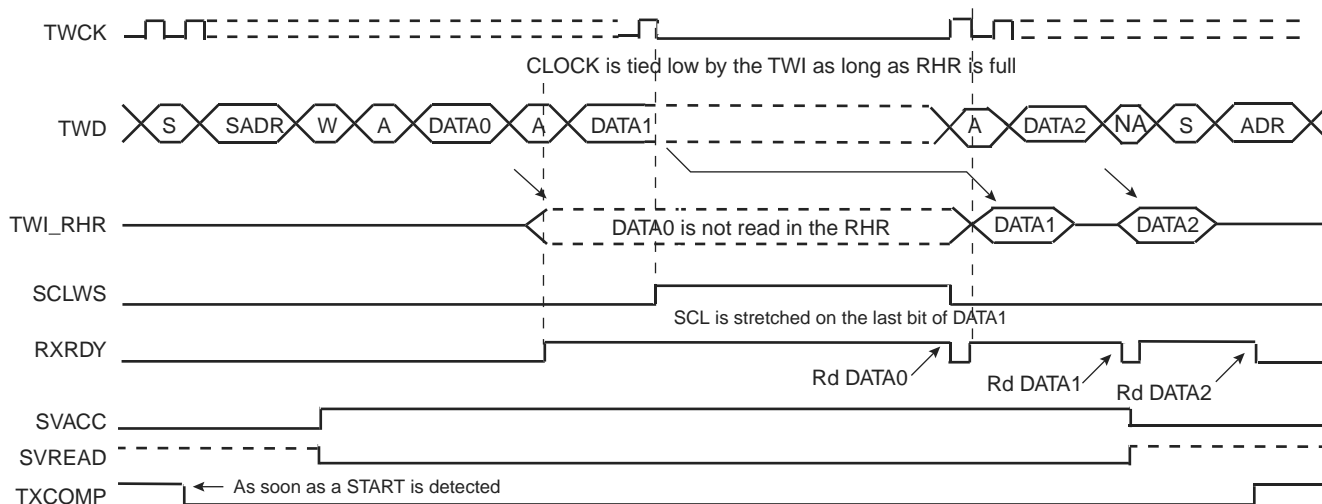
1 = The Peripheral Chip Select does not rise after the last transfer is achieved. It remains active until a new transfer is requested on a different chip select.

## Clock Synchronization in Write Mode

The clock is tied low if the shift register and the TWI\_RHR is full. If a STOP or REPEATED\_START condition was not detected, it is tied low until TWI\_RHR is read.

Figure 32-29 on page 650 describes the clock synchronization in Read mode.

**Figure 32-29. Clock Synchronization in Write Mode**



- Notes:
1. At the end of the read sequence, TXCOMP is set after a STOP or after a REPEATED\_START + an address different from SADR.
  2. SCLWS is automatically set when the clock synchronization mechanism is started and automatically reset when the mechanism is finished.

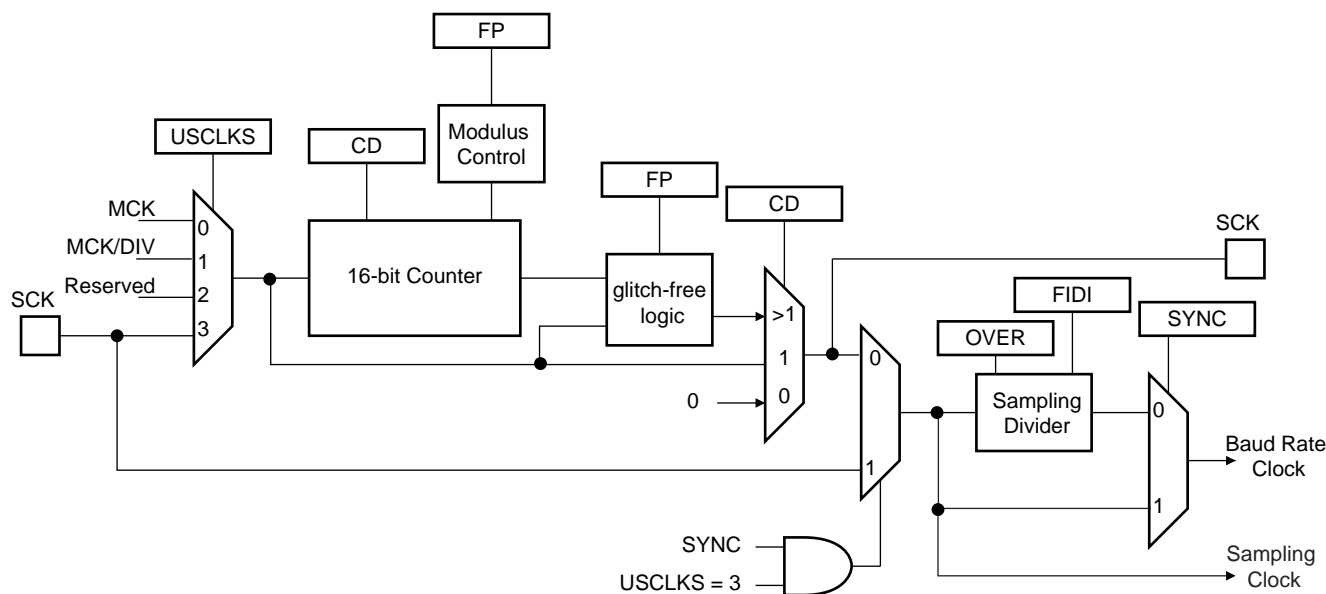
### 34.7.1.2 Fractional Baud Rate in Asynchronous Mode

The Baud Rate generator previously defined is subject to the following limitation: the output frequency changes by only integer multiples of the reference frequency. An approach to this problem is to integrate a fractional N clock generator that has a high resolution. The generator architecture is modified to obtain Baud Rate changes by a fraction of the reference source clock. This fractional part is programmed with the FP field in the Baud Rate Generator Register (US\_BRGR). If FP is not 0, the fractional part is activated. The resolution is one eighth of the clock divider. This feature is only available when using USART normal mode. The fractional Baud Rate is calculated using the following formula:

$$\text{Baudrate} = \frac{\text{SelectedClock}}{\left(8(2 - \text{Over})\left(\text{CD} + \frac{\text{FP}}{8}\right)\right)}$$

The modified architecture is presented below:

**Figure 34-4. Fractional Baud Rate Generator**



### 34.7.1.3 Baud Rate in Synchronous Mode or SPI Mode

If the USART is programmed to operate in synchronous mode, the selected clock is simply divided by the field CD in US\_BRGR.

$$\text{BaudRate} = \frac{\text{SelectedClock}}{\text{CD}}$$

In synchronous mode, if the external clock is selected (USCLKS = 3), the clock is provided directly by the signal on the USART SCK pin. No division is active. The value written in US\_BRGR has no effect. The external clock frequency must be at least 3 times lower than the system clock. In synchronous mode master (USCLKS = 0 or 1, CLK0 set to 1), the receive part limits the SCK maximum frequency to MCK/3 in USART mode, or MCK/6 in SPI mode.

When either the external clock SCK or the internal clock divided (MCK/DIV) is selected, the value programmed in CD must be even if the user has to ensure a 50:50 mark/space ratio on the SCK pin. If the internal clock MCK is selected, the Baud Rate Generator ensures a 50:50 duty cycle on the SCK pin, even if the value programmed in CD is odd.

- **FIFOEMPTY:** FIFO Empty Interrupt Mask
- **XFRDONE:** Transfer Done Interrupt Mask
- **ACKRCV:** Boot Operation Acknowledge Received Interrupt Mask
- **ACKRCVE:** Boot Operation Acknowledge Error Interrupt Mask
- **OVRE:** Overrun Interrupt Mask
- **UNRE:** Underrun Interrupt Mask

0 = The corresponding interrupt is not enabled.

1 = The corresponding interrupt is enabled.

**Table 37-5. Register Mapping (Continued)**

Offset	Register	Name	Access	Reset
0x200 + ch_num * 0x20 + 0x00	PWM Channel Mode Register <sup>(1)</sup>	PWM_CMR	Read-write	0x0
0x200 + ch_num * 0x20 + 0x04	PWM Channel Duty Cycle Register <sup>(1)</sup>	PWM_CDTY	Read-write	0x0
0x200 + ch_num * 0x20 + 0x08	PWM Channel Duty Cycle Update Register <sup>(1)</sup>	PWM_CDTYUPD	Write-only	–
0x200 + ch_num * 0x20 + 0x0C	PWM Channel Period Register <sup>(1)</sup>	PWM_CPRD	Read-write	0x0
0x200 + ch_num * 0x20 + 0x10	PWM Channel Period Update Register <sup>(1)</sup>	PWM_CPRDUPD	Write-only	–
0x200 + ch_num * 0x20 + 0x14	PWM Channel Counter Register <sup>(1)</sup>	PWM_CCNT	Read-only	0x0
0x200 + ch_num * 0x20 + 0x18	PWM Channel Dead Time Register <sup>(1)</sup>	PWM_DT	Read-write	0x0
0x200 + ch_num * 0x20 + 0x1C	PWM Channel Dead Time Update Register <sup>(1)</sup>	PWM_DTUPD	Write-only	–

Notes: 1. Some registers are indexed with “ch\_num” index ranging from 0 to 3.



- **OPMODE2: OpMode2**

0 = no effect.

1 = set to force the OpMode signal (UTMI interface) to “10”, to disable the bit-stuffing and the NRZI encoding.

Note: For the Test mode, Test\_SE0\_NAK (see Universal Serial Bus Specification, Revision 2.0: 7.1.20, Test Mode Support). Force the device in High Speed mode, and configure a bulk-type endpoint. Do not fill this endpoint for sending NAK to the host.

Upon command, a port's transceiver must enter the High Speed receive mode and remain in that mode until the exit action is taken. This enables the testing of output impedance, low level output voltage and loading characteristics. In addition, while in this mode, upstream facing ports (and only upstream facing ports) must respond to any IN token packet with a NAK handshake (only if the packet CRC is determined to be correct) within the normal allowed device response time. This enables testing of the device squelch level circuitry and, additionally, provides a general purpose stimulus/response test for basic functional testing.

### 38.7.20 UDPHS DMA Channel Address Register

**Name:** UDPHS\_DMAADDRESSx [x = 0..5]

**Address:** 0x400A4304 [0], 0x400A4314 [1], 0x400A4324 [2], 0x400A4334 [3], 0x400A4344 [4], 0x400A4354 [5]

**Access:** Read-write

31	30	29	28	27	26	25	24
BUFF_ADD							
23	22	21	20	19	18	17	16
BUFF_ADD							
15	14	13	12	11	10	9	8
BUFF_ADD							
7	6	5	4	3	2	1	0
BUFF_ADD							

Note: Channel 0 is not used.

#### • BUFF\_ADD

This field determines the AHB bus starting address of a DMA channel transfer.

Channel start and end addresses may be aligned on any byte boundary.

The firmware may write this field only when the UDPHS\_DMASTATUS register CHANN\_ENB bit is clear.

This field is updated at the end of the address phase of the current access to the AHB bus. It is incrementing of the access byte width. The access width is 4 bytes (or less) at packet start or end, if the start or end address is not aligned on a word boundary.

The packet start address is either the channel start address or the next channel address to be accessed in the channel buffer.

The packet end address is either the channel end address or the latest channel address accessed in the channel buffer.

The channel start address is written by software or loaded from the descriptor, whereas the channel end address is either determined by the end of buffer or the UDPHS device, USB end of transfer if the UDPHS\_DMACONTROLx register END\_TR\_EN bit is set.

Table 42-5. VDDUTMI Supply Monitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_T$	Supply Monitor Threshold	16 selectable steps of 100mV	1.9		3.4	V
$V_{T(accuracy)}$	Threshold Level Accuracy		-1.5		+1.5	%
$V_{hys}$	Hysteresis Voltage			20	30	mV
$I_{DDON}$	Current Consumption on VDDCORE	Enabled		18	28	$\mu A$
$I_{DDOFF}$		Disabled			1	
$t_{START}$	Startup Time	From disabled state to enabled state			140	$\mu s$

Figure 42-2. VDDUTMI Supply Monitor

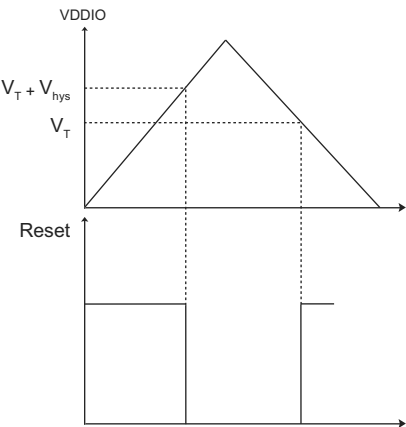
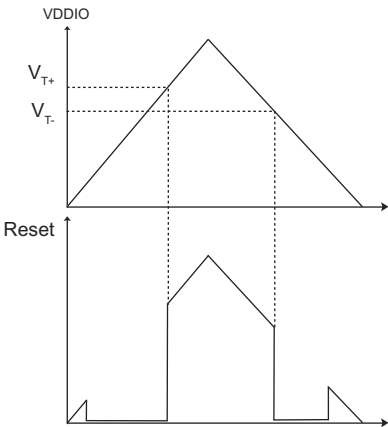


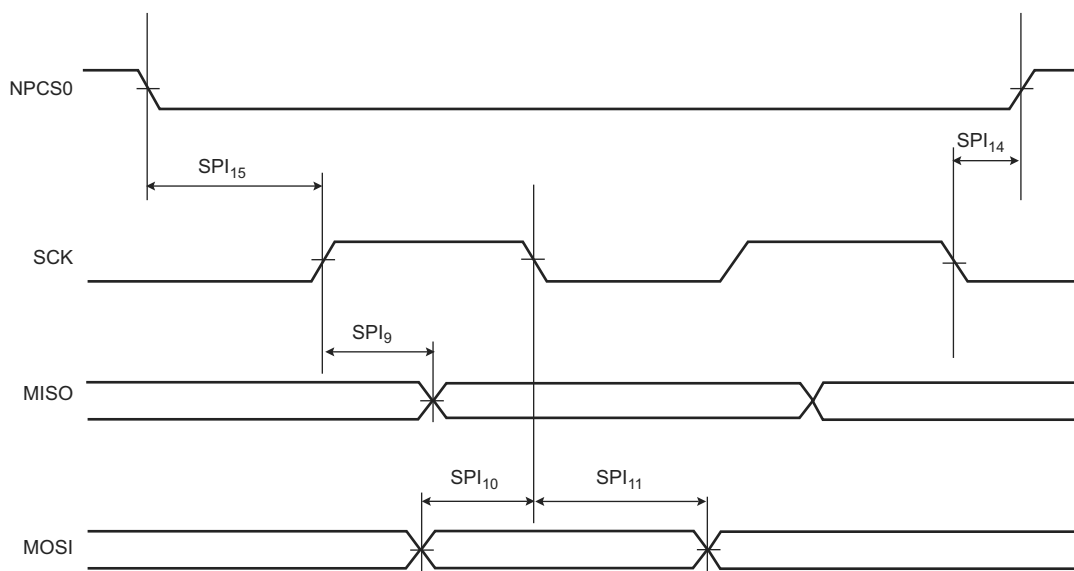
Table 42-6. Backup Power Supply Zero-Power-on Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{T+}$	Threshold Voltage Rising	At startup	1.50	1.55	1.60	V
$V_{T-}$	Threshold Voltage Falling		1.40	1.45	1.50	V
$t_{RST}$	Reset Period		40	90	150	$\mu s$

Figure 42-3. Zero-Power-on Reset Characteristics



**Figure 42-20. SPI Slave Mode with (CPOL = NCPHA = 0) or (CPOL = NCPHA = 1)**



### 42.9.3.1 Maximum SPI Frequency

The following formulas give maximum SPI frequency in Master read and write modes and in Slave read and write modes.

#### Master Write Mode

The SPI only sends data to a slave device such as an LCD, for example. The limit is given by SPI<sub>2</sub> (or SPI<sub>5</sub>) timing. Since it gives a maximum frequency above the maximum pad speed (see Section 42.9.2 "I/O Characteristics"), the max SPI frequency is defined by the pin FreqMax value.

#### Master Read Mode

$$f_{SPCK}^{Max} = \frac{1}{SPI_0(or SPI_3) + t_{valid}}$$

$t_{valid}$  is the slave time response to output data after detecting an SPCK edge. For a non-volatile memory with  $t_{valid}$  (or  $t_v$ ) = 12 ns,  $f_{SPCK}^{Max}$  = 38.5 MHz at  $V_{DDIO}$  = 3.3V.

#### Slave Read Mode

In slave mode, SPCK is the input clock for the SPI. The max SPCK frequency is given by setup and hold timings SPI<sub>7</sub>/SPI<sub>8</sub>(or SPI<sub>10</sub>/SPI<sub>11</sub>). Since this gives a frequency well above the pad limit, the limit in slave read mode is given by SPCK pad.

#### Slave Write Mode

$$f_{SPCK}^{Max} = \frac{1}{SPI_6(or SPI_9) + t_{su}}$$

For 3.3V I/O domain and SPI6,  $f_{SPCK}^{Max}$  = 33 MHz.  $t_{su}$  is the setup time from the master before sampling data.

Doc Rev 6430B	Comments (Continued)	Change Request Ref. <sup>(1)</sup>
	Electrical Characteristics: Section 42. "Electrical Characteristics", updated Section 42.9.3.1 "Maximum SPI Frequency", added Figure 42-5 "Measurement Setup", updated. Table 42-46, "I/O Characteristics", in the Conditions column: $V_{DDIO} = 1.62V$	rfo  6663
	Mechanical Characteristics: Section 43.5 "Soldering Profile", added.	rfo

Doc. Rev.	Date	Comments	Change Request Ref.
6430A	24-Mar-09	First Issue - advance information	
	16-May-09	Review	
	29-May-09	Approved	

Note: 1. "rfo" in this column indicates changes requested during document review and approval loop.