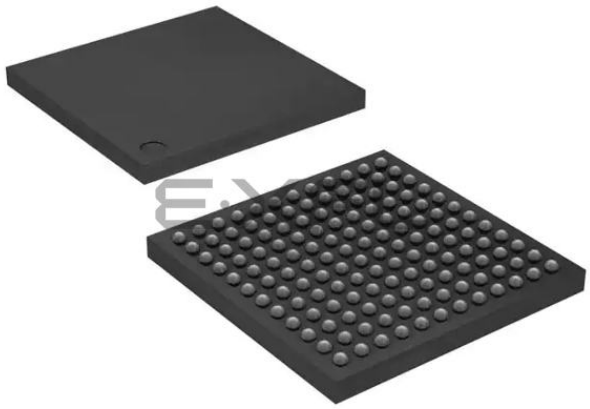

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	96
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3u1eb-cu

5.5 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.6 Low-power Modes

The SAM3U has the following low-power modes: Backup, Wait, and Sleep.

5.6.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (< 0.5 ms).

The Supply Controller, zero-power power-on reset, RTT, RTC, backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deep-sleep mode with the voltage regulator disabled.

The SAM3U Series can be woken up from this mode through the Force Wake-Up (FWUP) pin, and Wake-Up input pins WKUP0–15, Supply Monitor, RTT or RTC wake-up event. Current consumption is 2.5 µA typical on VDDBU.

Backup mode can be entered by using the WFE instruction.

The procedure to enter Backup mode using the WFE instruction is the following:

1. Write a 1 to the SLEEPDEEP bit in the Cortex-M3 processor System Control Register (SCR) (refer to Section 12.20.7 ”System Control Register”).
2. Execute the WFE instruction of the processor.

Exit from Backup mode happens if one of the following enable wake-up events occurs:

- Low level, configurable debouncing on FWUP pin
- Level transition, configurable debouncing on pins WKUPEN0–15
- SM alarm
- RTC alarm
- RTT alarm

5.6.2 Wait Mode

The purpose of the Wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake up the core (WFE). This is done by configuring the external lines WKUP0–15 as fast startup wake-up pins (refer to Section 5.8 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Current Consumption in Wait mode is typically 15 µA on VDDIN if the internal voltage regulator is used or 8 µA on VDDCORE if an external regulator is used.

The procedure to enter Wait mode is the following:

1. Select the 4/8/12 MHz fast RC oscillator as Main Clock
2. Set the LPM bit in PMC_FSMR
3. Execute the WFE instruction of the processor

Table 12-13. Cortex-M3 instructions (Continued)

Mnemonic	Operands	Brief description	Flags	Page
SDIV	{Rd,} Rn, Rm	Signed Divide	-	page 121
SEV	-	Send Event	-	page 144
SMLAL	RdLo, RdHi, Rn, Rm	Signed Multiply with Accumulate (32 x 32 + 64), 64-bit result	-	page 120
SMULL	RdLo, RdHi, Rn, Rm	Signed Multiply (32 x 32), 64-bit result	-	page 120
SSAT	Rd, #n, Rm {,shift #s}	Signed Saturate	Q	page 122
STM	Rn{!}, reglist	Store Multiple registers, increment after	-	page 99
STMDB, STMEA	Rn{!}, reglist	Store Multiple registers, decrement before	-	page 99
STMFD, STMIA	Rn{!}, reglist	Store Multiple registers, increment after	-	page 99
STR	Rt, [Rn, #offset]	Store Register word	-	page 94
STRB, STRBT	Rt, [Rn, #offset]	Store Register byte	-	page 94
STRD	Rt, Rt2, [Rn, #offset]	Store Register two words	-	page 94
STREX	Rd, Rt, [Rn, #offset]	Store Register Exclusive	-	page 102
STREXB	Rd, Rt, [Rn]	Store Register Exclusive byte	-	page 102
STREXH	Rd, Rt, [Rn]	Store Register Exclusive halfword	-	page 102
STRH, STRHT	Rt, [Rn, #offset]	Store Register halfword	-	page 94
STRT	Rt, [Rn, #offset]	Store Register word	-	page 94
SUB, SUBS	{Rd,} Rn, Op2	Subtract	N,Z,C,V	page 106
SUB, SUBW	{Rd,} Rn, #imm12	Subtract	N,Z,C,V	page 106
SVC	#imm	Supervisor Call	-	page 145
SXTB	{Rd,} Rm {,ROR #n}	Sign extend a byte	-	page 127
SXTH	{Rd,} Rm {,ROR #n}	Sign extend a halfword	-	page 127
TBB	[Rn, Rm]	Table Branch Byte	-	page 134
TBH	[Rn, Rm, LSL #1]	Table Branch Halfword	-	page 134
TEQ	Rn, Op2	Test Equivalence	N,Z,C	page 117
TST	Rn, Op2	Test	N,Z,C	page 117
UBFX	Rd, Rn, #lsb, #width	Unsigned Bit Field Extract	-	page 126
UDIV	{Rd,} Rn, Rm	Unsigned Divide	-	page 121
UMLAL	RdLo, RdHi, Rn, Rm	Unsigned Multiply with Accumulate (32 x 32 + 64), 64-bit result	-	page 120
UMULL	RdLo, RdHi, Rn, Rm	Unsigned Multiply (32 x 32), 64-bit result	-	page 120
USAT	Rd, #n, Rm {,shift #s}	Unsigned Saturate	Q	page 122
UXTB	{Rd,} Rm {,ROR #n}	Zero extend a byte	-	page 127
UXTH	{Rd,} Rm {,ROR #n}	Zero extend a halfword	-	page 127
WFE	-	Wait For Event	-	page 146
WFI	-	Wait For Interrupt	-	page 147

12.19.4 Interrupt Set-pending Registers

The ISPR0 register forces interrupts into the pending state, and shows which interrupts are pending. See:

- the register summary in Table 12-27 on page 149 for the register attributes
- Table 12-28 on page 150 for which interrupts are controlled by each register.

The bit assignments are:

31	30	29	28	27	26	25	24
SETPEND							

23	22	21	20	19	18	17	16
SETPEND							

15	14	13	12	11	10	9	8
SETPEND							

7	6	5	4	3	2	1	0
SETPEND							

- **SETPEND**

Interrupt set-pending bits.

Write:

0 = no effect.

1 = changes interrupt state to pending.

Read:

0 = interrupt is not pending.

1 = interrupt is pending.

Writing 1 to the ISPR bit corresponding to:

- an interrupt that is pending has no effect
- a disabled interrupt sets the state of that interrupt to pending

12.20.11.3 Usage Fault Status Register

The UFSR indicates the cause of a usage fault. The bit assignments are:

15	14	13	12	11	10	9	8
Reserved						DIVBYZERO	UNALIGNED

7	6	5	4	3	2	1	0
Reserved				NOCP	INVPC	INVSTATE	UNDEFINSTR

- **DIVBYZERO**

Divide by zero usage fault:

0 = no divide by zero fault, or divide by zero trapping not enabled

1 = the processor has executed an SDIV or UDIV instruction with a divisor of 0.

When the processor sets this bit to 1, the PC value stacked for the exception return points to the instruction that performed the divide by zero.

Enable trapping of divide by zero by setting the DIV_0_TRP bit in the CCR to 1, see “Configuration and Control Register” on page 171.

- **UNALIGNED**

Unaligned access usage fault:

0 = no unaligned access fault, or unaligned access trapping not enabled

1 = the processor has made an unaligned memory access.

Enable trapping of unaligned accesses by setting the UNALIGN_TRP bit in the CCR to 1, see “Configuration and Control Register” on page 171.

Unaligned LDM, STM, LDRD, and STRD instructions always fault irrespective of the setting of UNALIGN_TRP.

- **NOCP**

No coprocessor usage fault. The processor does not support coprocessor instructions:

0 = no usage fault caused by attempting to access a coprocessor

1 = the processor has attempted to access a coprocessor.

- **INVPC**

Invalid PC load usage fault, caused by an invalid PC load by EXC_RETURN:

0 = no invalid PC load usage fault

1 = the processor has attempted an illegal load of EXC_RETURN to the PC, as a result of an invalid context, or an invalid EXC_RETURN value.

When this bit is set to 1, the PC value stacked for the exception return points to the instruction that tried to perform the illegal load of the PC.

- **INVSTATE**

Invalid state usage fault:

0 = no invalid state usage fault

1 = the processor has attempted to execute an instruction that makes illegal use of the EPSR.

When this bit is set to 1, the PC value stacked for the exception return points to the instruction that attempted the illegal use of the EPSR.

This bit is not set to 1 if an undefined instruction uses the EPSR.

12.20.12Hard Fault Status Register

The HFSR gives information about events that activate the hard fault handler. See the register summary in Table 12-30 on page 161 for its attributes.

This register is read, write to clear. This means that bits in the register read normally, but writing 1 to any bit clears that bit to 0. The bit assignments are:

31	30	29	28	27	26	25	24
DEBUGEVT	FORCED	Reserved					

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						VECTTBL	Reserved

- **DEBUGEVT**

Reserved for Debug use. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable.

- **FORCED**

Indicates a forced hard fault, generated by escalation of a fault with configurable priority that cannot be handles, either because of priority or because it is disabled:

0 = no forced hard fault

1 = forced hard fault.

When this bit is set to 1, the hard fault handler must read the other fault status registers to find the cause of the fault.

- **VECTTBL**

Indicates a bus fault on a vector table read during exception processing:

0 = no bus fault on vector table read

1 = bus fault on vector table read.

This error is always handled by the hard fault handler.

When this bit is set to 1, the PC value stacked for the exception return points to the instruction that was preempted by the exception.

The HFSR bits are sticky. This means as one or more fault occurs, the associated bits are set to 1. A bit that is set to 1 is cleared to 0 only by writing 1 to that bit, or by a reset.

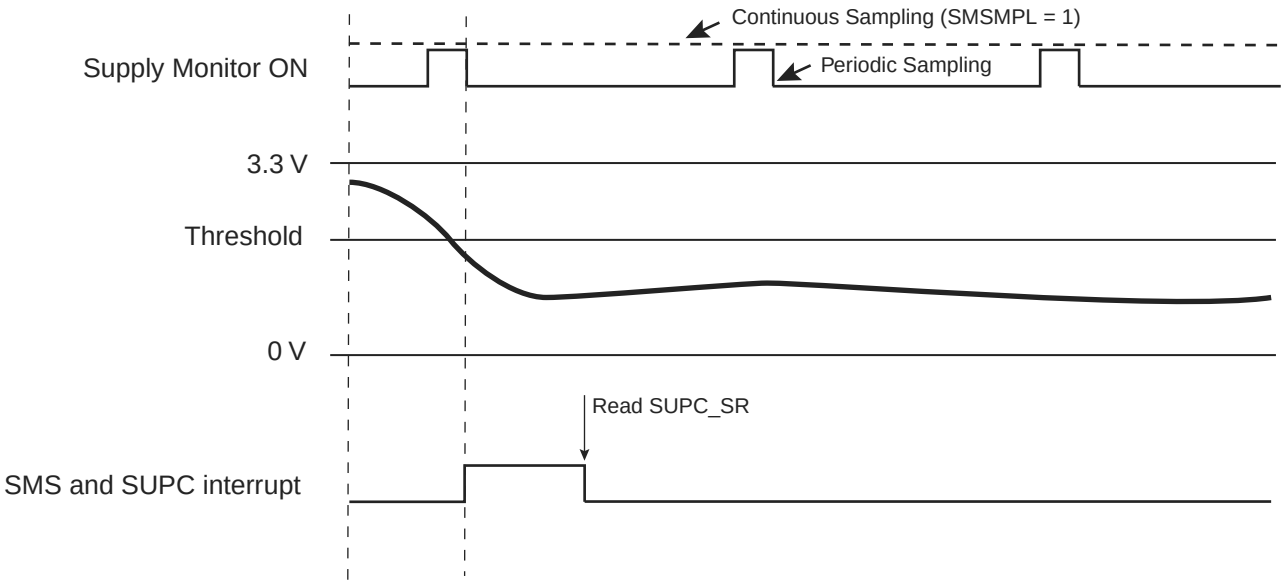
Waking up the core power supply when a supply monitor detection occurs can be enabled by programming the SMEN bit to 1 in the Supply Controller Wake Up Mode Register (SUPC_WUMR).

The Supply Controller provides two status bits in the Supply Controller Status Register for the supply monitor which allows to determine whether the last wake up was due to the supply monitor:

- The SMOS bit provides real time information, which is updated at each measurement cycle or updated at each Slow Clock cycle, if the measurement is continuous.
- The SMS bit provides saved information and shows a supply monitor detection has occurred since the last read of SUPC_SR.

The SMS bit can generate an interrupt if the SMIEN bit is set to 1 in the Supply Controller Supply Monitor Mode Register (SUPC_SMMR).

Figure 18-4. Supply Monitor Status Bit and Associated Interrupt



18.5.7 System Controller Wake Up Inputs Register

Name: SUPC_WUIR

Address: 0x400E1220

Access: Read-write

31	30	29	28	27	26	25	24
WKUPT15	WKUPT14	WKUPT13	WKUPT12	WKUPT11	WKUPT10	WKUPT9	WKUPT8
23	22	21	20	19	18	17	16
WKUPT7	WKUPT6	WKUPT5	WKUPT4	WKUPT3	WKUPT2	WKUPT1	WKUPT0
15	14	13	12	11	10	9	8
WKUPEN15	WKUPEN14	WKUPEN13	WKUPEN12	WKUPEN11	WKUPEN10	WKUPEN9	WKUPEN8
7	6	5	4	3	2	1	0
WKUPEN7	WKUPEN6	WKUPEN5	WKUPEN4	WKUPEN3	WKUPEN2	WKUPEN1	WKUPEN0

- **WKUPEN0 - WKUPEN15: Wake Up Input Enable 0 to 15**

0 (NOT_ENABLE) = the corresponding wake-up input has no wake up effect.

1 (ENABLE) = the corresponding wake-up input forces the wake up of the core power supply.

- **WKUPT0 - WKUPT15: Wake Up Input Transition 0 to 15**

0 (HIGH_TO_LOW) = a high to low level transition on the corresponding wake-up input forces the wake up of the core power supply.

1 (LOW_TO_HIGH) = a low to high level transition on the corresponding wake-up input forces the wake up of the core power supply.

24.10.3.1 NWE Waveforms

The NWE signal is characterized by a setup timing, a pulse width and a hold timing.

1. NWE_SETUP: the NWE setup time is defined as the setup of address and data before the NWE falling edge.
2. NWE_PULSE: The NWE pulse length is the time between NWE falling edge and NWE rising edge.
3. NWE_HOLD: The NWE hold time is defined as the hold time of address and data after the NWE rising edge.

The NWE waveforms apply to all byte-write lines in Byte Write access mode: NWR0 to NWR3.

24.18.18 SMC Pulse Register

Name: SMC_PULSEx [x=0..3]

Address: 0x400E0074 [0], 0x400E0088 [1], 0x400E009C [2], 0x400E00B0 [3]

Access: Read-write

Reset: 0x01010101

31	30	29	28	27	26	25	24
–	–	NCS_RD_PULSE					

23	22	21	20	19	18	17	16
–	–	NRD_PULSE					

15	14	13	12	11	10	9	8
–	–	NCS_WR_PULSE					

7	6	5	4	3	2	1	0
–	–	NWE_PULSE					

- **NWE_PULSE: NWE Pulse Length**

The NWE signal pulse length is defined as:

NWE pulse length = (256 * NWE_PULSE[6]+NWE_PULSE[5:0]) clock cycles.

The NWE pulse must be at least one clock cycle.

- **NCS_WR_PULSE: NCS Pulse Length in WRITE Access**

In Write access, The NCS signal pulse length is defined as:

NCS pulse length = (256 * NCS_WR_PULSE[6] + NCS_WR_PULSE[5:0]) clock cycles.

the NCS pulse must be at least one clock cycle.

- **NRD_PULSE: NRD Pulse Length**

The NRD signal pulse length is defined as:

NRD pulse length = (256 * NRD_PULSE[6] + NRD_PULSE[5:0]) clock cycles.

The NRD pulse width must be as least 1 clock cycle.

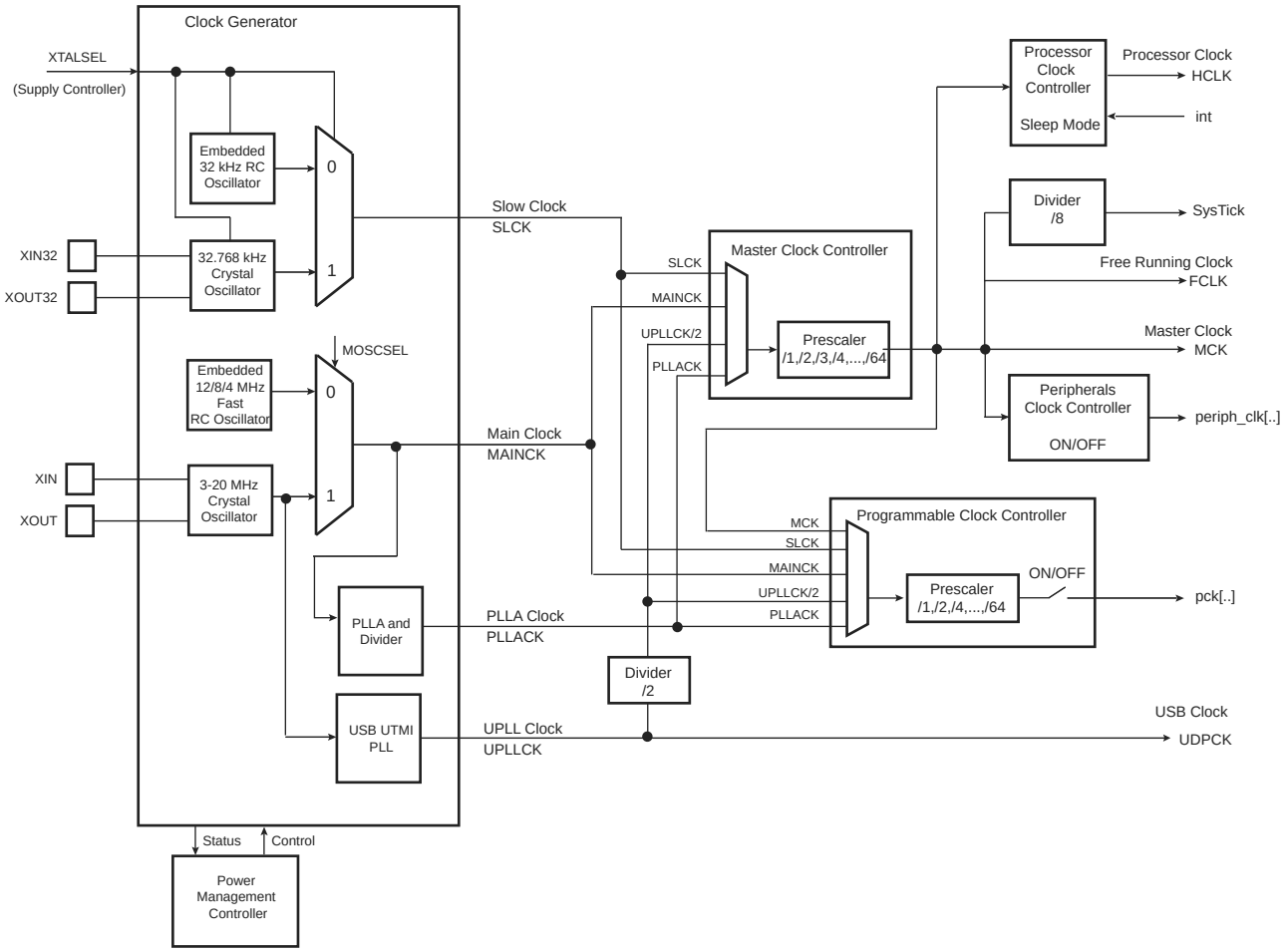
- **NCS_RD_PULSE: NCS Pulse Length in READ Access**

In READ mode, The NCS signal pulse length is defined as:

NCS pulse length = (256 * NCS_RD_PULSE[6] + NCS_RD_PULSE[5:0]) clock cycles.

27.2 Block Diagram

Figure 27-1. General Clock Block Diagram



27.3 Master Clock Controller

The Master Clock Controller provides selection and division of the Master Clock (MCK). MCK is the clock provided to all the peripherals and the memory controller.

The Master Clock is selected from one of the clocks provided by the Clock Generator. Selecting the Slow Clock provides a Slow Clock signal to the whole device. Selecting the Main Clock saves power consumption of the PLLs.

The Master Clock Controller is made up of a clock selector and a prescaler.

The Master Clock selection is made by writing the CSS field (Clock Source Selection) in PMC_MCKR (Master Clock Register). The prescaler supports the division by a power of 2 of the selected clock between 1 and 64, and the division by 3. The PRES field in PMC_MCKR programs the prescaler.

Each time PMC_MCKR is written to define a new Master Clock, the MCKRDY bit is cleared in PMC_SR. It reads 0 until the Master Clock is established. Then, the MCKRDY bit is set and can trigger an interrupt to the processor. This feature is useful when switching from a high-speed clock to a lower one to inform the software when the change is actually done.

29.7.16 PIO Controller Interrupt Mask Register

Name: PIO_IMR

Address: 0x400E0C48 (PIOA), 0x400E0E48 (PIOB), 0x400E1048 (PIOC)

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Change Interrupt Mask**

0 = Input Change Interrupt is disabled on the I/O line.

1 = Input Change Interrupt is enabled on the I/O line.

Figure 32-20. TWI Read Operation with Multiple Data Bytes with or without Internal Address

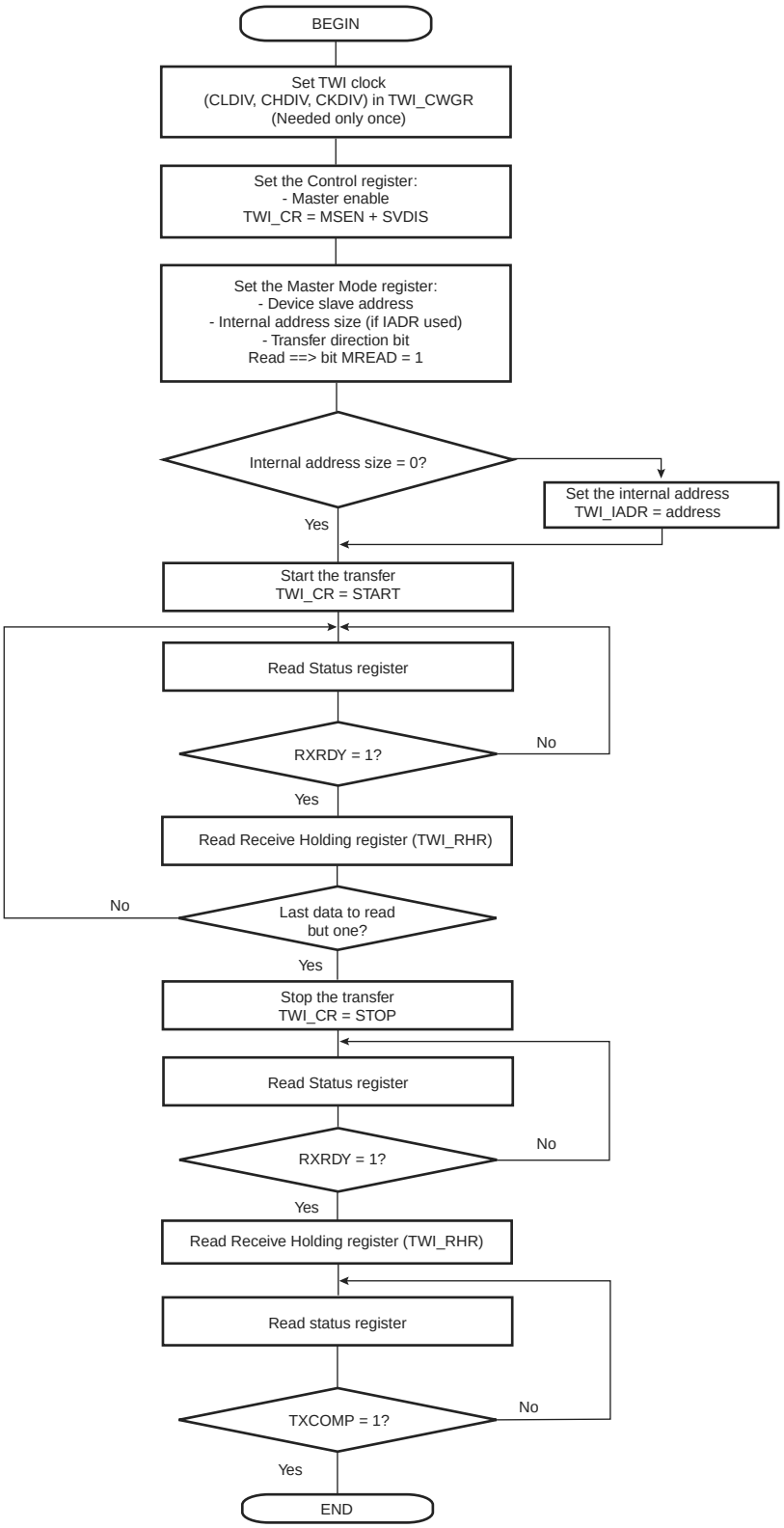
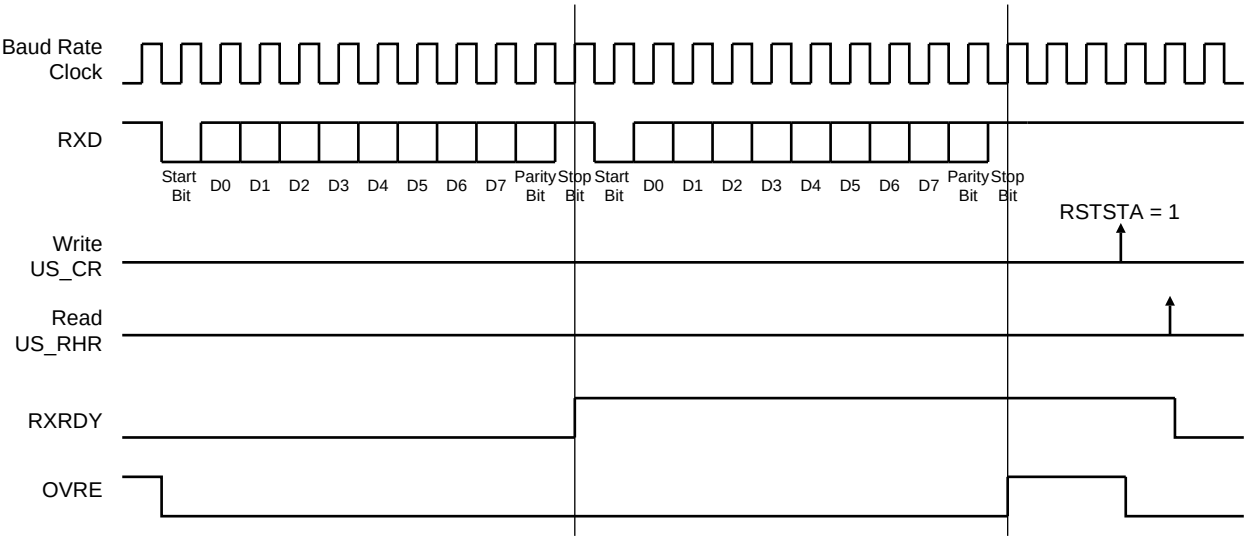


Figure 34-21. Receiver Status



34.7.3.8 Parity

The USART supports five parity modes selected by programming the PAR field in the Mode Register (US_MR). The PAR field also enables the Multidrop mode, see “Multidrop Mode” on page 705. Even and odd parity bit generation and error detection are supported.

If even parity is selected, the parity generator of the transmitter drives the parity bit to 0 if a number of 1s in the character data bit is even, and to 1 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If odd parity is selected, the parity generator of the transmitter drives the parity bit to 1 if a number of 1s in the character data bit is even, and to 0 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If the mark parity is used, the parity generator of the transmitter drives the parity bit to 1 for all characters. The receiver parity checker reports an error if the parity bit is sampled to 0. If the space parity is used, the parity generator of the transmitter drives the parity bit to 0 for all characters. The receiver parity checker reports an error if the parity bit is sampled to 1. If parity is disabled, the transmitter does not generate any parity bit and the receiver does not report any parity error.

Table 34-8 shows an example of the parity bit for the character 0x41 (character ASCII “A”) depending on the configuration of the USART. Because there are two bits to 1, 1 bit is added when a parity is odd, or 0 is added when a parity is even.

Table 34-8. Parity Bit Examples

Character	Hexa	Binary	Parity Bit	Parity Mode
A	0x41	0100 0001	1	Odd
A	0x41	0100 0001	0	Even
A	0x41	0100 0001	1	Mark
A	0x41	0100 0001	0	Space
A	0x41	0100 0001	None	None

When the receiver detects a parity error, it sets the PARE (Parity Error) bit in the Channel Status Register (US_CSR). The PARE bit can be cleared by writing the Control Register (US_CR) with the RSTSTA bit to 1. Figure 34-22 illustrates the parity bit status setting and clearing.

Figure 34-38. SPI Transfer Format (CPHA=1, 8 bits per transfer)

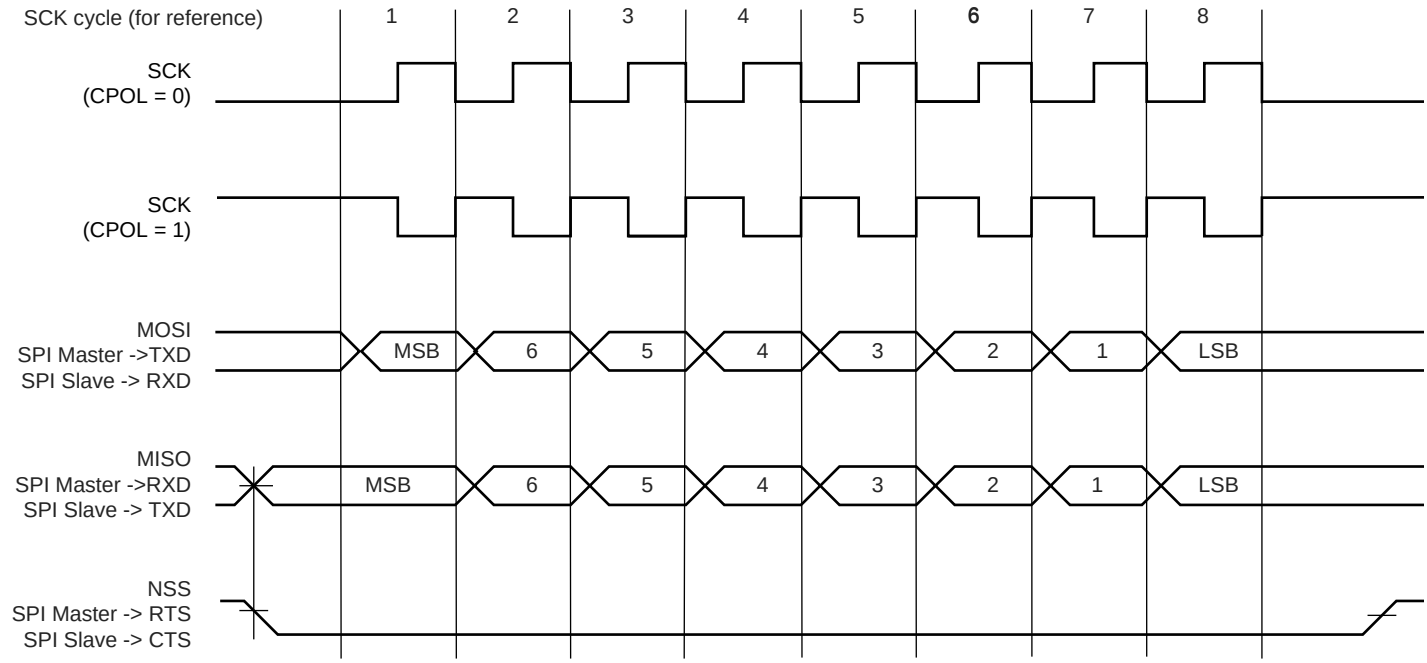
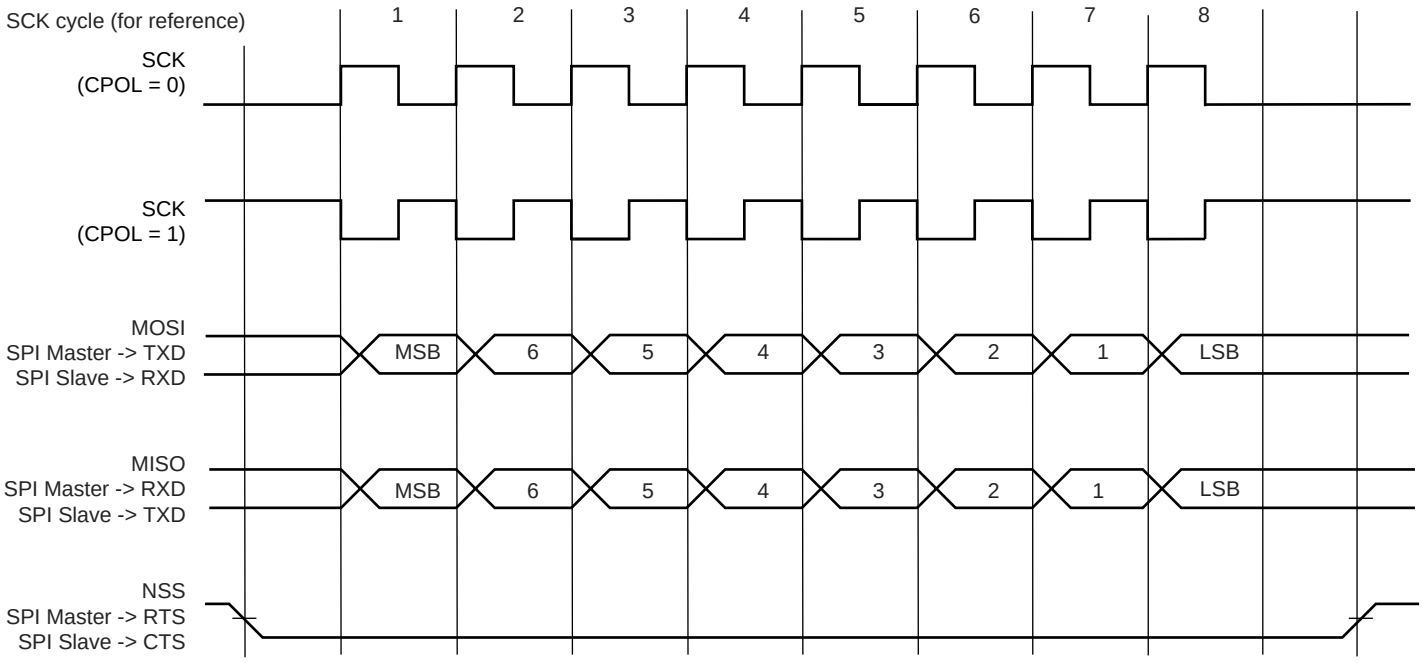


Figure 34-39. SPI Transfer Format (CPHA=0, 8 bits per transfer)



34.7.8.4 Receiver and Transmitter Control

See “Receiver and Transmitter Control” on page 696.

34.8.5 USART Interrupt Mask Register

Name: US_IMR

Address: 0x40090010 (0), 0x40094010 (1), 0x40098010 (2), 0x4009C010 (3)

Access: Read-only

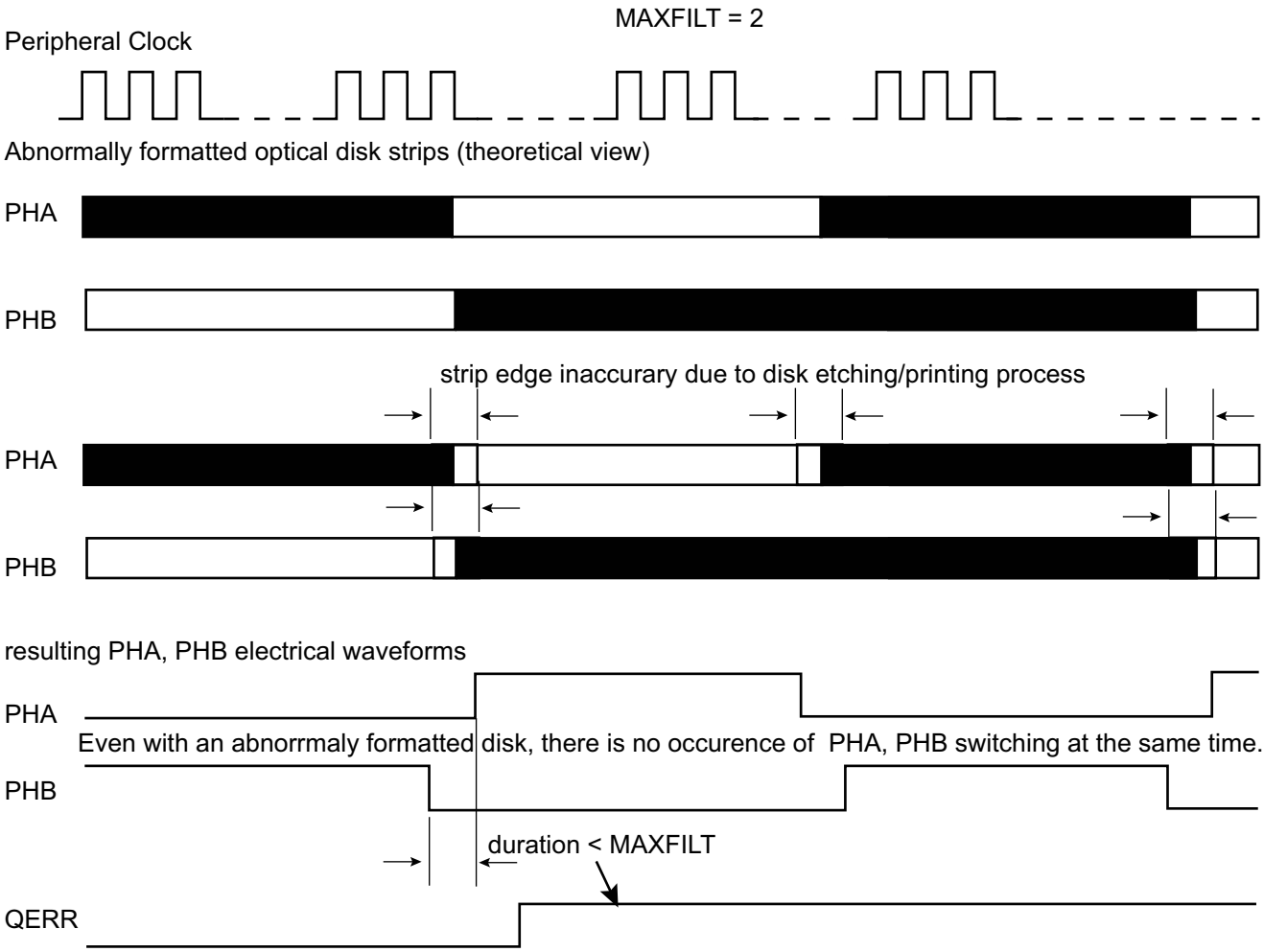
31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	MANE
23	22	21	20	19	18	17	16
–	–	–	–	CTSIC	DCDIC	DSRIC	RIIC
15	14	13	12	11	10	9	8
–	–	NACK	RXBUFF	TXBUFE	ITER/UNRE	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

- **RXRDY: RXRDY Interrupt Mask**
- **TXRDY: TXRDY Interrupt Mask**
- **RXBRK: Receiver Break Interrupt Mask**
- **ENDRX: End of Receive Transfer Interrupt Mask**
- **ENDTX: End of Transmit Interrupt Mask**
- **OVRE: Overrun Error Interrupt Mask**
- **FRAME: Framing Error Interrupt Mask**
- **PARE: Parity Error Interrupt Mask**
- **TIMEOUT: Time-out Interrupt Mask**
- **TXEMPTY: TXEMPTY Interrupt Mask**
- **ITER: Max number of Repetitions Reached Mask**
- **UNRE: SPI Underrun Error Mask**
- **TXBUFE: Buffer Empty Interrupt Mask**
- **RXBUFF: Buffer Full Interrupt Mask**
- **NACK: Non AcknowledgeInterrupt Mask**
- **RIIC: Ring Indicator Input Change Mask**
- **DSRIC: Data Set Ready Input Change Mask**

Figure 35-19. Quadrature Error Detection



MAXFILT must be tuned according to several factors such as the peripheral clock frequency, type of rotary sensor and rotation speed to be achieved.

35.6.14.4 Position and Rotation Measurement

When the POSEN bit is set in the TC_BMR, the motor axis position is processed on channel 0 (by means of the PHA, PHB edge detections) and the number of motor revolutions are recorded on channel 1 if the IDX signal is provided on the TIOB1 input. The position measurement can be read in the TC_CV0 register and the rotation measurement can be read in the TC_CV1 register.

Channel 0 and 1 must be configured in Capture mode (TC_CMR0.WAVE = 0). ‘Rising edge’ must be selected as the External Trigger Edge (TC_CMR.ETRGEDG = 0x01) and ‘TIOA’ must be selected as the External Trigger (TC_CMR.ABETRG = 0x1).

In parallel, the number of edges are accumulated on timer/counter channel 0 and can be read on the TC_CV0 register.

Therefore, the accurate position can be read on both TC_CV registers and concatenated to form a 32-bit word.

The timer/counter channel 0 is cleared for each increment of IDX count value.

Depending on the quadrature signals, the direction is decoded and allows to count up or down in timer/counter channels 0 and 1. The direction status is reported on TC_QISR.

38.7.1 UDPHS Control Register

Name: UDPHS_CTRL

Address: 0x400A4000

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	PULLD_DIS	REWAKEUP	DETACH	EN_UDPHS

7	6	5	4	3	2	1	0
FADDR_EN	DEV_ADDR						

- **DEV_ADDR: UDPHS Address**

This field contains the default address (0) after power-up or UDPHS bus reset (read), or it is written with the value set by a SET_ADDRESS request received by the device firmware (write).

- **FADDR_EN: Function Address Enable**

0 = Device is not in address state (read), or only the default function address is used (write).

1 = Device is in address state (read), or this bit is set by the device firmware after a successful status phase of a SET_ADDRESS transaction (write). When set, the only address accepted by the UDPHS controller is the one stored in the UDPHS Address field. It will not be cleared afterwards by the device firmware. It is cleared by hardware on hardware reset, or when UDPHS bus reset is received.

- **EN_UDPHS: UDPHS Enable**

0 = UDPHS is disabled (read), or this bit disables and resets the UDPHS controller (write). Disable the UTMI transceiver. The UTMI may disable the pull-up.

1 = UDPHS is enabled (read), or this bit enables the UDPHS controller (write).

- **DETACH: Detach Command**

0 = UDPHS is attached (read), or this bit pulls up the DP line (attach command) (write).

1 = UDPHS is detached, UTMI transceiver is suspended (read), or this bit simulates a detach on the UDPHS line and forces the UTMI transceiver into suspend state (Suspend M = 0) (write).

See PULLD_DIS description below.

- **REWAKEUP: Send Remote Wake Up**

0 = Remote Wake Up is disabled (read), or this bit has no effect (write).

1 = Remote Wake Up is enabled (read), or this bit forces an external interrupt on the UDPHS controller for Remote Wake UP purposes.

An Upstream Resume is sent only after the UDPHS bus has been in SUSPEND state for at least 5 ms.

This bit is automatically cleared by hardware at the end of the Upstream Resume.

39.5.14 DMAC Channel x [x = 0..3] Destination Address Register

Name: DMAC_DADDRx [x = 0..3]

Addresses: 0x400B0040 [0], 0x400B0068 [1], 0x400B0090 [2], 0x400B00B8 [3]

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
DADDRx							

23	22	21	20	19	18	17	16
DADDRx							

15	14	13	12	11	10	9	8
DADDRx							

7	6	5	4	3	2	1	0
DADDRx							

- **DADDRx**

Channel x destination address. This register must be aligned with the destination transfer width.

Table 42-3. 1.8V Voltage Regulator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDIN}	DC Input Voltage Range		1.8	3.3	3.6	V
V_{DDOUT}	DC Output Voltage	Normal Mode		1.8		V
		Standby Mode		0		
$V_{O(accuracy)}$	Output Voltage Accuracy	I_{LOAD} = 0.5–150 mA	-3		3	%
I_{LOAD}	Maximum DC Output Current	V_{DDIN} > 2.2V			150	mA
		$V_{DDIN} \leq$ 2.2V			60	
$I_{LOAD-START}$	Maximum Peak Current during startup(3)	(3)			300	mA
$V_{DROPOUT}$	Dropout Voltage	V_{DDIN} = 1.8V I_{LOAD} = 60 mA			150	mV
V_{LINE}	Line Regulation	V_{DDIN} 2.7–3.6 V I_{LOAD} MAX		20	50	mV
$V_{LINE-TR}$	Transient Line regulation	V_{DDIN} 2.7–3.6 V $t_r = t_f$ = 5 µs I_{LOAD} Max CD_{OUT} = 4.7µF		50	100	mV
V_{LOAD}	Load Regulation	$V_{DDIN} \geq$ 2.2V I_{LOAD} = 10% to 90% MAX		20	50	mV
$V_{LOAD-TR}$	Transient Load Regulation	$V_{DDIN} \geq$ 2.2V I_{LOAD} = 10% to 90% MAX $t_r = t_f$ = 5 µs CD_{OUT} = 4.7 µF		50	100	mV
I_Q	Quiescent Current	Normal Mode @ I_{LOAD} = 0 mA		7	10	µA
		Normal Mode @ I_{LOAD} = 150 mA		700	1200	
		Standby Mode			1	
CD_{IN}	Input Decoupling Capacitor	(1)		10		µF
CD_{OUT}	Output Decoupling Capacitor	(2)		4.7		µF
		ESR	0.5		10	Ω
t_{on}	Turn on Time	CD_{OUT} = 4.7 µF, V_{DDOUT} reaches V_{T+} (core power brownout detector supply rising threshold)		120	250	µs
		CD_{OUT} = 4.7 µF, V_{DDOUT} reaches 1.8V (± 3%)		200	400	µs

Notes:
1. A 10 µF or higher ceramic capacitor must be connected between VDDIN and the closest GND pin of the device. This large decoupling capacitor is mandatory to reduce startup current, improving transient response and noise rejection.
2. To ensure stability, an external 4.7µF output capacitor, CD_{OUT} must be connected between the VDDOUT and the closest GND pin of the device. The ESR (Equivalent Series Resistance) of the capacitor must be in the range 0.5 to 10 Ω. Solid tantalum, and multilayer ceramic capacitors are all suitable as output capacitor. A 100 nF bypass capacitor between VDDOUT and the closest GND pin of the device decreases output noise and improves the load transient response.
3. Defined as the current needed to charge external bypass/decoupling capacitor network.

43.5 Soldering Profile

Table 43-15 gives the recommended soldering profile from J-STD-020C.

Table 43-15. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/sec. max.
Preheat Temperature 175°C ±25°C	180 sec. max.
Temperature Maintained Above 217°C	60 sec. to 150 sec.
Time within 5°C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260°C
Ramp-down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 min. max.

Note: The package is certified to be backward compatible with Pb/Sn soldering profile.

A maximum of three reflow passes is allowed per component.

43.6 Packaging Resources

Land Pattern Definition.

Refer to the following IPC Standards:

- IPC-7351A and IPC-782 (*Generic Requirements for Surface Mount Design and Land Pattern Standards*) http://landpatterns.ipc.org/default.asp
- Atmel Green and RoHS Policy and Package Material Declaration Data Sheet available on www.atmel.com