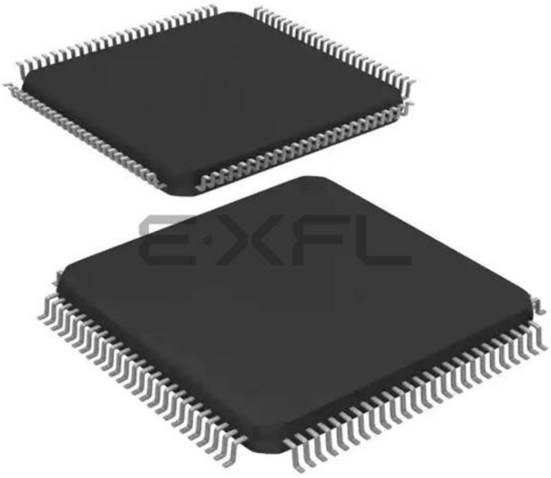

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 86 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg280f512g-e-qfp100 |

available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 2.1.19 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

### 2.1.20 Low Energy Timer (LETIMER)

The unique LETIMER$^{TM}$, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

### 2.1.21 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 2.1.22 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.23 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.24 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

### 2.1.25 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 2.1.26 Operational Amplifier (OPAMP)

The EFM32GG280 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

## 3.4 Current Consumption

### Table 3.3. Current Consumption

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EM0}$ | EM0 current. No prescaling. Running prime number calculation code from flash. (Production test condition = 14MHz) | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 219 | 240 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 205 | 225 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 206 | 229 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 209 | 232 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 211 | 234 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 215 | 242 | µA/ MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 243 | 327 | µA/ MHz |
| $I_{EM1}$ | EM1 current (Production test condition = 14MHz) | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 80 | 90 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 80 | 90 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 81 | 91 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 83 | 99 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 85 | 100 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 90 | 102 | µA/ MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 122 | 152 | µA/ MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 1.1[1] | 1.9[1] | µA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 8.8[1] | 21.5[1] | µA |
| $I_{EM3}$ | EM3 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.8[1] | 1.5[1] | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 8.2[1] | 20.3[1] | µA |
| $I_{EM4}$ | EM4 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.02 | 0.08 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 0.5 | 2.5 | µA |

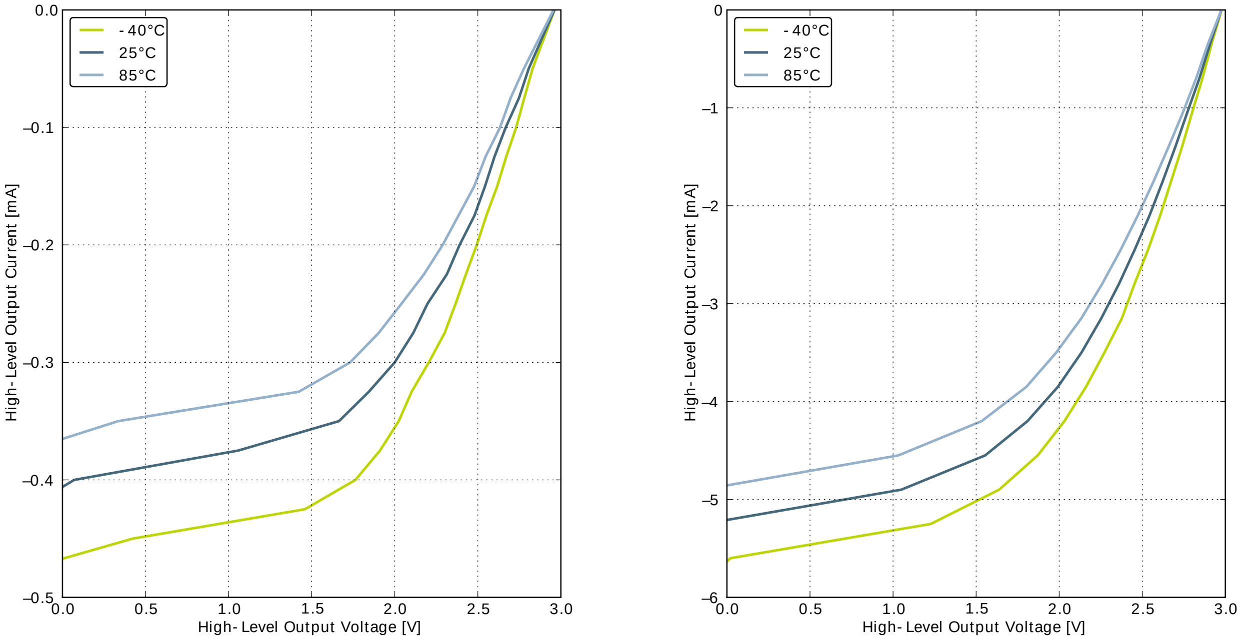
[1] Only one RAM block enabled. The RAM block size is 32 kB.

## 3.8 General Purpose Input Output

**Table 3.7. GPIO**

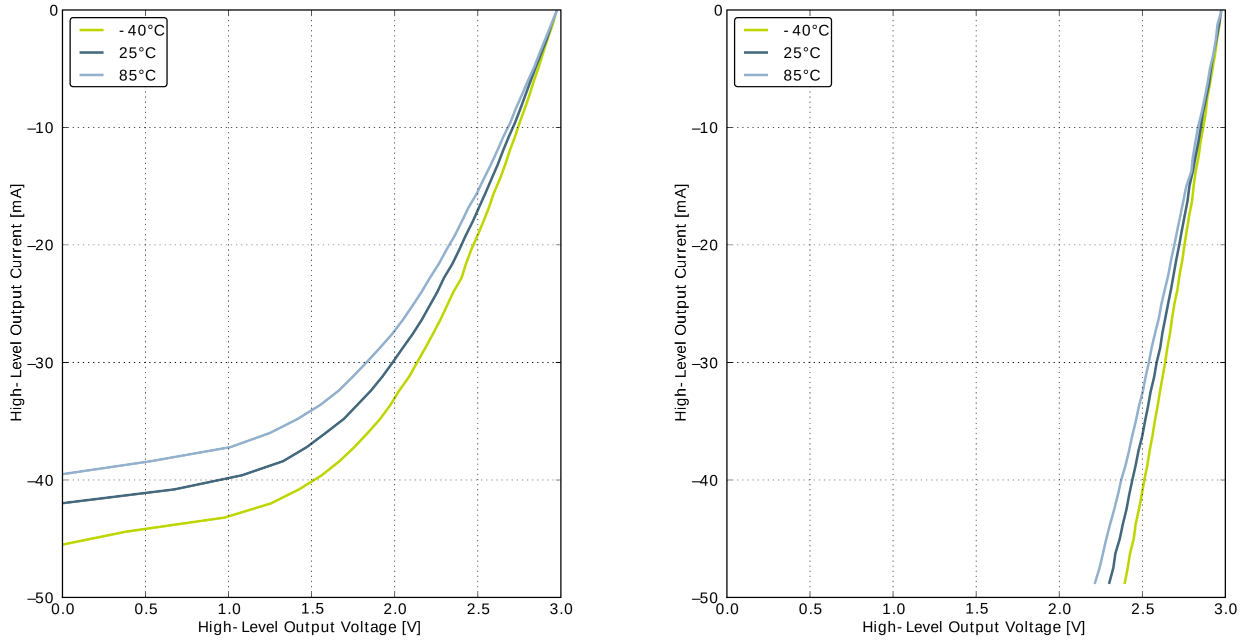
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | $0.30V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | $0.70V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.80V_{DD}$ | | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.90V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.85V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.90V_{DD}$ | | V |
| | | Sourcing 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.75V_{DD}$ | | | V |
| | | Sourcing 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.85V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.60V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.80V_{DD}$ | | | V |
| $V_{IOOL}$ | Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sinking 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.20V_{DD}$ | | V |
| | | Sinking 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.10V_{DD}$ | | V |
| | | Sinking 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.10V_{DD}$ | | V |
| | | Sinking 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.05V_{DD}$ | | V |
| | | Sinking 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | $0.30V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | $0.20V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | | | $0.35V_{DD}$ | V |

### Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

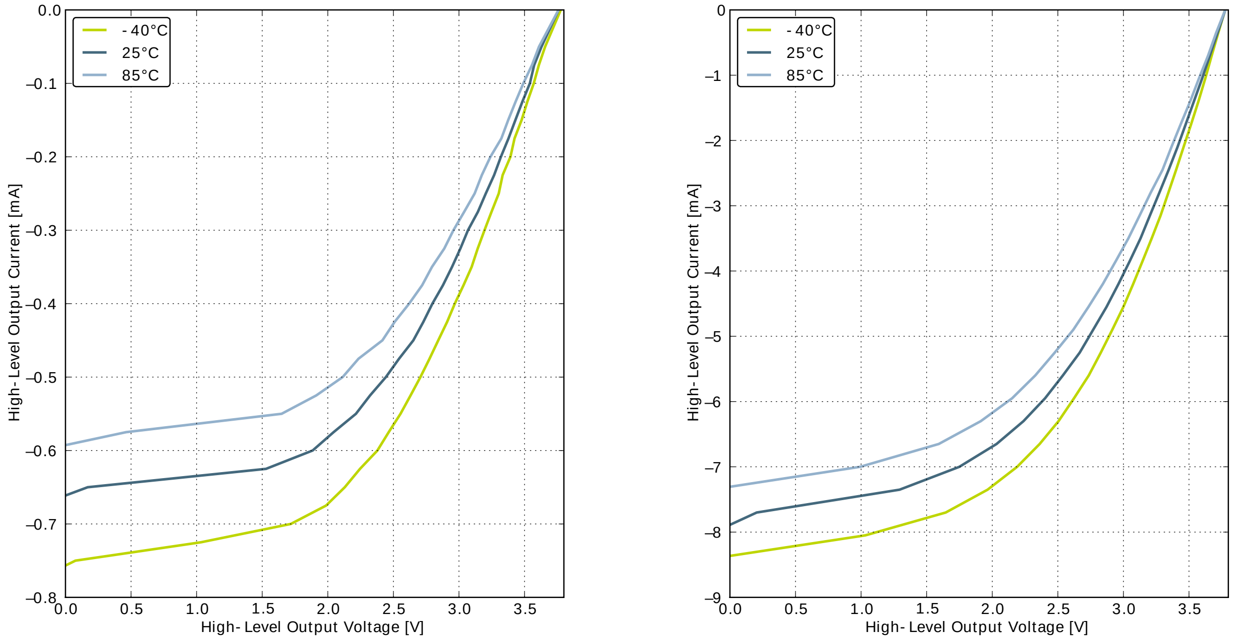
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

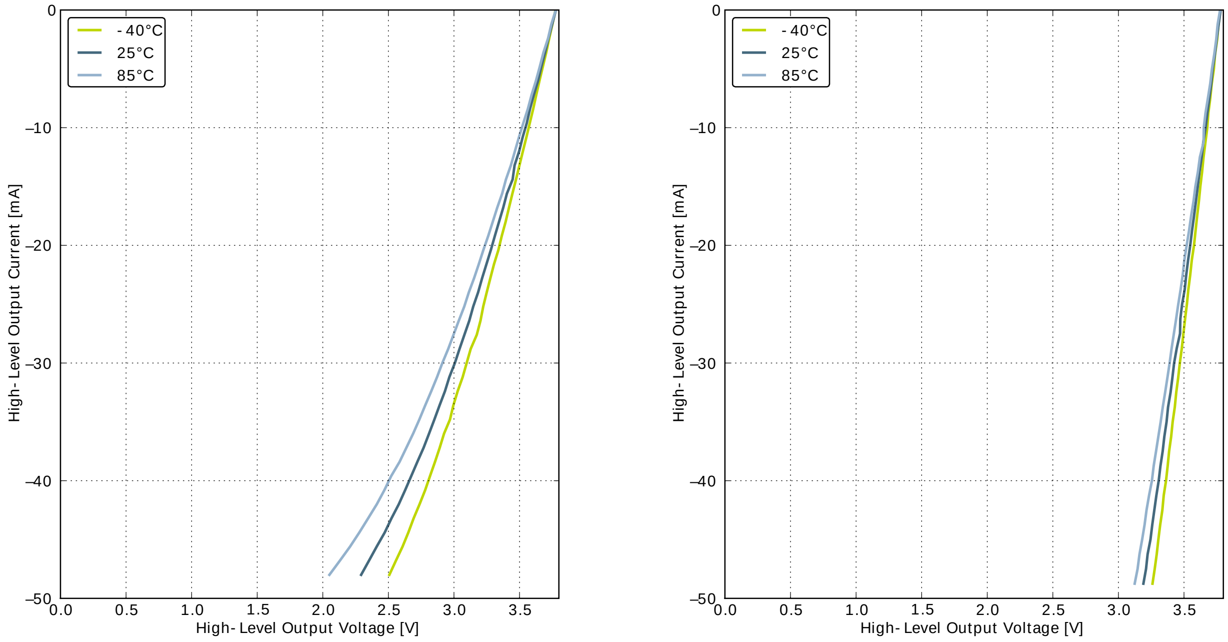
GPIO_Px_CTRL DRIVEMODE = HIGH

**Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage**



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

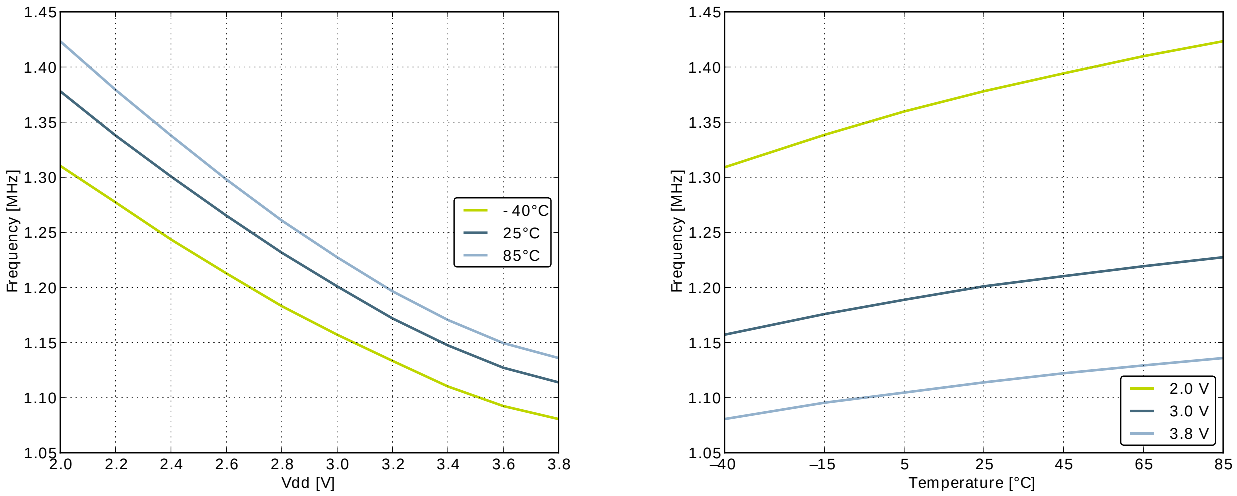
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{HFRCO}$ | Current consumption (Production test condition = 14MHz) | $f_{HFRCO}$ = 28 MHz | | 165 | 190 | µA |
| | | $f_{HFRCO}$ = 21 MHz | | 134 | 155 | µA |
| | | $f_{HFRCO}$ = 14 MHz | | 106 | 120 | µA |
| | | $f_{HFRCO}$ = 11 MHz | | 94 | 110 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | | 77 | 90 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | | 25 | 32 | µA |
| $TUNESTEP_{HFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[3] | | % |

[1] For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

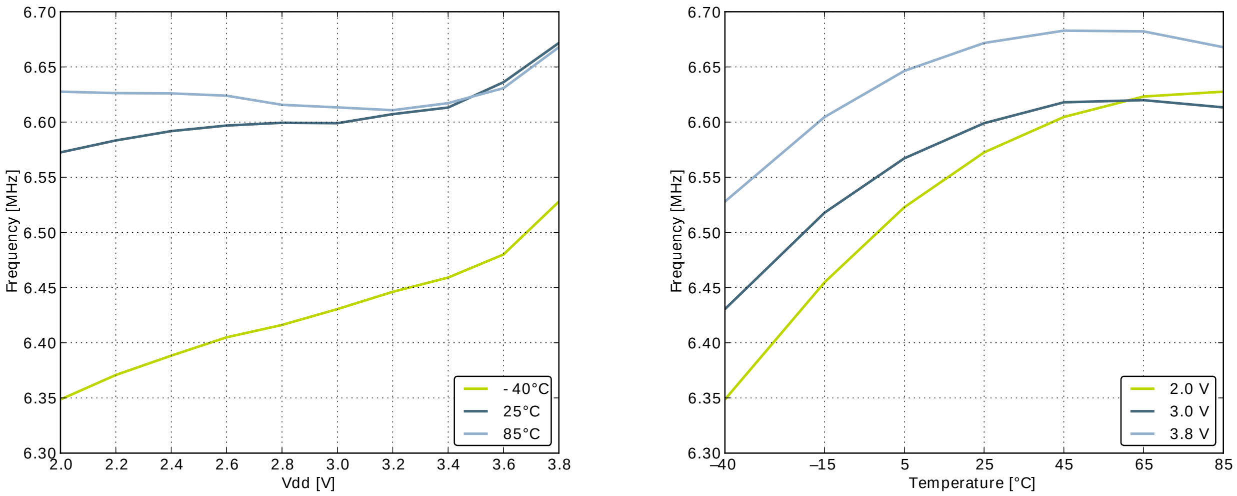
[2] For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3] The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature



### Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature



| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 67 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 63 | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 70 | | dB |
| $SINAD_{ADC}$ | SIgnal-to-Noise And Distortion-ratio (SINAD) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 62 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 66 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 68 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 61 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 65 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 62 | 65 | | dB |

***Figure 3.18. Differential Non-Linearity (DNL)***

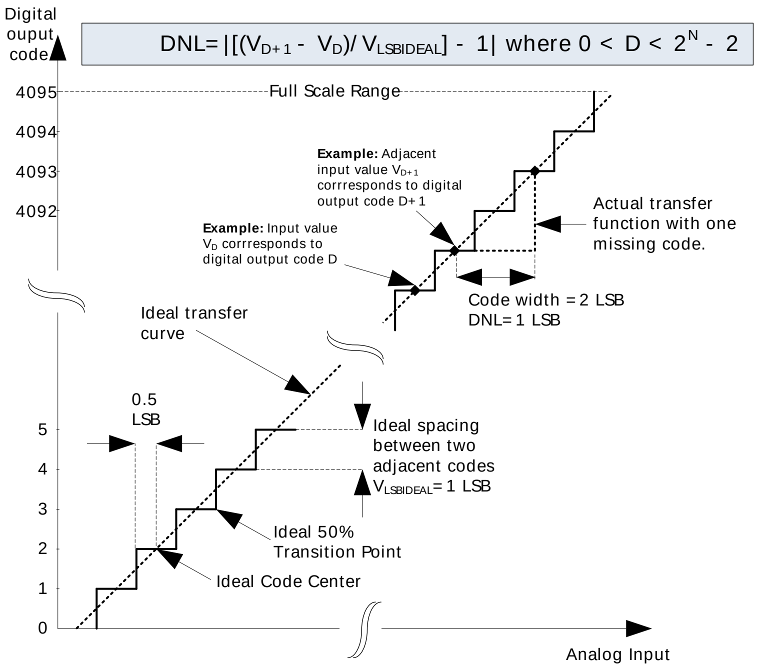
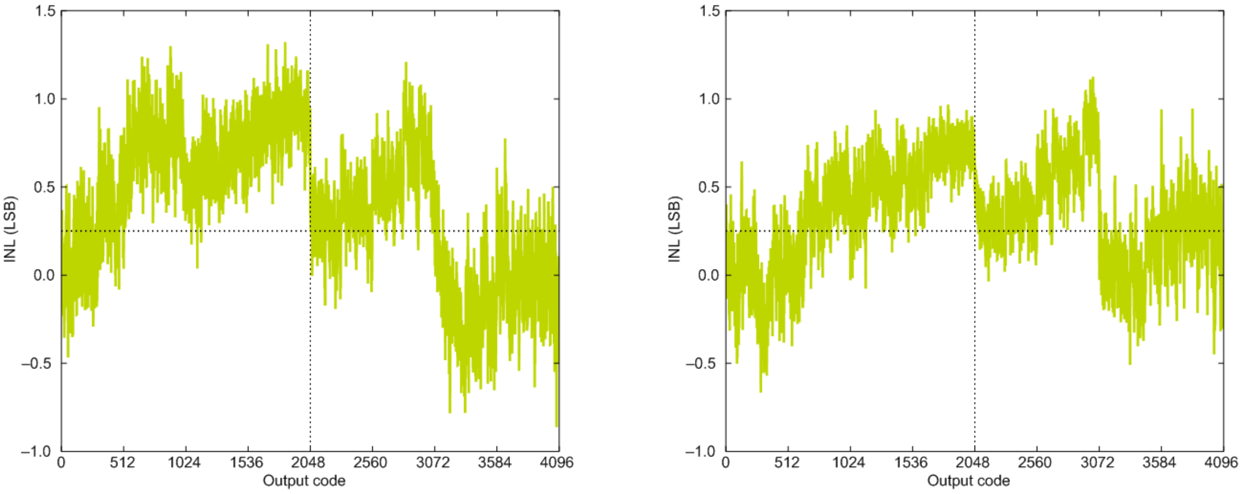
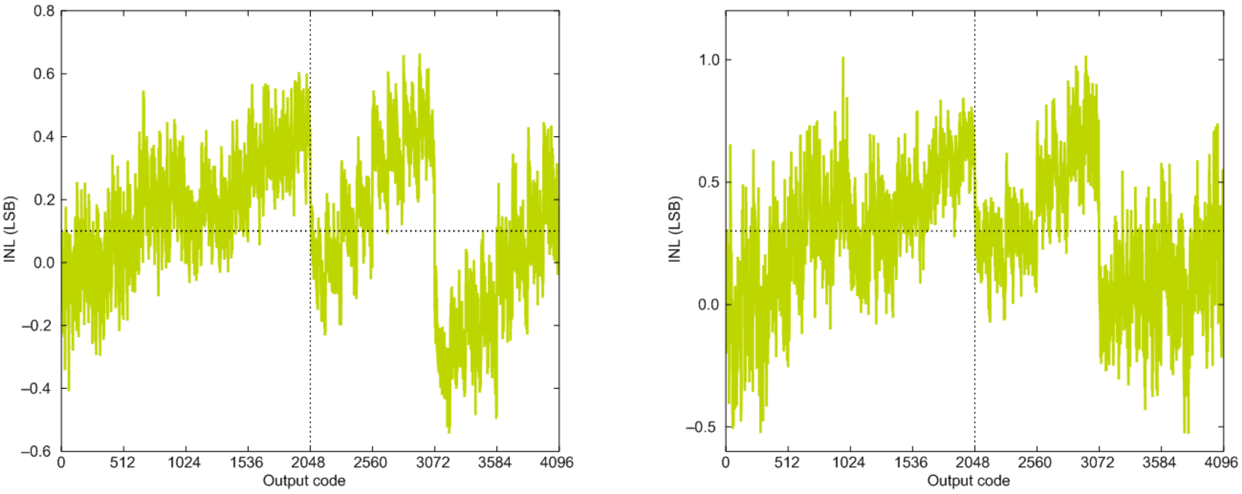


***Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C***



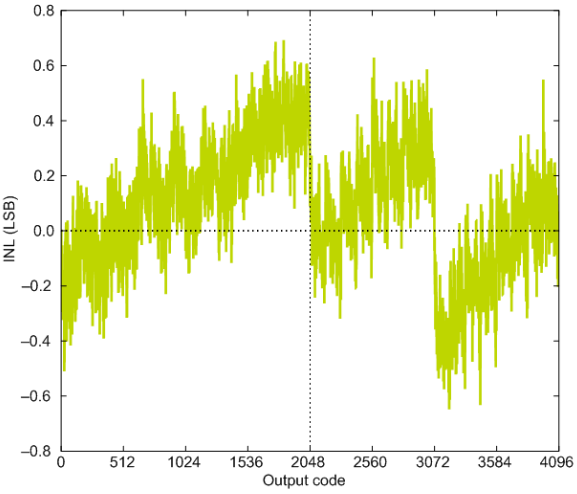
1.25V Reference

2.5V Reference



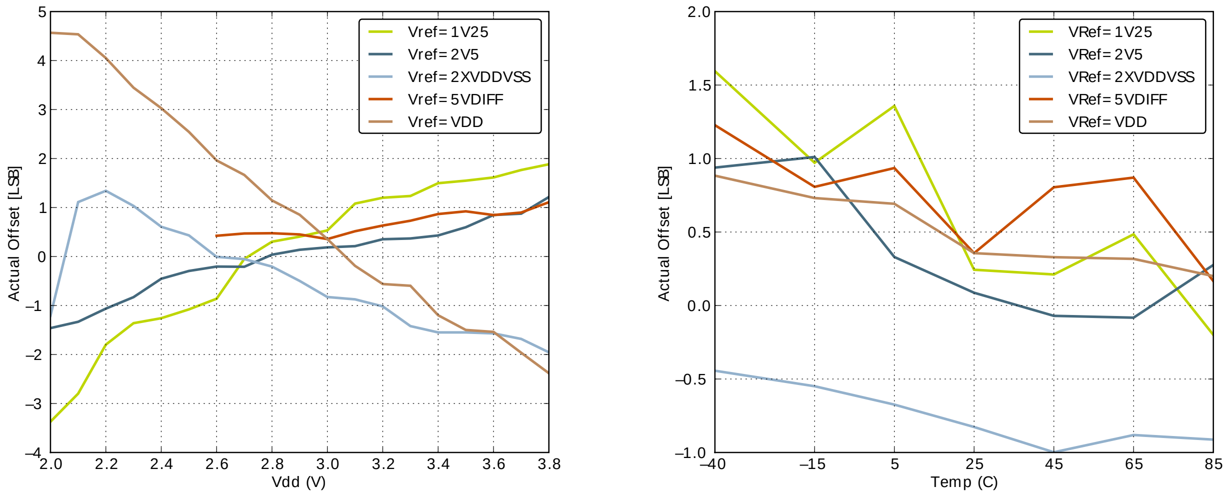
2XVDDVSS Reference

5VDIFF Reference



VDD Reference

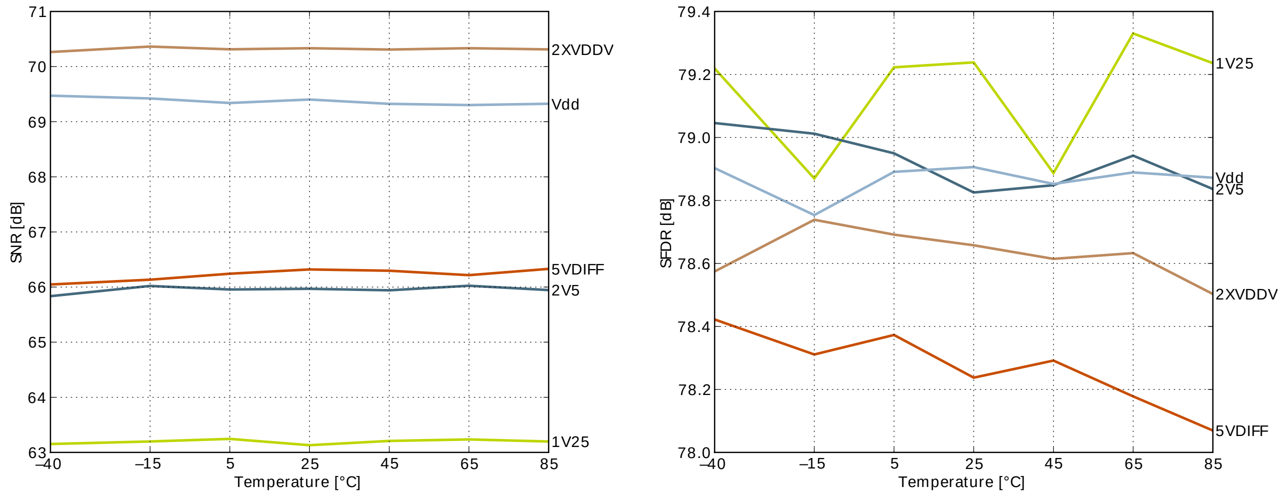
### Figure 3.22. ADC Absolute Offset, Common Mode = Vdd /2



Offset vs Supply Voltage, Temp = 25°C

Offset vs Temperature, Vdd = 3V

### Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



Signal to Noise Ratio (SNR)

Spurious-Free Dynamic Range (SFDR)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain | | 13 | 17 | µA |
| $G_{OL}$ | Open Loop Gain | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 101 | | dB |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 98 | | dB |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 91 | | dB |
| $GBW_{OPAMP}$ | Gain Bandwidth Product | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 6.1 | | MHz |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 1.8 | | MHz |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.25 | | MHz |
| $PM_{OPAMP}$ | Phase Margin | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, $C_L$=75 pF | | 64 | | ° |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| $R_{INPUT}$ | Input Resistance | | | 100 | | Mohm |
| $R_{LOAD}$ | Load Resistance | | 200 | | | Ohm |
| $I_{LOAD\_DC}$ | DC Load Current | | | | 11 | mA |
| $V_{INPUT}$ | Input Voltage | OPAxHCMDIS=0 | $V_{SS}$ | | $V_{DD}$ | V |
| | | OPAxHCMDIS=1 | $V_{SS}$ | | $V_{DD}$-1.2 | V |
| $V_{OUTPUT}$ | Output Voltage | | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{OFFSET}$ | Input Offset Voltage | Unity Gain, $V_{SS}<V_{in}<V_{DD}$, OPAxHCMDIS=0 | -13 | 0 | 11 | mV |
| | | Unity Gain, $V_{SS}<V_{in}<V_{DD}$-1.2, OPAxHCMDIS=1 | | 1 | | mV |
| $V_{OFFSET\_DRIFT}$ | Input Offset Voltage Drift | | | | 0.02 | mV/°C |
| $SR_{OPAMP}$ | Slew Rate | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 3.2 | | V/µs |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 0.8 | | V/µs |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.1 | | V/µs |
| $N_{OPAMP}$ | Voltage Noise | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=0 | | 101 | | $µV_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=1 | | 141 | | $µV_{RMS}$ |

## 3.14 Voltage Comparator (VCMP)

*Table 3.18. VCMP*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{VCMPIN}$ | Input voltage range | | | $V_{DD}$ | | V |
| $V_{VCMPCM}$ | VCMP Common Mode voltage range | | | $V_{DD}$ | | V |
| $I_{VCMP}$ | Active current | BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register | | 0.3 | 0.6 | µA |
| | | BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0. | | 22 | 30 | µA |
| $t_{VCMPREF}$ | Startup time reference generator | NORMAL | | 10 | | µs |
| $V_{VCMPOFFSET}$ | Offset voltage | Single ended | -230 | -40 | 190 | mV |
| | | Differential | | 10 | | mV |
| $V_{VCMPHYST}$ | VCMP hysteresis | | | 40 | | mV |
| $t_{VCMPSTART}$ | Startup time | | | | 10 | µs |

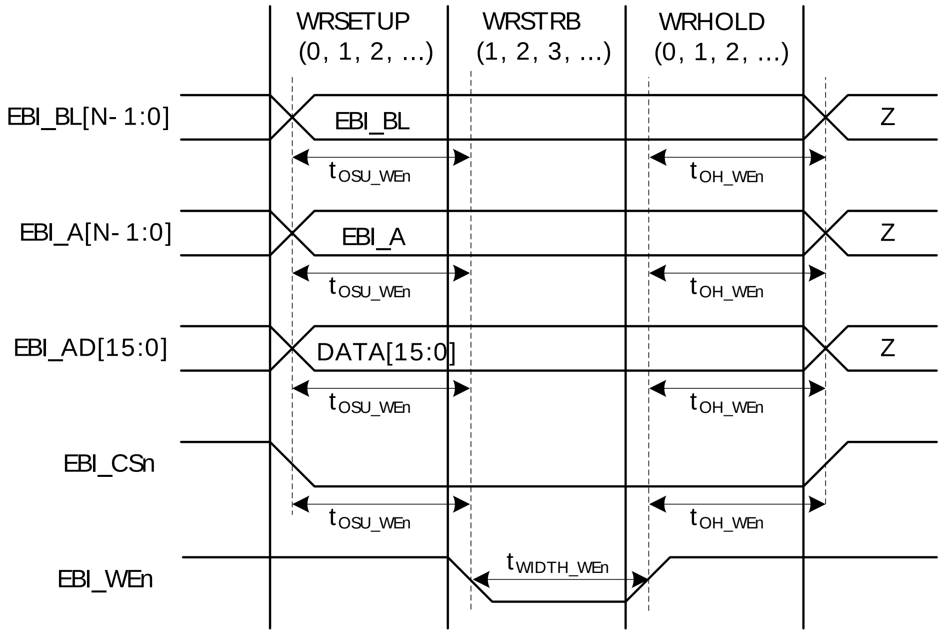
The $V_{DD}$ trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

***VCMP Trigger Level as a Function of Level Setting***

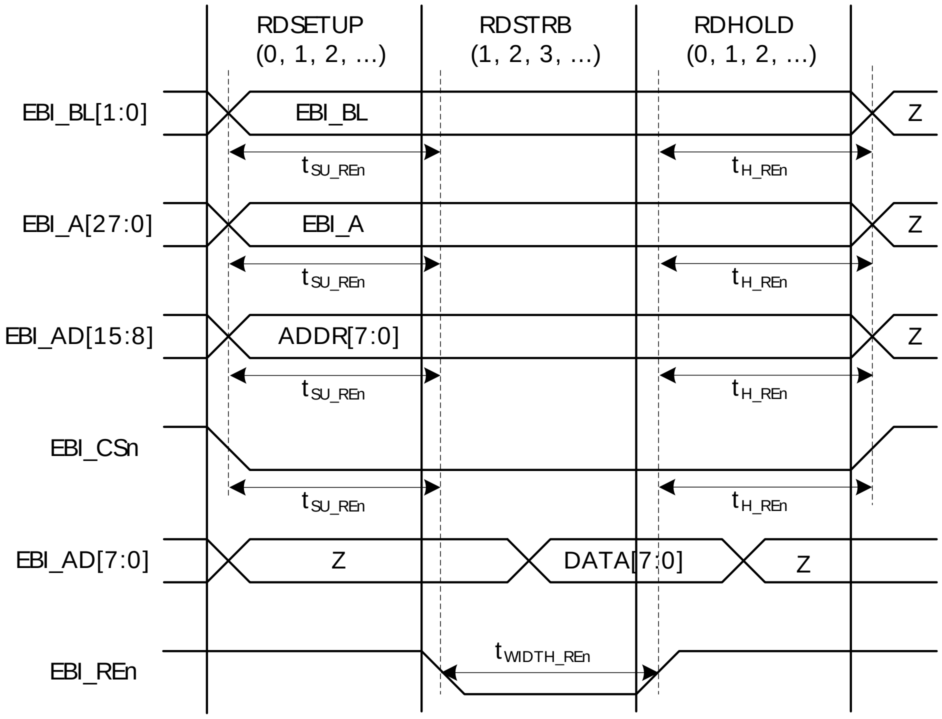
$$V_{DD\ Trigger\ Level}=1.667V+0.034\times TRIGLEVEL \tag{3.2}$$

## 3.15 EBI

*Figure 3.31. EBI Write Enable Timing*



### Figure 3.33. EBI Read Enable Related Output Timing



### Table 3.21. EBI Read Enable Related Output Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OH\_REn}$ [1 2 3 4] | Output hold time, from trailing EBI_REn/ EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | -10.00 + (RDHOLD * $t_{HFCORECLK}$) | | | ns |
| $t_{OSU\_REn}$ [1 2 3 4 5] | Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn/EBI_NANDREn edge | -10.00 + (RDSETUP * $t_{HFCORECLK}$) | | | ns |
| $t_{WIDTH\_REn}$ [1 2 3 4 5 6] | EBI_REn pulse width | -9.00 + ((RDSTRB+1) * $t_{HFCORECLK}$) | | | ns |

[1] Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)

[2] Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of $t_{WIDTH\_REn}$ and increases the length of $t_{OSU\_REn}$ by 1/2 * $t_{HFCLKNODIV}$.

[6] When page mode is used, RDSTRB is replaced by RDPA for page hits.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{PCNT}$ | PCNT current | PCNT idle current, clock enabled |  | 54 |  | nA |
| $I_{RTC}$ | RTC current | RTC idle current, clock enabled |  | 54 |  | nA |
| $I_{AES}$ | AES current | AES idle current, clock enabled |  | 3.2 |  | µA/ MHz |
| $I_{GPIO}$ | GPIO current | GPIO idle current, clock enabled |  | 3.7 |  | µA/ MHz |
| $I_{EBI}$ | EBI current | EBI idle current, clock enabled |  | 11.8 |  | µA/ MHz |
| $I_{PRS}$ | PRS current | PRS idle current |  | 3.5 |  | µA/ MHz |
| $I_{DMA}$ | DMA current | Clock enable |  | 11.0 |  | µA/ MHz |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 62 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| 63 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| 64 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| 65 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| 66 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| 67 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| 68 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 69 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| 70 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 71 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| 72 | PC12 | ACMP1_CH4<br>DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1<br>LES_CH12 #0 |
| 73 | PC13 | ACMP1_CH5<br>DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3<br>TIM1_CC0 #0<br>TIM1_CC2 #4<br>PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| 74 | PC14 | ACMP1_CH6<br>DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>U0_TX #3 | LES_CH14 #0 |
| 75 | PC15 | ACMP1_CH7<br>DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3<br>TIM1_CC2 #0 | US0_CLK #3<br>U0_RX #3 | LES_CH15 #0<br>DBG_SWO #1 |
| 76 | PF0 | | | TIM0_CC0 #5<br>LETIM0_OUT0 #2 | US1_CLK #2<br>I2C0_SDA #5<br>LEU0_TX #3 | DBG_SWCLK #0/1/2/3 |
| 77 | PF1 | | | TIM0_CC1 #5<br>LETIM0_OUT1 #2 | US1_CS #2<br>I2C0_SCL #5<br>LEU0_RX #3 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| 78 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| 79 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1<br>ETM_TD3 #1 |
| 80 | PF4 | | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| 81 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| 87 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |
| 88 | PD9 | | EBI_CS0 #0/1/2 | | | |
| 89 | PD10 | | EBI_CS1 #0/1/2 | | | |
| 90 | PD11 | | EBI_CS2 #0/1/2 | | | |
| 91 | PD12 | | EBI_CS3 #0/1/2 | | | |
| 92 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |

# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

*Figure 5.1. LQFP100 PCB Land Pattern*

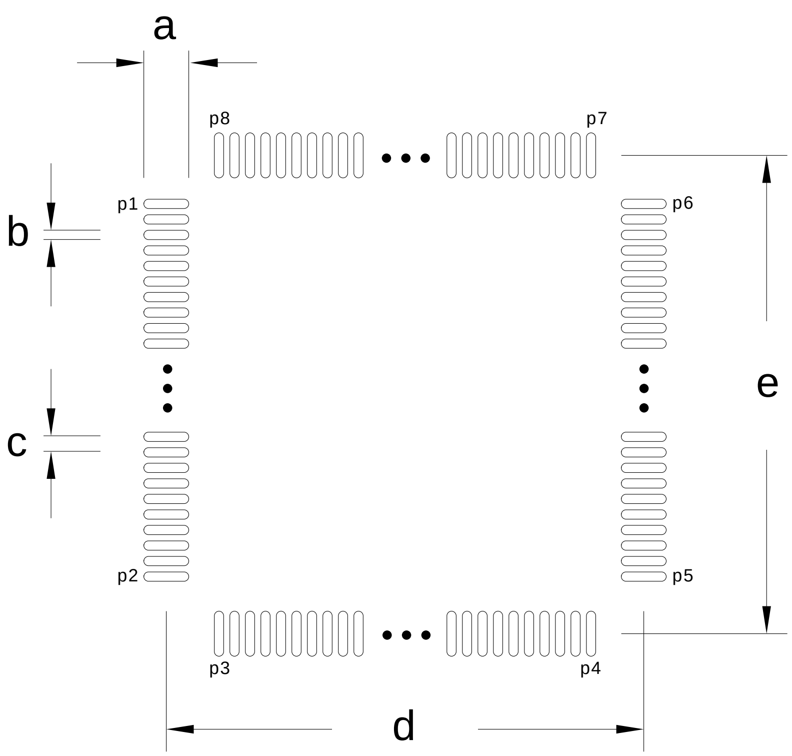


*Table 5.1. QFP100 PCB Land Pattern Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) | Symbol | Pin number | Symbol | Pin number |
|---|---|---|---|---|---|
| a | 1.45 | P1 | 1 | P6 | 75 |
| b | 0.30 | P2 | 25 | P7 | 76 |
| c | 0.50 | P3 | 26 | P8 | 100 |
| d | 15.40 | P4 | 50 | - | - |
| e | 15.40 | P5 | 51 | - | - |

*Figure 5.3. LQFP100 PCB Stencil Design*

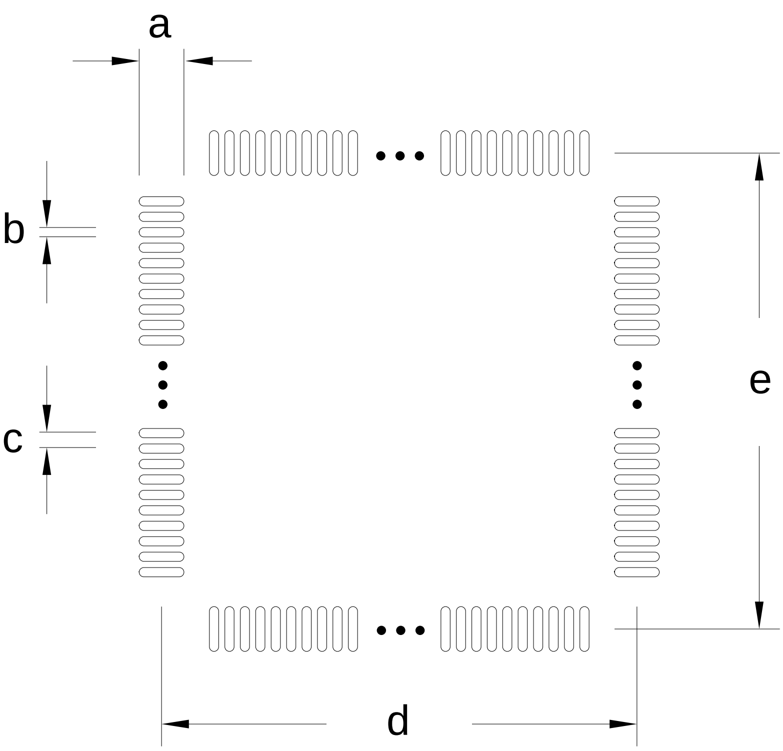


*Table 5.3. QFP100 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 1.35 |
| b | 0.20 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 64) .

## 5.2 Soldering Information

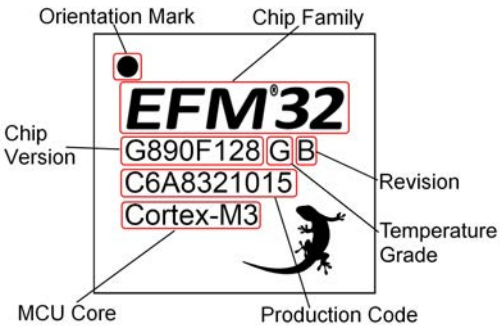
The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

# 6 Chip Marking, Revision and Errata

## 6.1 Chip Marking

In the illustration below package fields and position are shown.

***Figure 6.1. Example Chip Marking (top view)***



## 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 69) .

## 6.3 Errata

Please see the errata document for EFM32GG280 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

Added new alternative locations for EBI and SWO.

Corrected slew rate data for Opamps.

## 7.11 Revision 0.90

February 4th, 2011

Initial preliminary release.