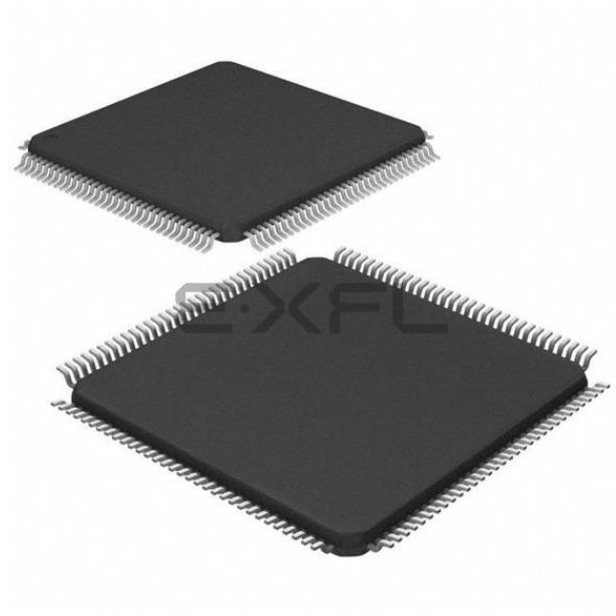

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	MIPS32® M14K™
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	128KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1404-nu

MEC140x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
94	3	Reserved	Reserved		Reserved	Reserved		
94	Strap							
95		VREF_CPU	VREF_CPU		VREF_CPU	VREF_CPU		Note 6, Note 18
95								
95								
95								
95	Strap							
96	Default: 0	GPIO141	PIO	I-4	VTR	VTR/VCC	No Gate	
96	1	SMB04_DATA	PIO		VTR	VTR	High	Note 4
96	2	SMB04_DATA18	PIO		VTR	VTR	High	Note 11
96	3	Reserved	Reserved		Reserved	Reserved		
96	Strap							
97	Default: 0	GPIO142	PIO	I-4	VTR	VTR/VCC	No Gate	
97	1	SMB04_CLK	PIO		VTR	VTR	High	Note 4
97	2	SMB04_CLK18	PIO		VTR	VTR	High	Note 11
97	3	Reserved	Reserved		Reserved	Reserved		
97	Strap							
98	Default: 0	GPIO143	PIO	I-4	VTR	VTR/VCC	No Gate	Note 9
98	1	KSI0	PIO		VTR	VTR	Low	Note 15
98	2	DTR#	PIO		VTR	VTR	Reserved	
98	3	Reserved	Reserved		Reserved	Reserved		
98	Strap							
99	Default: 0	GPIO144	PIO	I-4	VTR	VTR/VCC	No Gate	
99	1	KSI1	PIO		VTR	VTR	Low	Note 15
99	2	DCD#	PIO		VTR	VTR	High	
99	3	Reserved	Reserved		Reserved	Reserved		
99	Strap							
100		VSS	PWR		PWR	PWR		
100								
100								
100								
100	Strap							
101	Default: 0	GPIO145 (ICSP_CLOCK)	PIO	I-4	VTR	VTR/VCC	No Gate	Note 2
101	1	Reserved	PIO		Reserved	Reserved		
101	2	Reserved	Reserved		Reserved	Reserved		
101	3	Reserved	Reserved		Reserved	Reserved		
101	Strap							
102	Default: 0	GPIO146 (ICSP_DATA)	PIO	I-4	VTR	VTR/VCC	No Gate	Note 2
102	1	Reserved	PIO		Reserved	Reserved		
102	2	Reserved	Reserved		Reserved	Reserved		

4.0 LPC INTERFACE

4.1 Introduction

The Intel® Low Pin Count (LPC) Interface is the LPC Interface used by the system host to configure the chip and communicate with the logical devices implemented in the design through a series of read/write registers. Register access is accomplished through the LPC transfer cycles defined in Table 4-5, "LPC Cycle Types Supported".

The Logical Devices implemented in the design are identified in Table 4-15, “I/O Base Address Registers,” on page 117. The Base Address Registers allow any logical device’s runtime registers to be relocated in LPC I/O space. All chip configuration registers for the device are accessed indirectly through the LPC I/O Configuration Port (see Section 4.8.3, "Configuration Port," on page 105).

4.2 References

- Intel® Low Pin Count (LPC) Interface Specification, v1.1
- PCI Local Bus Specification, Rev. 2.2
- Serial IRQ Specification for PCI Systems Version 6.0.
- PCI Mobile Design Guide Rev 1.0

4.3 Terminology

This table defines specialized terms localized to this feature.

TABLE 4-1: TERMINOLOGY

Term	Definition
System Host	Refers to the external CPU that communicates with this device via the LPC Interface.
Logical Devices	Logical Devices are LPC accessible features that are allocated a Base Address and range in LPC I/O address space
Runtime Register	Runtime Registers are register that are directly I/O accessible by the System Host via the LPC interface. These registers are defined in Section 4.10, "Runtime Registers," on page 120.
Configuration Registers	Registers that are only accessible in CONFIG_MODE. These registers are defined in Section 4.9, "LPC Configuration Registers," on page 112.
EC_Only Registers	Registers that are not accessible by the System Host. They are only accessible by an internal embedded controller. These registers are defined in Section 4.11, "EC-Only Registers," on page 121.

4.9.5 SRAM MEMORY BAR CONFIGURATION

Offset	A4h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	RESERVED	RES	-	-
7	VALID If this bit is 1, the SRAM Memory BAR is valid and will participate in LPC matches. If it is 0 this SRAM Memory BAR is ignored.	R/W	0h	nSIO_RESET
6:1	RESERVED	RES	-	-

4.9.6 DEVICE MEMORY BASE ADDRESS REGISTERS (DEV_MEM_BARS)

Some Logical Devices have a Memory Base Address Register. These Device Memory BARs are located in blocks of

Configuration Registers in Logical Device 0Ch, in the AHB address range 000F_33C0h through 000F_33FFh. The following table defines the generic format used for all of these registers.

Each DEV_MEM_BAR is 48 bits wide. The format of each Device Memory BAR is summarized in Section 4.9.6.1, "Device Memory Base Address Register Format". An LPC memory request is translated by the Device Memory BAR into an 8-bit read or write transaction on the AHB bus. The 32-bit LPC memory address is translated into a 32-bit AHB address.

4.9.6.1 Device Memory Base Address Register Format

Offset	See Table 4-16, “Device Memory Base Address Registers,” on page 119			
Bits	**Description**	**Type**	**Default**	**Reset Event**
47:16	LPC Host Address These 16 bits are used to match LPC I/O addresses	R/W	See TABLE 4-16:	nSIO_RESET
15	VALID If this bit is 1, the BAR is valid and will participate in LPC matches. If it is 0 this BAR is ignored	R/W	See TABLE 4-16:	nSIO_RESET
14	DEVICE (device) This bit combined with FRAME constitute the Logical Device Number. DEVICE identifies the physical location of the logical device. This bit should always be set to 0.	R	See TABLE 4-16:	nSIO_RESET

TABLE 10-4: JTVIC REGISTER SUMMARY (CONTINUED)

Offset	Register Name
D0h	GIRQ21 Source Register
D4h	GIRQ21 Enable Set Register
D8h	GIRQ21 Enable Clear Register
DCh	GIRQ21 Result Register
E0h	GIRQ22 Source Register
E4h	GIRQ22 Enable Set Register
E8h	GIRQ22 Enable Clear Register
ECh	GIRQ22 Result Register
F0h	GIRQ23 Source Register
F4h	GIRQ23 Enable Set Register
F8h	GIRQ23 Enable Clear Register
FCh	GIRQ23 Result Register
100h	GIRQ24 Source Register
104h	GIRQ24 Enable Set Register
108h	GIRQ24 Enable Clear Register
10Ch	GIRQ24 Result Register
110h	GIRQ25 Source Register
114h	GIRQ25 Enable Set Register
118h	GIRQ25 Enable Clear Register
11Ch	GIRQ25 Result Register
120h	GIRQ26 Source Register
124h	GIRQ26 Enable Set Register
128h	GIRQ26 Enable Clear Register
12Ch	GIRQ26 Result Register
Aggregator Control Registers	
200h	GIRQ8 Aggregator Control Register
204h	GIRQ9 Aggregator Control Register
208h	GIRQ10 Aggregator Control Register
20Ch	GIRQ11 Aggregator Control Register
210h	GIRQ12 Aggregator Control Register
214h	GIRQ13Aggregator Control Register
218h	GIRQ14 Aggregator Control Register

TABLE 22-2: REGISTER SUMMARY (CONTINUED)

Offset	Register Name
3F8h	GPIO Lock 1
3FCh	GPIO Lock 0
500h	Reserved
504h - 51Ch	GPIO001-GPIO007 Pin Control Register 2
520h - 53Ch	GPIO010-GPIO017 Pin Control Register 2
540h - 55Ch	GPIO020-GPIO027 Pin Control Register 2
560h - 578h	GPIO030-GPIO036 Pin Control Register 2 (see Note 22-5 for limitations)
580h - 59Ch	GPIO040-GPIO047 Pin Control Register 2 (see Note 22-5 for limitations)
5A0h - 5BCh	GPIO050-GPIO057 Pin Control Register 2
5C0h - 5CCh	GPIO060-GPIO063 Pin Control Register 2 (see Note 22-5 for limitations)
5D0h	Reserved (GPIO064 not implemented - see Note 22-4)
5D4h - 5D8h	GPIO065-GPIO066 Pin Control Register 2
5DCh	Reserved (GPIO067 not implemented - see Note 22-4)
5E0h - 5F8h	Reserved (GPIO070-GPIO076 not implemented)
5E0h - 5FCh	GPIO100-GPIO107 Pin Control Register 2
600h - 61Ch	GPIO110-GPIO117 Pin Control Register 2
620h - 63Ch	GPIO120-GPIO127 Pin Control Register 2
640h - 658h	GPIO130-GPIO136 Pin Control Register 2
660h - 67Ch	GPIO140-GPIO147 Pin Control Register 2
680h - 69Ch	GPIO150-GPIO157 Pin Control Register 2
6A0h - 6B8h	GPIO160-GPIO166 Pin Control Register 2

Note 22-3 The GPIO input and output registers are LPC I/O accessible via Region 0 of the EMI block. This access is defined in the EMI Protocols chapter of the firmware specification.

Note 22-4 There is no Pin Control Register 2 for GPIO064 and GPIO067, which are PCI_PIO buffer type pins. The drive strength and slew rate are not configurable on these pins.

Note 22-5 The drive strength and slew rate are not configurable for the LPC functions on GPIO034, GPIO061, GPIO063, and GPIO40 - GPIO044 since they are controlled by the PCI_PIO type buffers.

Offset	28Ch (Note 22-3)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:8	GPIO[157:150] Output	R/W	00h	nSYSRST
7:0	GPIO[147:140] Output	R/W	00h	nSYSRST

22.6.3 GPIO INPUT REGISTERS

The GPIO Input Registers can always be used to read the state of a pin, even when the pin is in an output mode and/or when a signal function other than the GPIO signal function is selected; i.e., the Pin Control Register Mux Control bits are not equal to '00.'

The MSbit of the Input GPIO registers have been implemented as a read/write scratch pad bit to support processor specific instructions.

Note: Bits associated with GPIOs that are not implemented are shown as Reserved.

22.6.3.1 Input GPIO[000:036]

Offset	300h (Note 22-3)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Scratchpad Bit	R/W	0b	nSYSRST
30:24	GPIO[036:030] Input	R	00h	nSYSRST
23:16	GPIO[027:020] Input	R	00h	nSYSRST
15:8	GPIO[017:010] Input	R	00h	nSYSRST
7:0	GPIO[007:000] Input	R	00h	nSYSRST

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
5	BUSY This is a status signal. 1=The DMA Channel is busy (FSM is not IDLE) 0=The DMA Channel is not busy (FSM is IDLE)	RO	0h	DMA_RESET
4:3	STATUS This is a status signal. The status decode is listed in priority order with the highest priority first. 3: Error detected by the DMA 2: The DMA Channel is externally done, in that the Device has terminated the transfer over the **Hardware Flow Control** through the Port **dma_term** 1: The DMA Channel is locally done, in that **Memory Start Address** equals **Memory End Address** 0: DMA Channel Control:Run is Disabled (0x0) **Note:** This functionality has been replaced by the Interrupt field, and as such should never be used. The field will not flag back appropriately timed status, and if used may cause the firmware to become out-of-sync with the hardware. This field has multiple non-exclusive statuses, but may only display a single status. As such, multiple statuses may be TRUE, but this will appear as though only a single status has been triggered.	R	0h	DMA_RESET
2	DONE This is a status signal. It is only valid while **DMA Channel Control:Run** is Enabled. This is the inverse of the **DMA Channel Control:Busy** field, except this is qualified with the **DMA Channel Control:Run** field. 1=Channel is done 0=Channel is not done or it is OFF	RO	0h	DMA_RESET
1	REQUEST This is a status field. 1: There is a transfer request from the Master Device 0: There is no transfer request from the Master Device	RO	0h	DMA_RESET
0	RUN This is a control field. **Note:** This bit only applies to **Hardware Flow Control** mode. Do not use this bit in conjunction with the **Firmware Flow Control.** 1: This channel is enabled and will service transfer requests 0=This channel is disabled. All transfer requests are ignored	RW	0h	DMA_RESET

24.11.11 DMA CHANNEL N CRC TEST REGISTER

Offset	2Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	Reserved	R	-	-

26.0 TACHOMETER

26.1 Introduction

This block monitors tachometer output signals (or locked rotor signals) from various types of fans, and determines their speed.

26.2 References

No references have been cited for this feature.

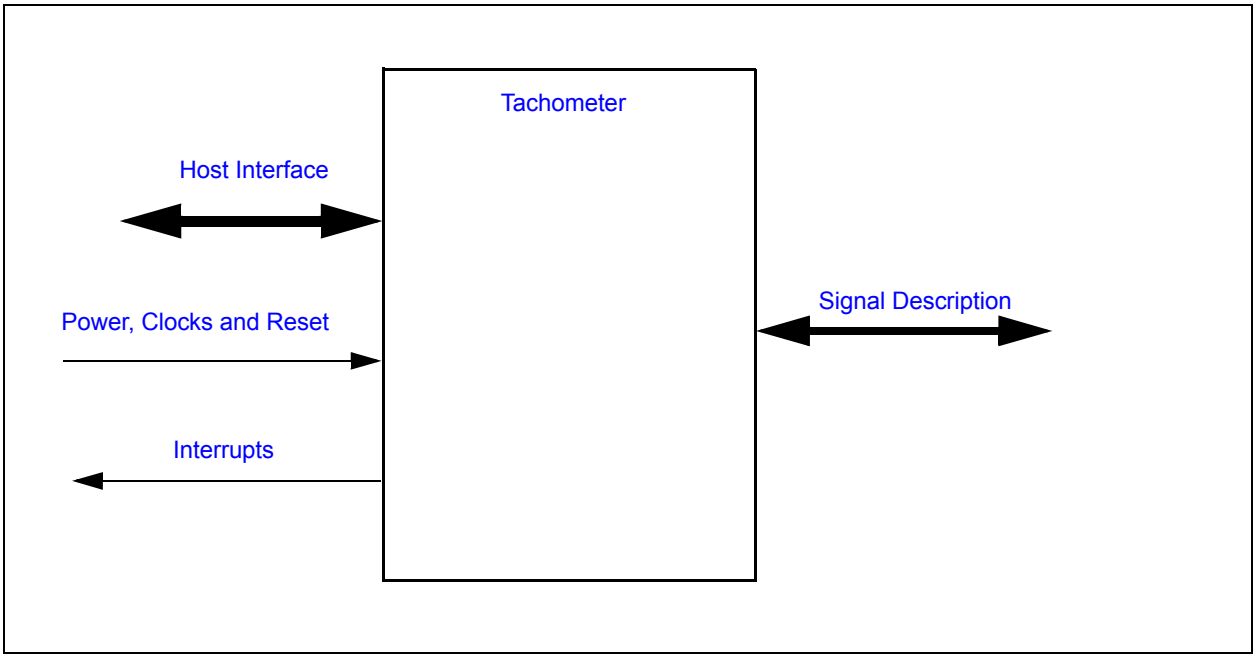
26.3 Terminology

There is no terminology defined for this section.

26.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 26-1: I/O DIAGRAM OF BLOCK



26.5 Signal Description

TABLE 26-1: SIGNAL DESCRIPTION

Name	Direction	Description
TACHx	Input	Tachometer input signal.

Note: 'x' represents the instance number (i.e., TACH0, TACH1, etc.). If there is only one tachometer input this may be omitted from the pin signal name.

28.4 Host Interface

The blinking/breathing PWM block is accessed by a controller over the standard register interface.

28.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

28.5.1 POWER DOMAINS

Name	Description
VTR	Main power. The source of main power for the device is system dependent.

28.5.2 CLOCK INPUTS

Name	Description
5Hz_Clk	32.768 KHz clock
48 MHz Ring Oscillator	48 MHz clock

28.5.3 RESETS

Name	Description
nSYSRST	Block reset

28.6 Interrupts

Each PWM can generate an interrupt. The interrupt is asserted for one 48 MHz clock period whenever the PWM WDT times out. The PWM WDT is described in Section 28.8.3.1, "PWM WDT," on page 382.

Source	Description
PWM_WDT	PWM watchdog time out

29.12 PS/2 Port Physical Layer Byte Transmission Protocol

The PS/2 physical layer transfers a byte of data via an eleven bit serial stream as shown in TABLE 29-2:. A logic 1 is sent at an active high level. Data sent from a Keyboard or mouse device to the host is read on the falling edge of the clock signal. The Keyboard or mouse device always generates the clock signal. The Host may inhibit communication by pulling the Clock line low. The Clock line must be continuously high for at least 50 microseconds before the Keyboard or mouse device can begin to transmit its data. See Table 29-3, "PS/2 Port Physical Layer Bus States".

TABLE 29-2: PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

Bit	Function
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd parity)
11	Stop Bit (always 1)

FIGURE 29-3: PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

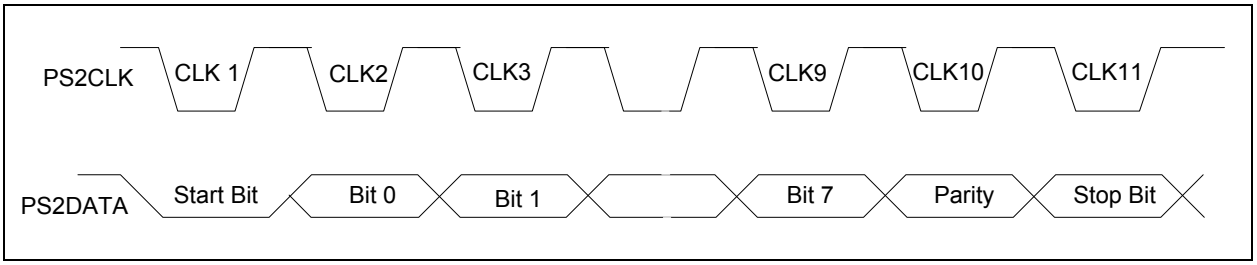


TABLE 29-3: PS/2 PORT PHYSICAL LAYER BUS STATES

Data	Clock	State
high	high	Idle
high	low	Communication Inhibited
low	low	Request to Send

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
5	KSO_ALL 0 = When key scan is enabled, KSO output controlled by the KSO_SELECT field. 1 = All KSO pins are active and the KSO_SELECT field is a don't care. **Note:** The active state is determined by the KSO_INVERT bit as is shown in Table 30-5, "Keyboard Scan Out Control Summary"	R/W	0b	nSYSRST
4:0	KSO_SELECT This field determines which KSO line(s) are active. 0_0000b = KSO00 Selected 0_0001b = KSO01 Selected . . . 1_0001b = KSO17 Selected 1_0010b - 1_1111b = All KSO pins selected **Note:** The full decode table is illustrated in Table 30-4, "KSO Select Decode" **Note:** The active state is determined by the KSO_INVERT bit as is shown in Table 30-5, "Keyboard Scan Out Control Summary"	R/W	0h	nSYSRST

TABLE 30-4: KSO SELECT DECODE

KSO Select [4:0]	KSO Selected
00h	KSO00
01h	KSO01
02h	KSO02
03h	KSO03
04h	KSO04
05h	KSO05
06h	KSO06
07h	KSO07
08h	KSO08
09h	KSO09
0Ah	KSO10

31.11.2 BC-LINK ADDRESS REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	ADDRESS Address in the Companion for the BC-Link transaction.	R/W	0h	nSYSRST

31.11.3 BC-LINK DATA REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	DATA As described in Section 31.10.1, "BC-Link Master READ Operation" and Section 31.10.2, "BC-Link Master WRITE Operation", this register hold data used in a BC-Link transaction.	R/W	0h	nSYSRST

31.11.4 BC-LINK CLOCK SELECT REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	DIVIDER The BC Clock is set to the Master Clock divided by this field, or 48MHz/ (Divider +1). The clock divider bits can only can be changed when the BC Bus is in soft RESET (when either the Reset bit is set by software or when the BUSY bit is set by the interface). Settings for DIVIDER are shown in Table 31-5, "Frequency Settings".	R/W	4h	nSYSRST

37.9.5 VCI POLARITY REGISTER

Offset	14h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:2	Reserved	R	-	-
1:0	VCI_IN_POL These bits determine the polarity of the VCI_IN input signals: For each bit in the field: 1=Active High. The value on the pins is inverted before use 0=Active Low (default)	RW	0	VBAT_POR

37.9.6 VCI POSEDGE DETECT REGISTER

Offset	18h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:1	Reserved	R	-	-
1:0	VCI_IN_POS These bits record a low to high transition on the VCI_IN# pins. A “1” indicates a transition occurred. For each bit in the field: 1=Positive Edge Detected 0=No edge detected	RWC	0	VBAT_POR

37.9.7 VCI NEGEDGE DETECT REGISTER

Offset	1Ch			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:2	Reserved	R	-	-
1:0	VCI_IN_NEG These bits record a high to low transition on the VCI_IN# pins. A “1” indicates a transition occurred. For each bit in the field: 1=Negative Edge Detected 0=No edge detected	RWC	0	VBAT_POR

38.8 Interrupts

Source	Description
ADC_Single_Int	Interrupt signal from ADC controller to EC for Single-Sample ADC conversion.
ADC_Repeat_Int	Interrupt signal from ADC controller to EC for Repeated ADC conversion.

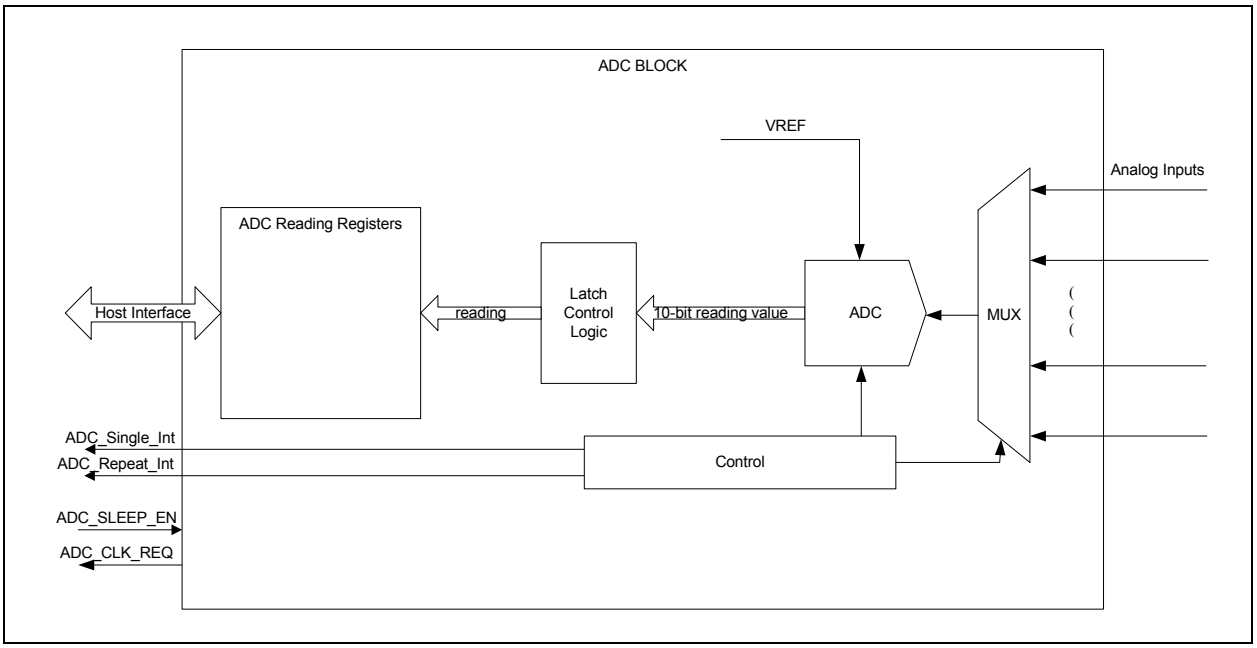
38.9 Low Power Modes

The ADC may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

The ADC is designed to conserve power when it is either sleeping or disabled. It is disabled via the Activate Bit and sleeps when the ADC_SLEEP_EN signal is asserted. The sleeping state only controls clocking in the ADC and does not power down the analog circuitry. For lowest power consumption, the ADC Activate bit must be set to '0.'

38.10 Description

FIGURE 38-2: ADC BLOCK DIAGRAM



The MEC140x/1x features successive approximation Analog to Digital Converter with up to sixteen channels. The ADC architecture features excellent linearity and converts analog signals to 10 bit words. Conversion takes less than 12 microseconds per 10-bit word. The sixteen channels are implemented with a single high speed ADC fed by a sixteen input analog multiplexer. The multiplexer cycles through the sixteen voltage channels, starting with the lowest-numbered channel and proceeding to the highest-number channel, selecting only those channels that are programmed to be active.

The input range on the voltage channels spans from 0V to the external voltage reference. With an external voltage reference of 3.0V, this provides resolutions of 2.9mV. The accuracy of any voltage reading depends on the accuracy and stability of the voltage reference input.

Note: The ADC pins are 3.3V tolerant.

42.2 Operational Specifications

42.2.1 POWER SUPPLY OPERATIONAL CHARACTERISTICS

TABLE 42-3: POWER SUPPLY OPERATING CONDITIONS

Symbol	Parameter	MIN	TYP	MAX	Units
VBAT	Battery Backup Power Supply	2.0	3.0	3.6	V
VTR	Suspend Power Supply	3.135	3.3	3.465	V
VTR_33_18	3.3V Power Supply	3.135	3.3	3.465	V
	1.8V Power Supply	1.71	1.80	1.89	V

Note: The specification for the VTR & VTR_33_18 supplies are +/- 5%.

42.2.2 AC ELECTRICAL SPECIFICATIONS

The AC Electrical Specifications for the clock input time are defined in Section 43.2, "Clocking AC Timing Characteristics," on page 504. The clock rise and fall times use the standard input thresholds of 0.8V and 2.0V unless otherwise specified and the capacitive values listed in Section 42.2.2, "AC Electrical Specifications," on page 490.

42.2.3 CAPACITIVE LOADING SPECIFICATIONS

The following table defines the maximum capacitive load validated for the buffer characteristics listed in Table 42-5, “DC Electrical Characteristics,” on page 491.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{cc} = 3.3 VDC

Note: All output pins, except pin under test, tied to AC ground.

TABLE 42-4: MAXIMUM CAPACITIVE LOADING

Parameter	Symbol	Limits			Unit	Notes
		MIN	TYP	MAX		
Input Capacitance of PCI_I and PCI_IO pins	C_{IN}			Note 42-2	pF	
Input Capacitance of PCI_CLK pin	C_{IN}			Note 42-2	pF	
Output Load Capacitance supported by PCI_IO, PCI_O, and PCI_OD	C_{OUT}			Note 42-2	pF	
SUSCLK Input Capacitance	C_{IN}			10	pF	
Input Capacitance of PECI_I and PECI_IO	C_{IN}			10	pF	
Output Load Capacitance supported by PECI_IO and OD_PH	C_{OUT}			10	pF	

43.11 Blinking/Breathing PWM Timing

FIGURE 43-9: BLINKING/BREATHING PWM OUTPUT TIMING

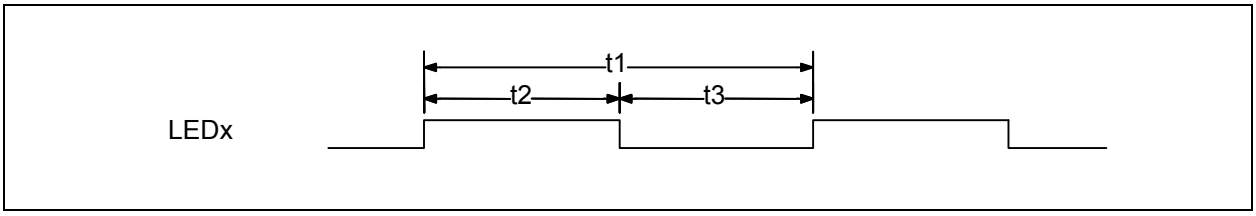


TABLE 43-11: BLINKING/BREATHING PWM TIMING PARAMETERS, BLINKING MODE

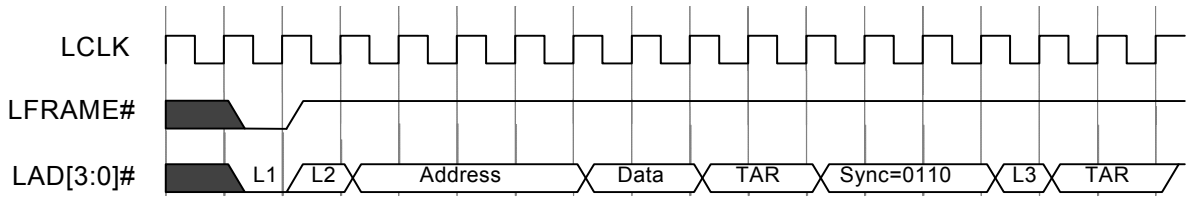
Name	Description	MIN	TYP	MAX	Units
t1	Period	7.8ms		32sec	
t_f	Frequency	0.03125		128	Hz
t2	High Time	0		16	sec
t3	Low Time	0		16	sec
t_d	Duty cycle	0		100	%

TABLE 43-12: BLINKING/BREATHING PWM TIMING PARAMETERS, GENERAL PURPOSE

Name	Description	MIN	TYP	MAX	Units
t1	Period	5.3us		21.8ms	
t_f	Frequency	45.8Hz		187.5kHz	
t2	High Time	0		10.9	ms
t3	Low Time	0		10.9	ms
t_d	Duty cycle	0		100	%

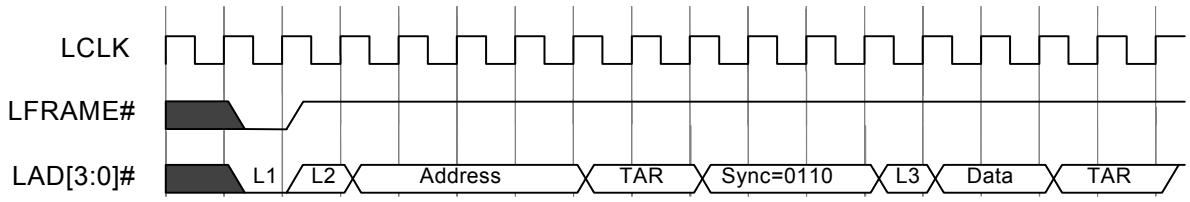
43.17.5 LPC I/O TIMING

FIGURE 43-18: I/O WRITE



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 43-19: I/O READ



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

43.17.6 SERIAL IRQ TIMING

FIGURE 43-20: SETUP AND HOLD TIME

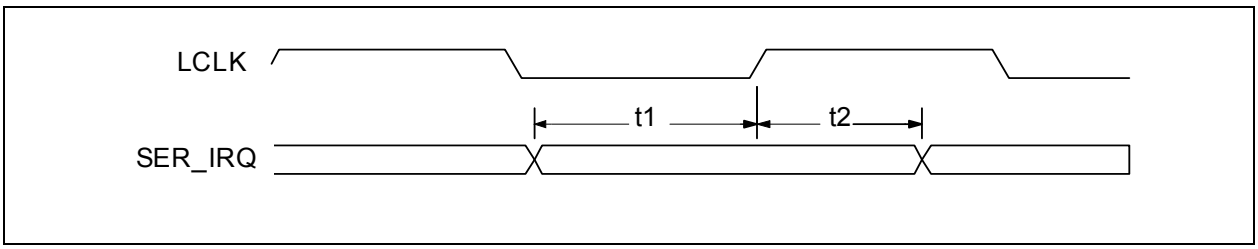


TABLE 43-21: SETUP AND HOLD TIME

Name	Description	MIN	TYP	MAX	Units
t1	SER_IRQ Setup Time to LCLK Rising	7			nsec
t2	SER_IRQ Hold Time to LCLK Rising	0			

43.17.7 nEC_SCI TIMING

nEC_SCI pin has the same minimum timing requirements as GPIO signals. See Section 43.5, "GPIO Timings," on page 507.

43.19 PECI Interface

Name	Description	MIN	MAX	Units	Notes
t_{BIT}	Bit time (overall time evident on PECI pin) Bit time driven by an originator	0.495 0.495	500 250	µsec µsec	43-1
$t_{BIT,jitter}$	Bit time jitter between adjacent bits in a PECI message header or data bytes after timing has been negotiated	-	-	%	
$t_{BIT,drift}$	Change in bit time across a PECI address or PECI message bits as driven by the originator. This limit only applies across t_{BIT-A} bit drift and t_{BIT-M} drift.	-	-	%	
t_{H1}	High level time for logic 1	0.6	0.8	t_{BIT}	43-2
t_{H0}	High level time for logic 0	0.2	0.4	t_{BIT}	
t_{PECIR}	Rise time (measured from V_{OL} to $V_{IH,min}$, $Vtt_{(nom)}$–5%)	-	30 + (5 x #nodes)	ns	43-3
t_{PECIF}	Fall time (measured from V_{OH} to $V_{IL,max}$, $Vtt_{(nom)}$+5%)	-	(30 x #nodes)	ns	43-3

Note 43-1 The originator must drive a more restrictive time to allow for quantized sampling errors by a client yet still attain the minimum time less than 500 µsec. t_{BIT} limits apply equally to t_{BIT-A} and t_{BIT-M} . The MEC140x/1x is designed to support 2 MHz, or a 500ns bit time. See the PECI 3.0 specification from Intel Corp. for further details.

Note 43-2 The minimum and maximum bit times are relative to t_{BIT} defined in the Timing Negotiation pulse. See the PECI 3.0 specification from Intel Corp. for further details.

Note 43-3 “#nodes” is the number of nodes on the PECI bus; host and client nodes are counted as one each. Extended trace lengths may appear as extra nodes. Refer also to Table 25-2, "PECI Routing Guidelines". See the PECI 3.0 specification from Intel Corp. for further details.

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