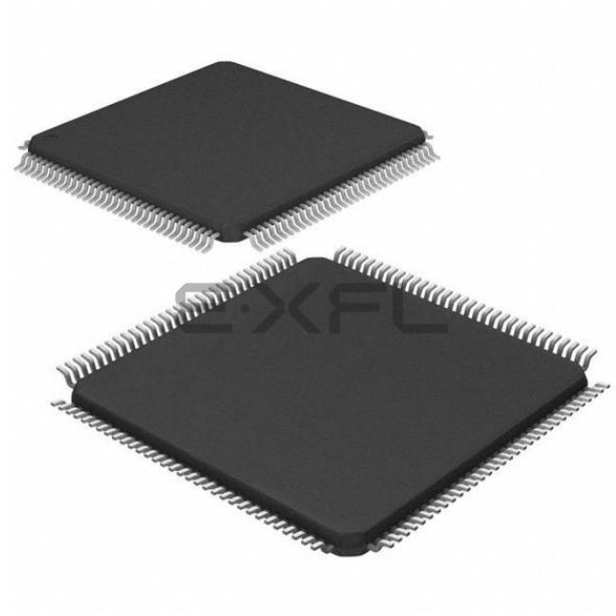

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Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	MIPS32® M14K™
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	160KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1406-nu

1.0 GENERAL DESCRIPTION

The MEC140x/1x is a family of keyboard and embedded controller designs customized for notebooks and tablet platforms. The MEC140x/1x family is a highly-configurable, mixed signal, advanced I/O controller architecture. Every device in the family incorporates a 32-bit MIPS32 M14K Microcontroller core with a closely-coupled SRAM for code and data. A secure boot-loader is used to download the custom firmware image from the system's shared SPI Flash device, thereby allowing system designers to customize the device's behavior.

The MEC140x/1x products may be configured to communicate with the system host through one of three host interfaces: Intel Low Pin Count (LPC), eSPI, or I2C. Note that this functionality is product dependent. To see which features apply to a specific part in the family see Products on page 3. The document defines the features for all devices in the family.

The MEC140x/1x products are designed to operate as either a stand-alone I/O device or as an EC Base Component of a split-architecture Advanced I/O Controller system which uses BC-Link communication protocol to access up to two BC bus companion components. The BC-Link protocol is peer-to-peer providing communication between the MEC140x/1x embedded controller and registers located in a companion device.

The MEC140x/1x is directly powered by a minimum of two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on' and system power management functions. In addition, this family of products has the option to connect the VTR_33_18 power pin to either a 3.3V VTR power supply or a 1.8V power supply. This option may only be used with the eSPI Host Interface or the I2C Host Interface. In systems using the I2C Host Interface, ten GPIOs are powered by VTR_33_18, thereby allowing them to operate at either 3.3V or 1.8V. All the devices are equipped with a Power Management Interface that supports low-power states and are capable of operating in a Connected Standby system.

The MEC140x/1x family of devices offer a software development system interface that includes a Trace FIFO Debug port, a host accessible serial debug port with a 16C550A register interface, a Port 80 BIOS Debug Port, and an In-circuit Serial Programming (ICSP) interface.

1.1 Boot ROM

Following the release of the EC_PROC_RESET# signal, the processor will start executing code in the Boot ROM. The Boot ROM executes the SPI Flash Loader, which downloads User Code from an external SPI Flash and stores it in the internal Code RAM. Upon completion, the Boot ROM jumps into the User Code and starts executing.

1.2 Initialize Host Interface

By default, this device powers up all the interfaces, except the VBAT powered interfaces and select signals, to GPIO inputs. The Boot ROM is used to download code from an external flash via either the Shared Flash Interface, the eSPI flash channel or the Private Flash Interface. The downloaded code must configure the device's pins according to the platform's needs. This includes initializing the Host Interface.

Once the device is configured for operation, the downloaded code must deassert the system's RSMRST# (Resume Reset) signal. Any GPIO may be selected for the RSMRST# function. This is up to the system board designer. The only requirement is that the board designer attach an external pull-down on the GPIO pin being used for the RSMRST# function. This will ensure the RSMRST# pin is asserted low by default and does not glitch during power-up.

This family of devices has up to three Host Interface options. It may be configured as an LPC Device, an eSPI Device, or I2C device. See Products on page 3 for the features supported in each device.

On a VTR POR, all the host interface pins default to GPIO inputs.

1.2.1 CONFIGURE LPC INTERFACE

The downloaded firmware must configure the GPIO Pin Control registers for the LPC alternate function, configure the LPC Base Address Register (BAR), and activate the LPC block.

Example:

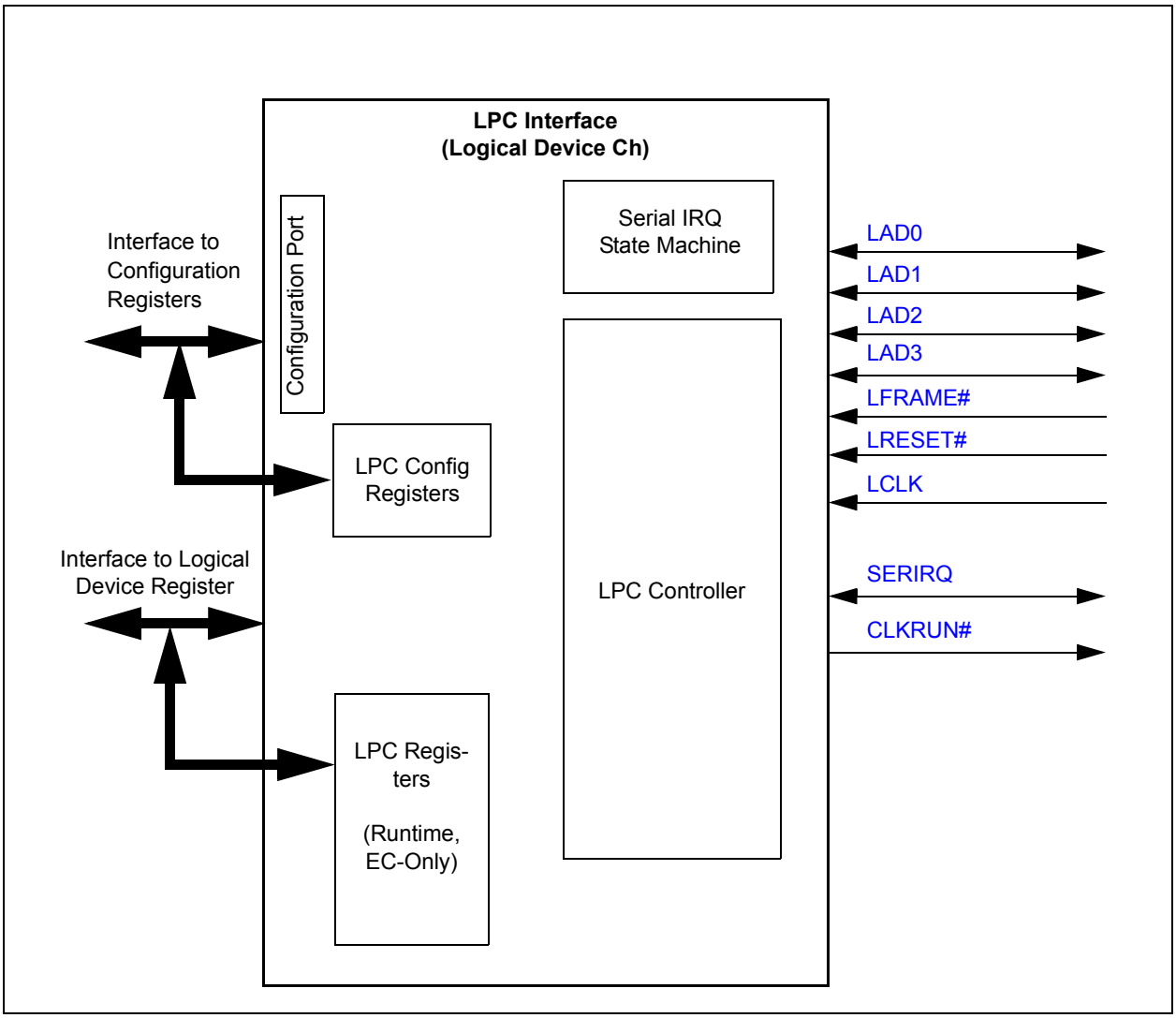
- GPIO034 Pin Control Register = 0x1000; //ALT FUNC1 – PCI_CLK
- GPIO040 Pin Control Register = 0x1000; //ALT FUNC1 – LAD0
- GPIO041 Pin Control Register = 0x1000; //ALT FUNC1 – LAD1
- GPIO042 Pin Control Register = 0x1000; //ALT FUNC1 – LAD2
- GPIO043 Pin Control Register = 0x1000; //ALT FUNC1 – LAD3
- GPIO044 Pin Control Register = 0x1000; //ALT FUNC1 – LFRAME_N

MEC141x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
56	Strap							
57	Default: 0	GPIO034	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
57	1	PCI_CLK	PCI_IO		VTR	VCC	Low	
57	2	ESPI_CLK	PIO		VTR_33_18	VTR	Low	
57	3	Reserved	Reserved		Reserved	Reserved		
57	Strap							
58	Default: 0	GPIO044	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
58	1	LFRAME#	PCI_IO		VTR	VCC	High	
58	2	ESPI_CS#	PIO		VTR_33_18	VTR	High	
58	3	Reserved	Reserved		Reserved	Reserved		
58	Strap							
59	Default: 0	GPIO040	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
59	1	LAD0	PCI_IO		VTR	VCC	High	Note 1
59	2	ESPI_IO0	PIO		VTR_33_18	VTR	Low	
59	3	Reserved	Reserved		Reserved	Reserved		
59	Strap							
60	Default: 0	GPIO041	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
60	1	LAD1	PCI_IO		VTR	VCC	High	Note 1
60	2	ESPI_IO1	PIO		VTR_33_18	VTR	Low	
60	3	Reserved	Reserved		Reserved	Reserved		
60	Strap							
61	Default: 0	GPIO042	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
61	1	LAD2	PCI_IO		VTR	VCC	High	Note 1
61	2	ESPI_IO2	PIO		VTR_33_18	VTR	Low	
61	3	Reserved	Reserved		Reserved	Reserved		
61	Strap							
62	Default: 0	GPIO043	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
62	1	LAD3	PCI_IO		VTR	VCC	High	Note 1
62	2	ESPI_IO3	PIO		VTR_33_18	VTR	Low	
62	3	Reserved	Reserved		Reserved	Reserved		
62	Strap							
63	Default: 0	GPIO067	PCI_PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
63	1	CLKRUN#	PCI_IO		VTR	VCC	Low	
63	2	Reserved	Reserved		Reserved	Reserved		
63	3	Reserved	Reserved		Reserved	Reserved		
63	Strap							
64		VSS	PWR		PWR	PWR		
64								
64								
64								
64	Strap							
65		VTR	PWR		PWR	PWR		

4.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 4-1: BLOCK DIAGRAM OF LPC INTERFACE CONTROLLER WITH CLKRUN# SUPPORT



4.4.1 SIGNAL DESCRIPTION

TABLE 4-2: SIGNAL DESCRIPTION

Name	Direction	Description
LAD0	Input/Output	Bit[0] of the LPC multiplexed command, address, and data bus.
LAD1	Input/Output	Bit[1] of the LPC multiplexed command, address, and data bus.

4.10 Runtime Registers

The runtime registers listed in Table 4-18, "Runtime Register Summary" are for a single instance of the LPC Interface. The addresses of each register listed in TABLE 4-18: are defined as a relative offset to the host “Begin Address” define in TABLE 4-2:.

TABLE 4-17: RUNTIME REGISTER ADDRESS RANGE TABLE

Instance Name	Instance Number	Host	Address Space	Begin Address
LPC Interface	0	LPC	I/O	Programmed BAR
		EC	32-bit internal address space	000F_3000h

Note 1: The Begin Address indicates where the first register can be accessed in a particular address space for a block instance.

2: The LPC Runtime registers are only accessible from the LPC interface and are used to implement the LPC Configuration Port. They are not accessible by any other Host.

TABLE 4-18: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	INDEX Register
01h	DATA Register

Note: The LPC Runtime Register space has been used to implement the INDEX and DATA registers in the Configuration Port. In CONFIG_MODE, the Configuration Port is used to access the Configuration Registers.

4.10.1 INDEX REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	INDEX The INDEX register, which is part of the Configuration Port, is used as a pointer to a Configuration Register Address. **Note:** For a description of accessing the Configuration Port see Section 4.8.3, "Configuration Port," on page 105.	R/W	0h	nSYSRST

4.10.2 DATA REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DATA The DATA register, which is part of the Configuration Port, is used to read or write data to the register currently being selected by the INDEX Register. **Note:** For a description of accessing the Configuration Port see Section 4.8.3, "Configuration Port," on page 105	R/W	0h	nSYSRST

4.11 EC-Only Registers

Note: EC-Only registers are not accessible by the LPC interface.

The registers listed in Table 4-20, "EC-Only Register Summary" are for a single instance of the LPC Interface. Their addresses are defined as a relative offset to the host base address defined in TABLE 4-19:.

The following table defines the fixed host base address for each LPC Interface instance.

TABLE 4-19: EC-ONLY REGISTER ADDRESS RANGE TABLE

INSTANCE NAME	INSTANCE NUMBER	HOST	ADDRESS SPACE	BEGIN ADDRESS
LPC Interface	0	EC	32-bit internal address space	000F_3100h

Note: The Begin Address indicates where the first register can be accessed in a particular address space for a block instance.

TABLE 4-20: EC-ONLY REGISTER SUMMARY

Offset	Register Name
04h	LPC Bus Monitor Register
08h	Host Bus Error Register
0Ch	EC SERIRQ Register
10h	EC Clock Control Register
14h	Test Register
18h	Test Register
20h	I/O BAR Inhibit Register
24h	Reserved
28h	Reserved
2Ch	Reserved
30h	LPC BAR Init Register
40h	Device Memory BAR Inhibit Register
FCh	SRAM Memory Host Configuration Register

Note 4-13 Some Test registers are read/write registers. Modifying these registers may have unwanted results.

TABLE 10-2: INTERRUPT SOURCE, ENABLE SET, ENABLE CLEAR, AND RESULT BIT ASSIGNMENTS (CONTINUED)

Aggregator IRQ	Aggregator Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description
GIRQ15	13	ACPI_EC Interface 1	IBF	No	ACPI EC Interface 1 - Input Buffer Full Event
GIRQ15	14	ACPI_EC Interface 1	OBF	No	ACPI EC Interface 1 - Output Buffer Full Event
GIRQ15	15	ACPI_EC Interface 2	IBF	No	ACPI EC Interface 2 - Input Buffer Full Event
GIRQ15	16	ACPI_EC Interface 2	OBF	No	ACPI EC Interface 2 - Output Buffer Full Event
GIRQ15	17	ACPI_EC Interface 3	IBF	No	ACPI EC Interface 3 - Input Buffer Full Event
GIRQ15	18	ACPI_EC Interface 3	OBF	No	ACPI EC Interface 3 - Output Buffer Full Event
GIRQ16	0	LPC Interface	LPC_WAKE	Yes	Wake-Only Interrupt Event - LPC Traffic Detected
GIRQ16	1	SMBus Controller 0	SMB_WAKE	Yes	Wake-Only Interrupt Event - SMBus.0 START Detected
GIRQ16	2	SMBus Controller 1	SMB_WAKE	Yes	Wake-Only Interrupt Event - SMBus.1 START Detected
GIRQ16	3	SMBus Controller 2	SMB_WAKE	Yes	Wake-Only Interrupt Event - SMBus.2 START Detected
GIRQ16	4	PS2 Device Interface 0	PS2_DAT0_WAKE	Yes	Wake-Only Interrupt Event - PS/2.0 Start Bit Detected
GIRQ16	5	PS2 Device Interface 1A	PS2_DAT1A_WAKE	Yes	Wake-Only Interrupt Event - PS/2.1A Start Bit Detected
GIRQ16	6	PS2 Device Interface 1B	PS2_DAT1B_WAKE	Yes	Wake-Only Interrupt Event - PS/2.1B Start Bit Detected
GIRQ16	7	Keyboard Matrix Scan Interface	KSC_INT_WAKE	Yes	Wake-Only Interrupt Event - Keyboard Scan Interface Active
GIRQ16	8	ICSP Debugger	DEBUG_DONE	Yes	Wake-Only Interrupt Event - Processor may use this bit to put the chip back to sleep after Debug Access.
GIRQ16	9	ESPI Interface	ESPI_WAKE	Yes	Wake-Only Interrupt Event - ESPI Traffic Detected
GIRQ17	0	ADC Controller	ADC_Single_Int	No	ADC Controller - Single-Sample ADC Conversion Event
GIRQ17	1	ADC Controller	ADC_Repeat_Int	No	ADC Controller - Repeat-Sample ADC Conversion Event
GIRQ17	2	Reserved	Reserved	-	-
GIRQ17	3	Reserved	Reserved	-	-
GIRQ17	4	PS2 Device Interface 0	PS2_ACT	No	PS/2 Device Interface 0 - Activity Interrupt Event
GIRQ17	5	PS2 Device Interface 1	PS2_ACT	No	PS/2 Device Interface 1 - Activity Interrupt Event
GIRQ17	6	Keyboard Scan Interface	KSC_INT	No	Keyboard Scan Interface - Runtime Interrupt
GIRQ17	7	UART	UART	No	UART Interrupt Event

10.12 JTVIC Registers

The registers listed in the JTVIC Register Summary table are for a single instance of the Jump Table Vectored Interrupt Controller (JTVIC). The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the EC-Only Register Base Address Table.

TABLE 10-3: EC-ONLY REGISTER BASE ADDRESS

Block Instance	Instance Number	Host	Address Space	Base Address
Interrupt Controller	0	EC	32-bit internal address space	1FFF_C000h

The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

TABLE 10-4: JTVIC REGISTER SUMMARY

Offset	Register Name
Interrupt Source, Enable Set, Enable Clear, and Result Registers	
00h	GIRQ8 Source Register
04h	GIRQ8 Enable Set Register
08h	GIRQ8 Enable Clear Register
0Ch	GIRQ8 Result Register
10h	GIRQ9 Source Register
14h	GIRQ9 Enable Set Register
18h	GIRQ9 Enable Clear Register
1Ch	GIRQ9 Result Register
20h	GIRQ10 Source Register
24h	GIRQ10 Enable Set Register
28h	GIRQ10 Enable Clear Register
2Ch	GIRQ10 Result Register
30h	GIRQ11 Source Register
34h	GIRQ11 Enable Set Register
38h	GIRQ11 Enable Clear Register
3Ch	GIRQ11 Result Register
40h	GIRQ12 Source Register
44h	GIRQ12 Enable Set Register
48h	GIRQ12 Enable Clear Register
4Ch	GIRQ12 Result Register

12.9.4 EC ADDRESS MSB REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	REGION The field specifies which of two segments in the 32-bit internal address space is to be accessed by the EC_Address[14:2] to generate accesses to the memory. 1= The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 1 Register. 0= The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 0 Register.	R/W	0h	nSYSRST
6:0	EC_ADDRESS_MSB This field defines bits[14:8] of EC_Address. Bits[1:0] of the EC_Address are always forced to 00b. The EC_Address is aligned on a DWord boundary. It is the address of the memory being accessed by EC Data Byte 0 Register, which is an offset from the programmed base address of the selected REGION.	R/W	0h	nSYSRST

12.9.5 EC DATA BYTE 0 REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_0 This is byte 0 (Least Significant Byte) of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 12.8.2, "EC Data Register".	R/W	0h	nSYSRST

12.9.6 EC DATA BYTE 1 REGISTER

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_1 This is byte 1 of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 12.8.2, "EC Data Register".	R/W	0h	nSYSRST

Note:	These bits are set/cleared by the EC directly i.e., writing ‘1’ sets the bit and writing ‘0’ clears it. These bits can also be cleared by the Host software writing a one to this bit position and by nSYSRST. Writing a 0 by the Host has no effect.

15.11.3 POWER MANAGEMENT 1 ENABLE 1 REGISTER

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Reserved	R	-	-

15.11.4 POWER MANAGEMENT 1 ENABLE 2 REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:3	Reserved	R	-	-
2	RTC_EN This bit can be read or written by the Host. It can be read by the EC.	R/W (See Note:)	00h	nSYSRST
1	SLPBTN_EN This bit can be read or written by the Host. It can be read by the EC.	R/W (See Note:)	00h	nSYSRST
0	PWRBTN_EN This bit can be read or written by the Host. It can be read by the EC.	R/W (See Note:)	00h	nSYSRST

Note:	These bits are read-only by the EC.

15.11.5 POWER MANAGEMENT 1 CONTROL 1 REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Reserved	R	0h	nSYSRST

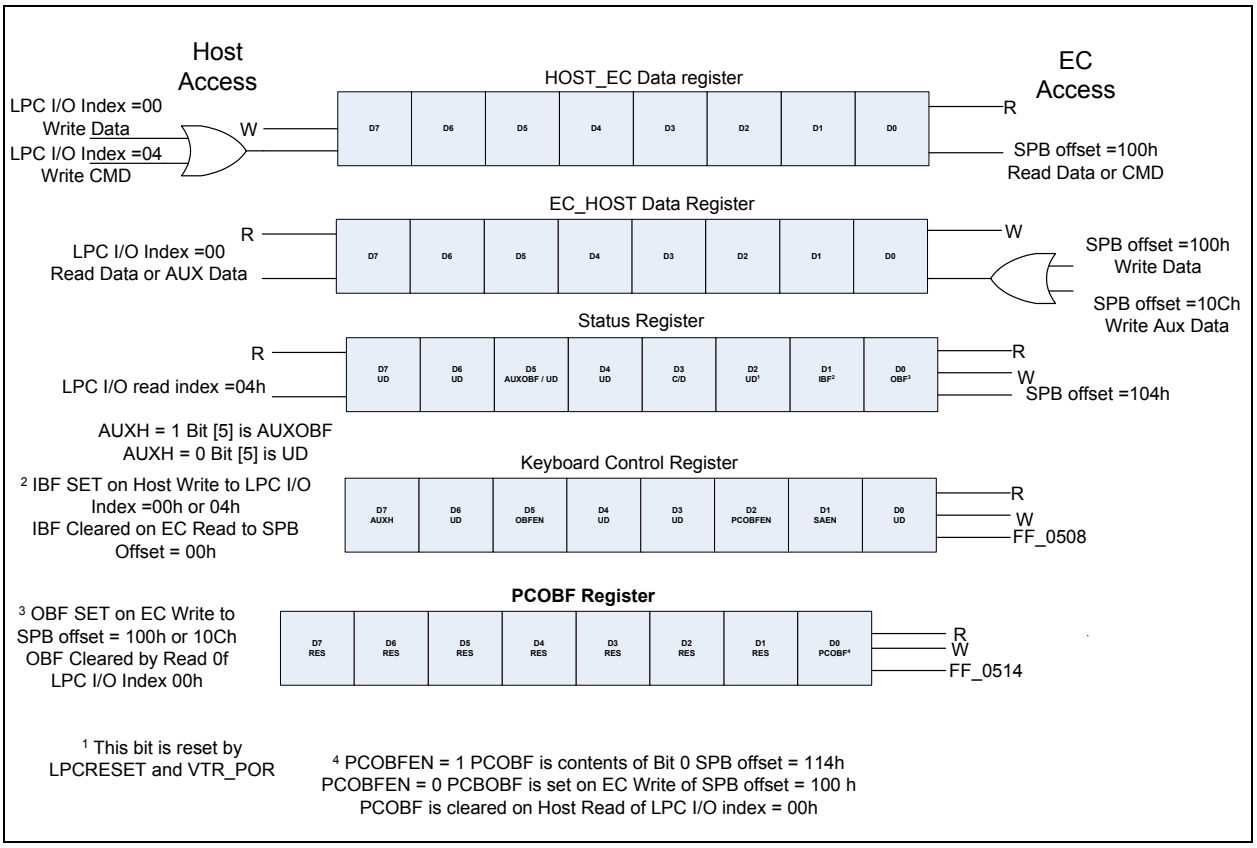
16.8 Low Power Modes

The 8042 Interface may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

16.9 Description

16.9.1 BLOCK DIAGRAM

FIGURE 16-2: BLOCK DIAGRAM OF 8042 Emulated Keyboard Controller



16.10 EC-to-Host Keyboard Communication

The EC can write to the EC_HOST Data / AUX Data Register by writing to the HOST2EC Data Register at EC-Only offset 0h or the EC AUX Data Register at EC-Only offset Ch. A write to either of these addresses automatically sets bit 0 (OBF) in the Status register. A write to the HOST2EC Data Register may also set PCOBF. A write to the EC AUX Data Register may also set AUXOBF.

16.10.1 PCOBF DESCRIPTION

If enabled by the bit OBFEN, the bit PCOBF is gated onto KIRQ. The KIRQ signal is a system interrupt which signifies that the EC has written to the EC2Host Data Register (EC-Only offset 0h). On power-up, PCOBF is reset to 0. PCOBF will normally reflect the status of writes to EC2Host Data Register, if PCOBFEN is "0". PCOBF is cleared by hardware on a HOST read of the EC_HOST Data / AUX Data Register.

KIRQ is normally selected as IRQ1 for keyboard support.

Additional flexibility has been added which allows firmware to directly control the PCOBF output signal, independent of data transfers to the host-interface data output register. This feature allows the MEC140x/1x to be operated via the host "polled" mode. Firmware control is active when PCOBFEN is '1'. Firmware sets PCOBF high by writing a "1" to the PCOBF field of the PCOBF Register. Firmware must also clear PCOBF by writing a "0" to the PCOBF field.

TABLE 16-10: EC-ONLY REGISTER SUMMARY

Offset	Register Name (Mnemonic)
0h	HOST2EC Data Register
0h	EC2Host Data Register
4h	EC Keyboard Status Register
8h	Keyboard Control Register
Ch	EC AUX Data Register
14h	PCOBF Register

16.15.1 HOST2EC DATA REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	HOST2EC_DATA This register is an alias of the HOST_EC Data / CMD Register. When read at the EC-Only offset of 0h, it returns the data written by the Host to either Runtime Register offset 0h or Runtime Register offset 04h.	R	0h	nSYSRST

16.15.2 EC2HOST DATA REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC2HOST_DATA This register is an alias of the EC_HOST Data / AUX Data Register. Writing this register sets the OBF status bit.	W	0h	nSYSRST

16.15.3 EC KEYBOARD STATUS REGISTER

This register is an alias of the Keyboard Status Read Register. The fields C/D, IBF, and OBF remain read-only.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	UD2 User-defined data. Readable and writable by the EC.	R/W	0h	nSYSRST
5	AUXOBF Auxiliary Output Buffer Full. This bit is set to ‘1’ whenever the EC writes the EC AUX Data Register. This flag is reset to ‘0’ whenever the EC writes the EC2Host Data Register.	R/W	0h	nSYSRST

17.0 UART

17.1 Introduction

The 16550 UART (Universal Asynchronous Receiver/Transmitter) is a full-function Two Pin Serial Port that supports the standard RS-232 Interface.

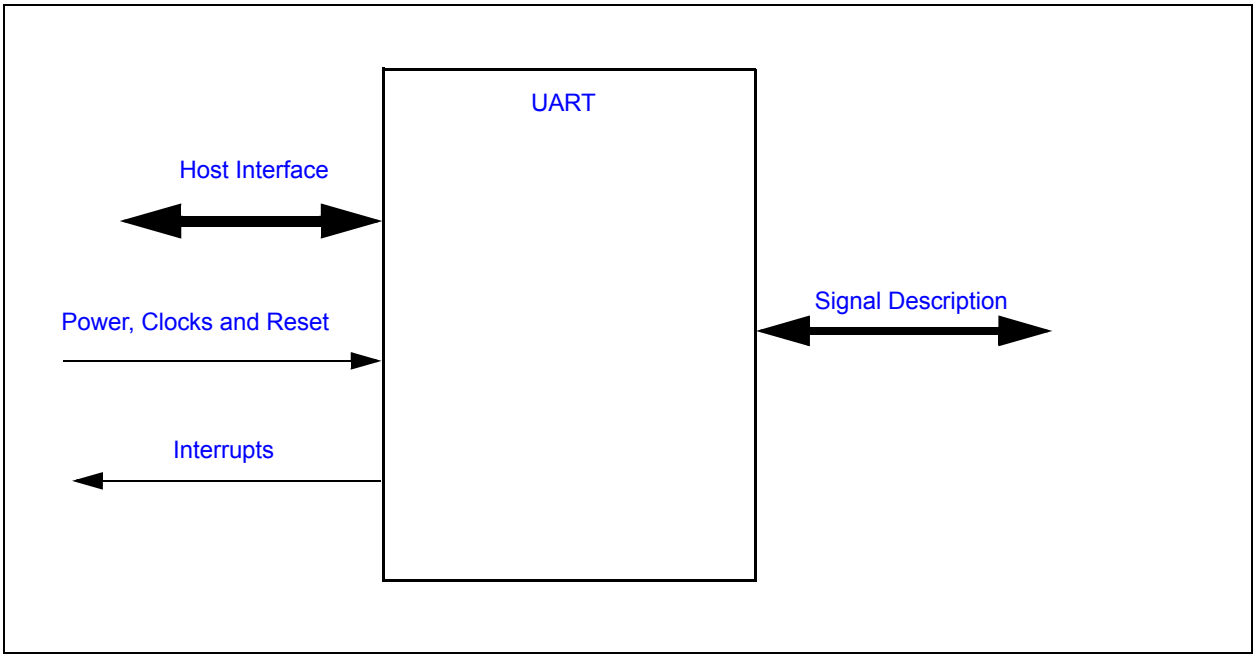
17.2 References

- EIA Standard RS-232-C specification

17.3 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 17-1: I/O DIAGRAM OF BLOCK



17.4 Signal Description

TABLE 17-1: SIGNAL DESCRIPTION

Name	Direction	Description
DTR#	Output	Active low Data Terminal ready output for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). **Note:** Defaults to tri-state on V3_DUAL power on.

17.11.11 MODEM STATUS REGISTER

Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	DCD This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to OUT2 in the MCR.	R	0h	RESET
6	RI# This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to OUT1 in the MCR.	R	0h	RESET
5	DSR This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to DTR in the MCR.	R	0h	RESET
4	CTS This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to nRTS in the MCR.	R	0h	RESET
3	DCD Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state. NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic ‘1’, a MODEM Status Interrupt is generated.	R	0h	RESET
2	RI Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic ‘0’ to logic ‘1’.	R	0h	RESET
1	DSR Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.	R	0h	RESET
0	CTS Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.	R	0h	RESET

Note: The Modem Status Register (MSR) only provides the current state of the UART MODEM control lines in Loopback Mode. The MEC140x/1x does not support external connections for the MODEM Control inputs (nCTS, nDSR, nRI and nDCD) or for the four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2).

21.10.1 CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:7	Reserved	R	-	-
6	POWERUP_EN This bit controls the state of the Power-Up Event Output and enables Week POWER-UP Event decoding in the VBAT-Powered Control Interface on page 462 . See Section 2.5.8, "Power-Up Event Output," on page 307 for a functional description of the POWER-UP_EN bit. 1=Power-Up Event Output Enabled 0=Power-Up Event Output Disabled and Reset	R/W	00h	VBAT_POR
5	BGPO VBAT-powered General Purpose Output Control that is used as part of the VBAT-Powered Control Interface. 1=Output high 0=Output low	R/W	00h	VBAT_POR
4:1	Reserved	R	-	-
0	WT_ENABILE The WT_ENABLE bit is used to start and stop the Week Alarm Counter Register and the Clock Divider Register. The value in the Counter Register is held when the WT_ENABLE bit is not asserted (‘0’) and the count is resumed from the last value when the bit is asserted (‘1’). The 15-Bit Clock Divider is reset to 00h and the RTC/Week Alarm Interface is in its lowest power consumption state when the WT_ENABLE bit is not asserted.	R/W	00h	VBAT_POR

21.10.2 WEEK ALARM COUNTER REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	Reserved	R	-	-
27:0	WEEK_COUNTER While the WT_ENABLE bit is ‘1’, this register is incremented at a 1 Hz rate. Writes of this register may require one second to take effect. Reads return the current state of the register. Reads and writes complete independently of the state of WT_ENABLE.	R/W	00h	VBAT_POR

Note:	Routing guidelines for the PECI_DAT pin is provided in Intel Platform design guides. Refer to the appropriate Intel document for current information. See TABLE 25-2:.

TABLE 25-2: PECI ROUTING GUIDELINES

Trace Impedance	50 Ohms +/- 15%
Spacing	10 mils
Routing Layer	Microstrip
Trace Width	Calculate to match impedance
Length	1” - 15”

25.6 Host Interface

The registers defined for the PECI Interface are accessible by the various hosts as indicated in Section 25.11, "PECI Interface Registers".

25.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

25.7.1 POWER DOMAINS

Name	Description
VTR	The PECI Interface logic and registers are powered by VTR.

25.7.2 CLOCK INPUTS

Name	Description
48 MHz Ring Oscillator	PECI Module Input Clock

25.7.3 RESETS

Name	Description
nSYSRST	PECI Core Reset Input

25.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
PECIHOST	PECI Host

25.9 Low Power Modes

The PECI Interface may be put into a low power state by the chip’s Power, Clocks, and Reset (PCR) circuitry.

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
10	TACH_READING_MODE_SELECT 1=Counter is incremented on the rising edge of the 100kHz_Clk input. The counter is latched into the TACHX_COUNTER field and reset when the programmed number of edges is detected. 0=Counter is incremented when TACHx Input transitions from low-to-high state (default)	R/W	0b	nSYSRST
9	Reserved	R	-	-
8	FILTER_ENABLE This filter is used to remove high frequency glitches from TACHx Input. When this filter is enabled, TACHx input pulses less than two 100kHz_Clk periods wide get filtered. 1= Filter enabled 0= Filter disabled (default) It is recommended that the TACHx input filter always be enabled.	R/W	0b	nSYSRST
7:2	Reserved	R	-	-
1	TACH_ENABLE This bit gates the clocks into the block. When clocks are gated, the TACHx pin is tristated. When re-enabled, the internal counters will continue from the last known state and stale status events may still be pending. Firmware should discard any status or reading values until the reading value has been updated at least one time after the enable bit is set. 1= TACH Monitoring enabled, clocks enabled. 0= TACH Idle, clocks gated	R/W	0b	nSYSRST
0	TACH_OUT_OF_LIMIT_ENABLE This bit is used to enable the TACH_OUT_OF_LIMIT_STATUS bit in the TACHx Status Register to generate an interrupt event. 1=Enable interrupt output from Tachometer block 0=Disable interrupt output from Tachometer block (default)	R/W	0b	nSYSRST

Note:	Pull-up resistors are required on both the KSI and KSO pins. Either external 10k ohm resistors or the internal resistors may be used. However, if the internal pull-ups are used then the PreDrive Mode must also be enabled.

30.6 Host Interface

The registers defined for the Keyboard Scan Interface are accessible by the various hosts as indicated in Section 30.11, "EC-Only Registers".

30.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

30.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

30.7.2 CLOCK INPUTS

Name	Description
48 MHz Ring Oscillator	This is the clock source for Keyboard Scan Interface logic.

30.7.3 RESETS

Name	Description
nSYSRST	This signal resets all the registers and logic in this block to their default state.

30.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
KSC_INT	Interrupt request to the Interrupt Aggregator.
KSC_INT_WAKE	Wake-up request to the Interrupt Aggregator’s wake-up interface.

30.9 Low Power Modes

The Keyboard Scan Interface automatically enters a low power mode whenever it is not actively scanning the keyboard matrix. The block is also placed in a low-power state when it is disabled by the KSEN bit. When the interface is in a low-power mode it will not prevent the chip from entering a sleep state. When the interface is active it will inhibit the chip sleep state until the interface has re-entered its low power mode.

37.0 VBAT-POWERED CONTROL INTERFACE

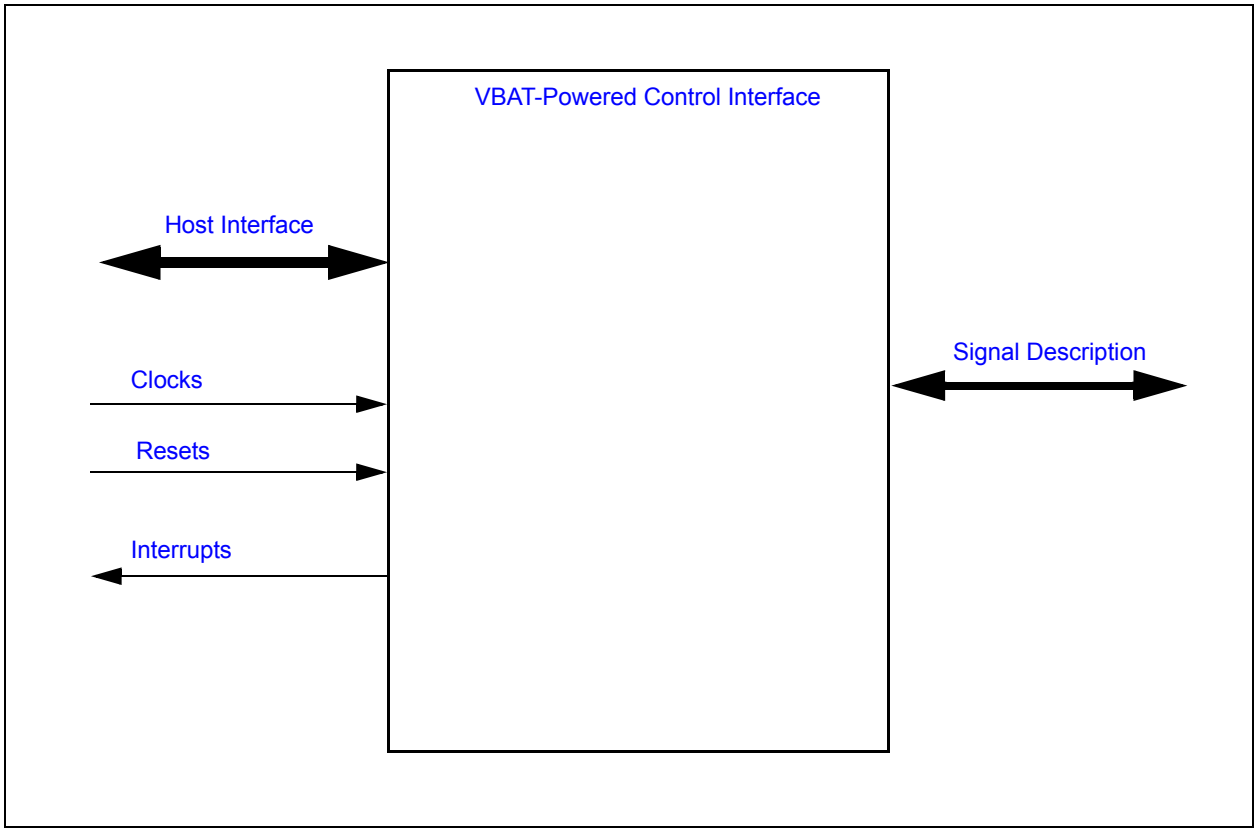
37.1 General Description

The VBAT-Powered Control Interface has VBAT powered combinational logic and input and output signal pins. The VBAT-Powered Control Interface block interfaces with the RTC/Week Timer on page 303.

37.2 Interface

This block's connections are entirely internal to the chip.

FIGURE 37-1: I/O DIAGRAM OF BLOCK



37.3 Signal Description

TABLE 37-1: EXTERNAL SIGNAL DESCRIPTION

Name	Direction	Description
VCI_OUT	OUTPUT	Output status driven by this block.
VCI_IN0#	INPUT	Input, active low
VCI_IN1#	INPUT	Input, active low
VCI_OVRD_IN	INPUT	Input, active high

TABLE 40-1: SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
CMP_VOUT0	Output	Comparator 0 output
CMP_VOUT1	Output	Comparator 1 output

40.6 Host Interface

The registers defined for the Comparator Interface are only accessible by the embedded controller. The Comparator Registers for both comparators are located in one register in the EC Subsystem register bank. See Section 34.8.2, "Comparator Control," on page 435.

40.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

40.7.1 POWER DOMAINS

Name	Description
VTR	The logic implemented in this block are powered by this power well.

40.7.2 CLOCK INPUTS

This component does not require a clock input.

40.7.3 RESETS

Name	Description
VTR_RESET#	This signal resets all the register in the EC Subsystem that interact with the comparators.

40.8 Interrupts

The comparators do not have a dedicated interrupt output event. An interrupt can be generated by the GPIO which shares the pin with the comparator output signal.

- GPIO124/CMP_VOUT0
- GPIO120/CMP_VOUT1

The GPIO interrupt is very configurable, thereby allowing CMP_VOUTx signal to generate an event when the CMP_VINx input is greater than the CMP_VREFx input or when it is less than the CMP_VREFx input. See the definition of Bits[7:4] of the Pin Control Register on page 329.

40.9 Low Power Modes

Each comparator is in its lowest powered state when its ENABLE bit is ‘0’.

44.0 REGISTER MEMORY MAP

TABLE 44-1: REGISTER MEMORY MAP

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
400	Watchdog Timer Interface	0	WDT Registers	WDT Load Register	2
404	Watchdog Timer Interface	0	WDT Registers	WDT Control Register	1
408	Watchdog Timer Interface	0	WDT Registers	WDT Kick Register	1
40C	Watchdog Timer Interface	0	WDT Registers	WDT Count Register	2
C00	Basic Timer	0	Basic_Timer_EC_Only	Timer Count	4
C04	Basic Timer	0	Basic_Timer_EC_Only	Timer Preload	4
C08	Basic Timer	0	Basic_Timer_EC_Only	Timer Status	4
C0C	Basic Timer	0	Basic_Timer_EC_Only	Timer Interrupt Enable	4
C10	Basic Timer	0	Basic_Timer_EC_Only	Timer Control	4
C20	Basic Timer	1	Basic_Timer_EC_Only	Timer Count	4
C24	Basic Timer	1	Basic_Timer_EC_Only	Timer Preload	4
C28	Basic Timer	1	Basic_Timer_EC_Only	Timer Status	4
C2C	Basic Timer	1	Basic_Timer_EC_Only	Timer Interrupt Enable	4
C30	Basic Timer	1	Basic_Timer_EC_Only	Timer Control	4
C40	Basic Timer	2	Basic_Timer_EC_Only	Timer Count	4
C44	Basic Timer	2	Basic_Timer_EC_Only	Timer Preload	4
C48	Basic Timer	2	Basic_Timer_EC_Only	Timer Status	4
C4C	Basic Timer	2	Basic_Timer_EC_Only	Timer Interrupt Enable	4
C50	Basic Timer	2	Basic_Timer_EC_Only	Timer Control	4
C60	Basic Timer	3	Basic_Timer_EC_Only	Timer Count	4
C64	Basic Timer	3	Basic_Timer_EC_Only	Timer Preload	4
C68	Basic Timer	3	Basic_Timer_EC_Only	Timer Status	4
C6C	Basic Timer	3	Basic_Timer_EC_Only	Timer Interrupt Enable	4
C70	Basic Timer	3	Basic_Timer_EC_Only	Timer Control	4
1800	SMB Device Interface	0	SMB_EC_Only	Status Register	1
1800	SMB Device Interface	0	SMB_EC_Only	Control Register	1
1801	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1804	SMB Device Interface	0	SMB_EC_Only	Own Address Register	2
1806	SMB Device Interface	0	SMB_EC_Only	Reserved	2
1808	SMB Device Interface	0	SMB_EC_Only	Data	1
1809	SMB Device Interface	0	SMB_EC_Only	Reserved	3
180C	SMB Device Interface	0	SMB_EC_Only	SMBus Master Command Register	4
1810	SMB Device Interface	0	SMB_EC_Only	SMBus Slave Command Register	4
1814	SMB Device Interface	0	SMB_EC_Only	PEC Register	1
1815	SMB Device Interface	0	SMB_EC_Only	Reserved	3