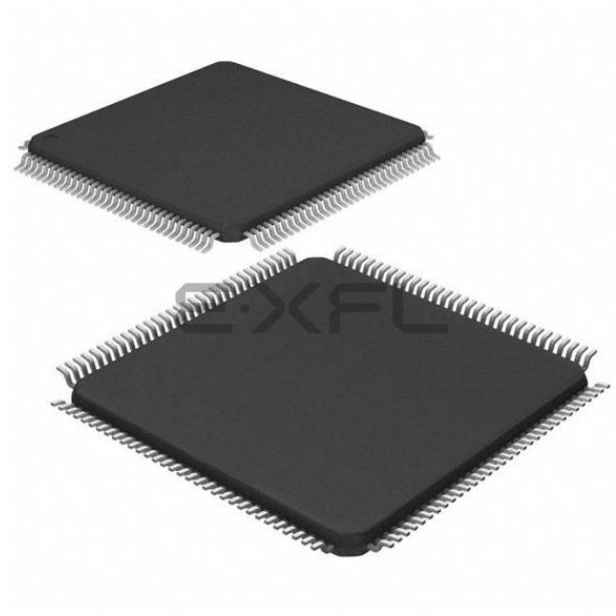

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Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	MIPS32® M14K™
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	192KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1408-nu

MEC140x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
35	Strap							
36	Default: 0	GPIO032	PIO	I-4	VTR	VTR/VCC	No Gate	
36	1	BCM_CLK0	PIO		VTR	VTR	Reserved	
36	2	PWM6	PIO		VTR	VTR	Reserved	
36	3	Reserved	Reserved		Reserved	Reserved		
36	Strap							
37	Default: 0	GPIO045	PIO	I-4	VTR	VTR/VCC	No Gate	
37	1	BCM_INT1#	PIO		VTR	VTR	High	
37	2	KSO04	PIO		VTR	VTR	Reserved	Note 15
37	3	Reserved	Reserved		Reserved	Reserved		
37	Strap							
38	Default: 0	GPIO046	PIO	I-4	VTR	VTR/VCC	No Gate	
38	1	BCM_DAT1	PIO		VTR	VTR	Low	Note 7
38	2	KSO05	PIO		VTR	VTR	Reserved	Note 15
38	3	Reserved	Reserved		Reserved	Reserved		
38	Strap							
39	Default: 0	GPIO047	PIO	I-4	VTR	VTR/VCC	No Gate	
39	1	BCM_CLK1	PIO		VTR	VTR	Reserved	
39	2	KSO06	PIO		VTR	VTR	Reserved	Note 15
39	3	Reserved	Reserved		Reserved	Reserved		
39	Strap							
40	Default: 0	GPIO050	PIO	I-4	VTR	VTR/VCC	No Gate	
40	1	TACH0	PIO		VTR	VTR	Low	
40	2	Reserved	Reserved		Reserved	Reserved		
40	3	Reserved	Reserved		Reserved	Reserved		
40	Strap							
41	Default: 0	GPIO051	PIO	I-4	VTR	VTR/VCC	No Gate	
41	1	TACH1	PIO		VTR	VTR	Low	
41	2	Reserved	Reserved		Reserved	Reserved		
41	3	Reserved	Reserved		Reserved	Reserved		
41	Strap							
42	Default: 0	GPIO052	PIO	I-4	VTR	VTR/VCC	No Gate	
42	1	SPI_IO2	PIO		VTR	VTR	Low	
42	2	Reserved	Reserved		Reserved	Reserved		
42	3	Reserved	Reserved		Reserved	Reserved		
42	Strap							
43		VTR	PWR		PWR	PWR		
43								
43								
43								
43	Strap							
44	Default: 0	GPIO053	PIO	I-4	VTR	VTR/VCC	No Gate	

MEC141x								
VTQFP Pin#	Mux	Signal Name	Buffer Type	Default Buffer Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
14	Strap							
15	Default: 0	GPIO016	PIO	I-4	VTR	VTR/VCC	No Gate	
15	1	KSO02	PIO		VTR	VTR	Reserved	Note 15
15	2	PVT_SCLK	PIO		VTR	VTR	Reserved	Note 10
15	3	Reserved	Reserved		Reserved	Reserved		
15	Strap							
16	Default: 0	GPIO017	PIO	I-4	VTR	VTR/VCC	No Gate	
16	1	KSO03	PIO		VTR	VTR	Reserved	Note 15
16	2	PVT_IO0	PIO		VTR	VTR	Low	Note 10
16	3	Reserved	Reserved		Reserved	Reserved		
16	Strap							
17		VSS	PWR		PWR	PWR		
17								
17								
17								
17	Strap							
18		VR_CAP	PWR		PWR	PWR		Note 3
18								
18								
18								
18	Strap							
19		VTR	PWR		PWR	PWR		
19								
19								
19								
19	Strap							
20	Default: 0	GPIO020	PIO	I-4	VTR	VTR/VCC	No Gate	
20	1	CMP_VIN0	I_AN		I_AN	I_AN	No Gate	
20	2	Reserved	Reserved		Reserved	Reserved		
20	3	Reserved	Reserved		Reserved	Reserved		
20	Strap							
21	Default: 0	GPIO021	PIO	I-4	PWR	VTR/VCC	No Gate	
21	1	CMP_VIN1	I_AN		I_AN	I_AN	No Gate	
21	2	Reserved	Reserved		Reserved	Reserved		
21	3	Reserved	Reserved		Reserved	Reserved		
21	Strap							
22	0	Reserved	Reserved		Reserved	Reserved		
22	Default: 1	DAC_VREF	DAC_VREF		DAC_VREF	DAC_VREF	No Gate	Note 18
22	2	Reserved	Reserved		Reserved	Reserved		
22	3	Reserved	Reserved		Reserved	Reserved		
22	Strap							
23	Default: 0	GPIO160	PIO	I-4	VTR	VTR/VCC	No Gate	

MEC141x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
123	1	Reserved	Reserved		Reserved	Reserved		
123	2	Reserved	Reserved		Reserved	Reserved		
123	3	Reserved	Reserved		Reserved	Reserved		
123	Strap							
124		VSS_VBAT	PWR		PWR	PWR		
124								
124								
124								
124	Strap							
125	Default: 0	XTAL2	ICLK	ICLK	VBAT	VBAT	No Gate	
125	1	Reserved	Reserved		Reserved	Reserved		
125	2	Reserved	Reserved		Reserved	Reserved		
125	3	Reserved	Reserved		Reserved	Reserved		
125	Strap							
126	0	GPIO162	PIO		VBAT	VTR/VCC	No Gate	
126	Default: 1	VCI_IN1#	ILLK	ILLK-4	VBAT	VBAT	High	Note 14
126	2	Reserved	Reserved		Reserved	Reserved		
126	3	Reserved	Reserved		Reserved	Reserved		
126	Strap							
127	0	GPIO163	PIO		VBAT	VTR/VCC	No Gate	
127	Default: 1	VCI_IN0#	ILLK	ILLK-4	VBAT	VBAT	High	Note 14
127	2	Reserved	Reserved		Reserved	Reserved		
127	3	Reserved	Reserved		Reserved	Reserved		
127	Strap							
128	0	GPIO164	PIO		VBAT	VTR/VCC	No Gate	
128	Default: 1	VCI_OVRD_IN	ILLK	ILLK-4	VBAT	VBAT	Low	Note 14
128	2	Reserved	Reserved		Reserved	Reserved		
128	3	Reserved	Reserved		Reserved	Reserved		
128	Strap							

3.4.3 POWER GOOD SIGNALS

The power good timing and thresholds are defined in the Section 43.1, "Voltage Thresholds and Power Good Timing," on page 501.

TABLE 3-3: POWER GOOD SIGNAL DEFINITIONS

Power Good Signal	Description	Source
VTRGD	VTRGD is an internal power good signal used to indicate when the VTR rail is on and stable.	VTRGD is asserted following a delay after the VTR power well exceeds its preset voltage threshold. VTRGD is de-asserted as soon as either of these voltages drop below this threshold. **Note:** See Section 43.1.1, "VTR Threshold and VTRGD Timing," on page 501.
VCC_PWRGD	VCC_PWRGD is used to indicate when the main power rail voltage is on and stable.	VCC_PWRGD Input pin

3.4.4 SYSTEM POWER SEQUENCING

The following table defines the behavior of the Power Sources in each of the defined ACPI power states.

TABLE 3-4: TYPICAL POWER SUPPLIES VS. ACPI POWER STATES

Supply Name	ACPI Power State						Description
	S0 (FULL ON)	S1 (POS)	S3 (STR)	S4 (STD)	S5 (Soft Off)	G3 (MECH Off)	
VTR_33_18	ON	ON	ON/OFF	ON/OFF	ON/OFF	OFF	LPC/eSPI Host Interface Power Supply.
VTR	ON	ON	ON	ON	ON	OFF	“Always-on” Supply. (Note 3-4)
VBAT	ON	ON	ON	ON (Note 3-5)	ON (Note 3-5)	ON (Note 3-5)	Battery Back-up Supply

Note 3-4 VTR power supply is always on while the battery pack or ac power is applied to the system.

Note 3-5 This device requires that the VBAT power is on when the VTR power supply is on. External circuitry, a diode isolation circuit, is implemented on the motherboard to extend the battery life. This external circuitry ensures the VBAT pin will derive power from the VTR power well when it is on. Therefore, the VBAT supply will never appear to be off when the VTR rail is on. See APPLICATION NOTE: on page 65.

3.5 Clocks

The following section defines the clocks that are generated and derived.

3.5.1 RAW CLOCK SOURCES

The table defines raw clocks that are either generated externally or via an internal oscillator.

TABLE 3-9: DEFINITION OF RESET SIGNALS (CONTINUED)

Reset	Description	Source
nRESET_IN	External Pin that can generate the equivalent of a VTR POR event. Asserting this signal will cause the nSYSRST to be asserted, which resets the majority of the chip.	Pin Interface
nRESET_OUT	External Pin that can generate the equivalent of a VCC POR or main reset event to other external devices.	This signal is asserted low when the nSIO_RESET is asserted low.
nSYSRST	Internal VTR Reset signal. This signal is used to reset VTR powered registers.	nSYSRST is asserted when VTRGD is low, when a WDT_RESET event occurs, when the nRESET_IN pin is asserted low, or when the EJTAG.PrRST bit is asserted. It is only deasserted when VTRGD is high, nRESET_IN is high, the EJTAG.PrRST bit is deasserted,.and their is no WDT_RESET event active. The EJTAG.PrRST bit is defined in the MIPS® EJTAG Specification, DN: MD00047, Rev 5.06, March 05, 2011.
LRESET#	System reset signal connected to the LPC LRESET# pin (also referred to as PCI Reset).	Pin Interface
eSPI_RESET#	System reset signal connected to the eSPI eSPI_RESET# pin	Pin Interface
eSPI_PLTRST#	Platform Reset.	Generated by the eSPI Block when VCC_PWRGD is low, when eSPI_RESET# is low, by a Virtual Wire, or by PC_Channel_Disable.
PCI_RESET#	System reset signal	Generated by either the LPC LRESET# pin (also referred to as PCI Reset) or the eSPI_PLTRST# depending on the configuration of the Host_Reset_Select bit.
nSIO_RESET	Performs a reset when VCC is turned off or when the system host resets the LPC or eSPI Host Interfaces.	nSIO_RESET is a signal that is asserted if nSYSRST is low, VCC_PWRGD is low, or PCI_RESET# is asserted low and may be deasserted when these three signals are all high. The iRESET_OUT bit controls the deassertion of nSIO_RESET. A WDT_RESET event will also cause an nSIO_RESET assertion.
WDT_RESET	Internal WDT Reset signal. This signal resets VTR powered registers with the exception of the WDT Event Count register. Note that the glitch protect circuits do not activate on a WDT reset. WDT_RESETdoes not reset VBAT registers or logic.	A WDT_RESET is asserted by a WDT Event. This event is indicated by the WDT bit in the Power-Fail and Reset Status Register
EC_PROC_RESET#	Internal reset signal to reset the processor in the EC Subsystem.	An EC_PROC_RESET# is a stretched version of the nSYSRST. This reset asserts at the same time that nSYSRST asserts and is held asserted for 1ms after the nSYSRST deasserts.

3.7 Chip Power Management Features

This device is designed to always operate in its lowest power state during normal operation. In addition, this device offers additional programmable options to put individual logical blocks to sleep as defined in Section 3.7.1, "Block Low Power Modes," on page 72 and to gate off or power down the internal oscillator as described in Section 3.7.2, "Configuring the Chip's Sleep States," on page 72.

CLKRUN# Support for Serial IRQ Cycle

If a logical device asserts or de-asserts an interrupt and CLKRUN# is sampled “high”, the LPC Controller can request the restoration of the clock by asserting the CLKRUN# signal asynchronously (TABLE 4-6:). The LPC Controller holds CLKRUN# low until it detects two rising edges of the clock. After the second clock edge, the controller must disable the open drain driver (FIGURE 4-3:).

The LPC Controller must not assert CLKRUN# if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in FIGURE 4-2:. The controller will not assert CLKRUN# under any conditions if the Serial IRQs are disabled.

The LPC Controller must not assert CLKRUN# unless the line has been de-asserted for two successive clocks; i.e., before the clock was stopped (FIGURE 4-3:).

The LPC Controller will not assert CLKRUN# if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR. The LPC Controller also will not assert CLKRUN# unless the signal has been de-asserted for two successive clocks; i.e., before the clock was stopped.

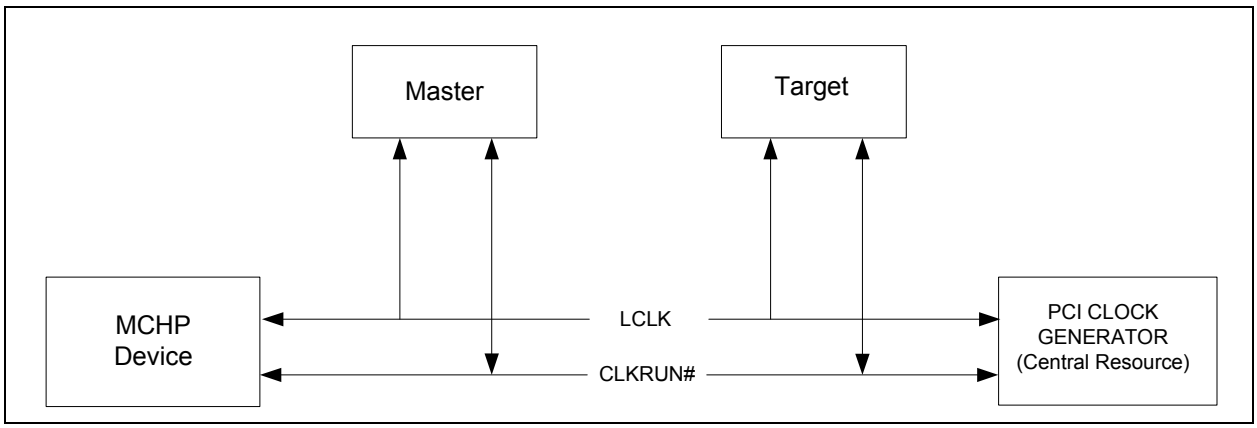
TABLE 4-6: LPC CONTROLLER CLKRUN# FUNCTION

SIRQ_MODE	Internal Interrupt Or DMA Request	CLKRUN#	Action
0	X	X	None
1	NO CHANGE	X	None
	CHANGE(Note 4-6)	0	None
		1	Assert CLKRUN#

Note 4-5 SIRQ_MODE is defined in Section 4.8.4.1, "Enabling SERIRQ Function," on page 107.

Note 4-6 “Change” means either-edge change on any or all parallel IRQs routed to the Serial IRQ block. The “change” detection logic must run asynchronously to LCLK and regardless of the Serial IRQ mode; i.e., “continuous” or “quiet”.

FIGURE 4-2: CLKRUN# SYSTEM IMPLEMENTATION EXAMPLE



Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
5:4	TX_DMA_ENABLE This bit enables DMA support for Transmit Transfer. If enabled, DMA will be requested to fill the FIFO until either the interface reaches TRANSFER_LENGTH or the DMA sends a termination request. The size defined here must match DMA programmed access size. 1=DMA is enabled.and set to 1 Byte 2=DMA is enabled and set to 2 Bytes 3=DMA is enabled and set to 4 Bytes 0=DMA is disabled. All data in the Transmit Buffer must be emptied by firmware	R/W	0h	RESET
3:2	TX_TRANSFER_ENABLE This field bit selects the transmit function of the SPI interface. 3=Transmit Enabled in 1 Mode. The MOSI or IO Bus will send out only 1's. The Transmit Buffer will not be used 2=Transmit Enabled in 0 Mode. The MOSI or IO Bus will send out only 0's. The Transmit Buffer will not be used. 1=Transmit Enabled. Data will be fetched from the Transmit Buffer and sent out on the MOSI or IO Bus. 0=Transmit is Disabled. Not data is sent. This will cause the MOSI be to be undriven, or the IO bus to be undriven if Receive is also disabled.	R/W	0h	RESET
1:0	INTERFACE_MODE This field sets the transmission mode. If this field is set for Dual Mode or Quad Mode then either TX_TRANSFER_ENABLE or RX_TRANSFER_ENABLE **must** be 0. 3=Reserved 2=Quad Mode 1=Dual Mode 0=Single/Duplex Mode	R/W	0h	RESET

6.11.3 QMSPI EXECUTE REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	Reserved	R	-	-
2	CLEAR_DATA_BUFFER Writing a ‘1’ to this bit will clear out the Transmit and Receive FIFOs. Any data stored in the FIFOs is discarded and all count fields are reset. Writing a ‘0’ to this bit has no effect. This bit is self-clearing.	W	0h	RESET

17.6 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

17.6.1 POWER DOMAINS

Name	Description
VTR	This Power Well is used to power the registers and logic in this block.

17.6.2 CLOCK INPUTS

Name	Description
1.8432MHz_Clk	The UART requires a 1.8432 MHz ± 2% clock input for baud rate generation.
24MHz_Clk	24 MHz ± 2% clock input. This clock may be enabled to generate the baud rate, which requires a 1.8432 MHz ± 2% clock input.

17.6.3 RESETS

Name	Description
nSYSRST	This reset is asserted when VTR is applied.
nSIO_RESET	This is an alternate reset condition, typically asserted when the main power rail is asserted.
RESET	This reset is determined by the POWER bit signal. When the power bit signal is 1, this signal is equal to nSIO_RESET. When the power bit signal is 0, this signal is equal to nSYSRST.

17.7 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
UART	The UART interrupt event output indicates if an interrupt is pending. See Table 17-8, “Interrupt Control,” on page 278.

Source	Description
UART	The UART interrupt event output indicates if an interrupt is pending. See Table 17-8, “Interrupt Control,” on page 278.

The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

TABLE 18-2: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	Timer Count Register
04h	Timer Preload Register
08h	Timer Status Register
0Ch	Timer Int Enable Register
10h	Timer Control Register

18.9.1 TIMER COUNT REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COUNTER This is the value of the Timer counter. This is updated by Hardware but may be set by Firmware. If it is set while the Hardware Timer is operating, functionality can not be ensured. When read, it is buffered so single byte reads will be able to catch the full 4 byte register without it changing. The size of the Counter is indicated by the instance name. Bits 0 to (size-1) are r/w counter bits. Bits 31 down to size are reserved. Reads return 0 and writes have no effect.	R/W	0h	Timer_Reset

18.9.2 TIMER PRELOAD REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	PRE_LOAD This is the value of the Timer pre-load for the counter. This is used by H/W when the counter is to be restarted automatically; this will become the new value of the counter upon restart. The size of the Pre-Load value is the same as the size of the counter. The size of the Counter is indicated by the instance name. Bits 0 to (size-1) are r/w pre-load bits. Bits 31 down to size are reserved. Reads return 0 and writes have no effect.	R/W	0h	Timer_Reset

21.9 Description

The RTC/Week Alarm block provides battery-powered timekeeping functions, derived from a low-power 32KHz clock, that operate even when the device's main power is off. The block contains a set of counters that can be used to generate one-shot and periodic interrupts to the EC for periods ranging from about 30 microseconds to over 8 years. The RTC/Week Alarm can be used in conjunction with the VBAT-Powered Control Interface to power up a sleeping system after a configurable period.

In addition to basic timekeeping, the RTC/Week Alarm block can be used to control the battery-powered general purpose BGPO outputs.

21.9.1 INTERNAL COUNTERS

The RTC/Week Timer includes 3 counters:

21.9.1.1 28-bit Week Alarm Counter

This counter is 28 bits wide. The clock for this counter is the overflow of the Clock Divider, and as long as the RTC/Week Timer is enabled, it is incremented at a 1 Hz rate.

Both an interrupt and a power-up event can be generated when the contents of this counter matches the contents of the Week Timer Compare Register.

21.9.1.2 9-bit Sub-Week Alarm Counter

This counter is 9 bits wide. It is decremented by 1 at each tick of its selected clock. It can be configured either as a one-shot or repeating event generator.

Both an interrupt and a power-up event can be generated when this counter decrements from 1 to 0.

The Sub-Week Alarm Counter can be configured with a number of different clock sources for its time base, derived from either the Week Alarm Counter or the Clock Divider, by setting the SUBWEEK_TICK field of the Sub-Week Control Register.

TABLE 21-7: SUB-WEEK ALARM COUNTER CLOCK

SUBWEEK_ TICK	Source	SPISR	Frequency	Minimum Duration	Maximum Duration
0	Counter Disabled				
1	Sub-Second	0	Counter Disabled		
		1	2 Hz	500 ms	255.5 sec
		2	4 Hz	250 ms	127.8 sec
		3	8 Hz	125 ms	63.9 sec
		4	16 Hz	62.5	31.9 sec
		5	32 Hz	31.25 ms	16.0 sec
		6	64 Hz	15.6 ms	8 sec
		7	128 Hz	7.8 ms	4 sec
		8	256 Hz	3.9 ms	2 sec
		9	512 Hz	1.95 ms	1 sec
		10	1024 Hz	977 µS	499 ms
		11	2048 Hz	488 µS	249.5 ms
		12	4096 Hz	244 µS	124.8 ms
		13	8192 Hz	122 µS	62.4 ms
		14	16.384 Khz	61.1 µS	31.2 ms
		15	32.768 KHz	30.5 µS	15.6 ms
2	Second	n/a	1 Hz	1 sec	511 sec
3	Reserved				
4	Week Counter bit 3	n/a	125 Hz	8 sec	68.1 min

22.3 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

22.3.1 POWER DOMAINS

Name	Description
VTR	The registers and logic in this block are powered by VTR.

22.3.2 CLOCK INPUTS

Name	Description
48 MHz Ring Oscillator	The 48 MHz Ring Oscillator is used for synchronizing the GPIO inputs.

22.3.3 RESETS

Name	Description
nSYSRST	This reset is asserted when VTR is applied.
nSIO_RESET	This is an alternate reset condition, typically asserted when the main power rail is asserted. This reset is used for VCC Power Well Emulation.

22.4 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
GPIO_Event	Each pin in the GPIO Interface has the ability to generate an interrupt event. This event may be used as a wake event. The GPIO Interface can generate an interrupt source event on a high level, low level, rising edge and falling edge, as configured by the Interrupt Detection (int_det) bits in the Pin Control Register associated with the GPIO signal function. **Note:** The minimum pulse width required to generate an interrupt/wakeup event is 5ns.

22.5 Description

The GPIO Interface refers to all the GPIOxxx pins implemented in the design. GPIO stands for General Purpose I/O.

The GPIO signals may be used by firmware to both monitor and control a pin in “bit-banged” mode. The GPIOs may be individually controlled via their Pin Control Register or group controlled via the Output and Input GPIO registers. The GPIO Output Control Select

The GPIO Pin control registers are used to select the alternate functions on GPIO pins (unless otherwise specified), to control the buffer direction, strength, and polarity, to control the internal pull-ups and pull-downs, for VCC emulation, and for selecting the event type that causes a GPIO interrupt.

The GPIO input is always live, even when an alternate function is selected. Firmware may read the GPIO input anytime to see the value on the pin. In addition, the GPIO interrupt is always functional, and may be used for either the GPIO itself or to support the alternate functions on the pin. See FIGURE 22-1: GPIO Interface Block Diagram on page 313.

MEC141x				
GPIO Name (Octal)	**Mux Control = 00**	**Mux Control = 01**	**Mux Control = 10**	**Mux Control = 11**
GPIO136	GPIO136	SHD_IO3	Reserved	Reserved
GPIO140	GPIO140	KSO17	Reserved	Reserved
GPIO141	GPIO141	SMB04_DATA	SMB04_DATA18	Reserved
GPIO142	GPIO142	SMB04_CLK	SMB04_CLK18	Reserved
GPIO143	GPIO143	KSI0	DTR#	Reserved
GPIO144	GPIO144	KSI1	DCD#	Reserved
GPIO145	GPIO145	Reserved	Reserved	Reserved
GPIO146	GPIO146	Reserved	Reserved	Reserved
GPIO147	GPIO147	KSI4	DSR#	Reserved
GPIO150	GPIO150	KSI5	RI#	Reserved
GPIO151	GPIO151	KSI6	RTS#	Reserved
GPIO152	GPIO152	KSI7	CTS#	Reserved
GPIO153	GPIO153	ADC4	Reserved	Reserved
GPIO154	GPIO154	ADC3	Reserved	Reserved
GPIO155	GPIO155	ADC2	Reserved	Reserved
GPIO156	GPIO156	LED1	Reserved	Reserved
GPIO157	GPIO157	LED0	TST_CLK_OUT	Reserved
GPIO160	GPIO160	DAC_0	Reserved	Reserved
GPIO161	GPIO161	DAC_1	Reserved	Reserved
GPIO162	GPIO162	VCI_IN1#	Reserved	Reserved
GPIO163	GPIO163	VCI_IN0#	Reserved	Reserved
GPIO164	GPIO164	VCI_OVRD_IN	Reserved	Reserved
GPIO165	GPIO165	CMP_VREF0	Reserved	Reserved
GPIO166	GPIO166	CMP_VREF1	UART_CLK	Reserved

22.5.4 PIN CONTROL REGISTERS

Each GPIO has two Pin Control registers. The Pin Control Register, which is the primary register, is used to read the value of the input data and set the output either high or low. It is used to select the alternate function via the Mux Control bits, set the Polarity of the input, configure and enable the output buffer, configure the GPIO interrupt event source, enable internal pull-up/pull-down resistors, and to enable VCC Emulation via the Power Gating Signals control bits. The Pin Control Register 2 is used to configure the output buffer drive strength and slew rate.

The following tables define the default settings for the two Pin Control registers for each GPIO in each product group.

22.5.4.1 MEC140x Pin Control Registers Defaults

MEC140x						
GPIO Name (Octal)	**Pin Control Register Offset (Hex)**	**Pin Control Register Default (Hex)**	**Default Function**	**Pin Control Register 2 Offset (Hex)**	**Pin Control Register 2 Default (Hex)**	**Default Drive Strength (mA)**
GPIO001	0004	00000000	GPIO001	504	00000010	4
GPIO002	0008	00000000	GPIO002	508	00000010	4
GPIO003	000C	00001000	SYS-PWR_PRES	50C	00000010	4

Offset	See Table 22-2, "Register Summary"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
6:4	Interrupt Detection (int_det) The interrupt detection bits determine the event that generates a GPIO_Event. **Note:** See Table 22-3, "Edge Enable and Interrupt Detection Bits Definition". **Note:** Since the GPIO input is always available, even when the GPIO is not selected as the alternate function, the GPIO interrupts may be used for detecting pin activity on alternate functions. The only exception to this is the analog functions (e.g., ADC, DAC, Comparator inputs)	R/W	Note 22-6	nSYSRST
3:2	Power Gating Signals The Power Gating Signals provide the chip Power Emulation options. The pin will be tristated when the selected power well is off (i.e., gated) as indicated. The Emulated Power Well column defined in Pin Multiplexing tables indicates the emulation options supported for each signal. The Signal Power Well column defines the buffer power supply per function. **Note:** Note that all GPIOs support Power Gating unless otherwise noted. 00 = VTR The output buffer is tristated when VTRGD = 0. 01 = VCC The output buffer is tristate when VCC_PWRGD = 0. 10 = Reserved 11 = Reserved	R/W	Note 22-6	nSYSRST
1:0	PU/PD (PU_PD) These bits are used to enable an internal pull-up or pull-down resistor device on the pin. 00 = None. Pin tristates when no active driver is present on the pin. 01 = Pull Up Enabled 10 = Pull Down Enabled (Note 22-7) 11 = Repeater mode. Pin is kept at previous voltage level when no active driver is present on the pin.	R/W	Note 22-6	nSYSRST

Note 22-6 See Section 22.5.4, "Pin Control Registers," on page 320 for the offset and default values for each GPIO Pin Control Register.

Note 22-7 The internal pull-down control should not be selected when configured for an LPC function, which uses the PCI_PIO buffer. Signals with PCI_PIO buffer type do not have an internal pull-down. This configuration option has no effect on the pin.

TABLE 22-3: EDGE ENABLE AND INTERRUPT DETECTION BITS DEFINITION

Edge Enable	Interrupt Detection Bits			Selected Function
D7	D6	D5	D4	
0	0	0	0	Low Level Sensitive
0	0	0	1	High Level Sensitive
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Interrupt events are disabled
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	1	0	1	Rising Edge Triggered
1	1	1	0	Falling Edge Triggered
1	1	1	1	Either edge triggered

Note: Only edge triggered interrupts can wake up the main ring oscillator. The GPIO must be enabled for edge-triggered interrupts and the GPIO interrupt must be enabled in the interrupt aggregator in order to wake up the ring when the ring is shut down.

APPLICATION NOTE: All GPIO interrupt detection configurations default to '0000', which is low level interrupt. Having interrupt detection enabled will un-gated the clock to the GPIO module whenever the interrupt is active, which increases power consumption. Interrupt detection should be disabled when not required to save power; this is especially true for pin interfaces (i.e., LPC).

22.6.1.2 Pin Control Register 2

Offset	See Note 22-6			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:6	RESERVED	RES	-	-
5:4	Drive Strength These bits are used to select the drive strength on the pin. 00 = 2mA 01 = 4mA 10 = 8mA 11 = 12mA	R/W	00	nSYSRST

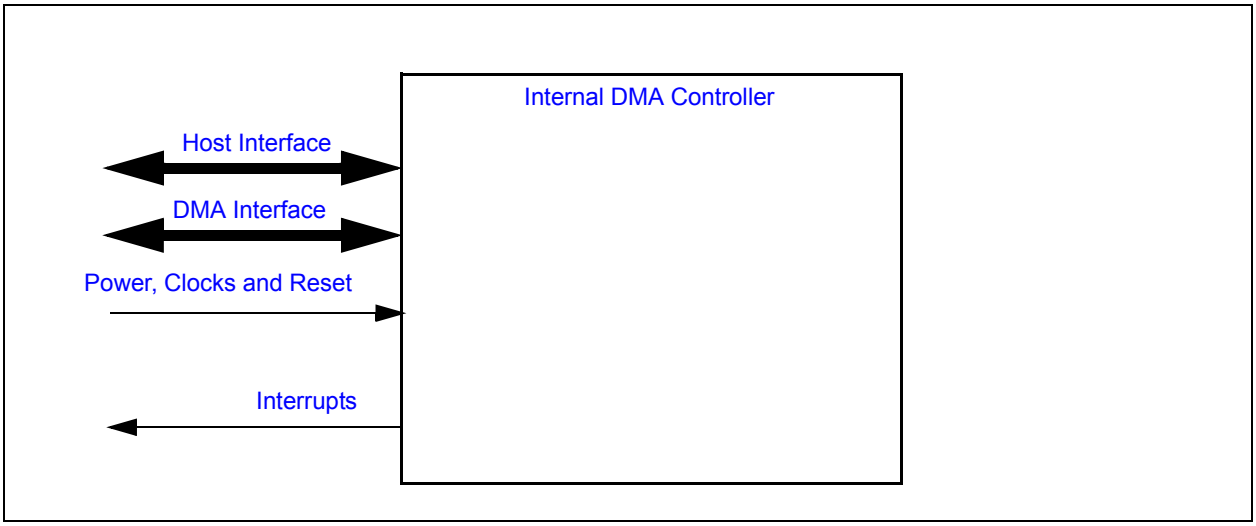
TABLE 24-1: TERMINOLOGY (CONTINUED)

Term	Definition
Source	The DMA Controller moves data from the Source to the Destination. The Source provides the data. The Source may be either the Master or Slave Controller.
Destination	The DMA Controller moves data from the Source to the Destination. The Destination receives the data. The Destination may be either the Master or Slave Controller.

24.5 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 24-1: INTERNAL DMA CONTROLLER I/O DIAGRAM



24.5.1 SIGNAL DESCRIPTION

This block doesn't have any external signals that may be routed to the pin interface. This DMA Controller is intended to be used internally to transfer large amounts of data without the embedded controller being actively involved in the transfer.

24.5.2 HOST INTERFACE

The registers defined for the Internal DMA Controller are accessible by the various hosts as indicated in Section 24.10, "DMA Main Registers".

24.5.3 DMA INTERFACE

Each DMA Master Device that may engage in a DMA transfer must have a compliant DMA interface. The following table lists the DMA Devices in the MEC140x/1x.

TABLE 24-2: DMA CONTROLLER DEVICE SELECTION

Device Name	Device Number (Note 1)	Controller Source
SMBus 0 Controller	0	Slave
	1	Master

24.11.9 DMA CHANNEL N CRC DATA REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CRC Writes to this register initialize the CRC generator. Reads from this register return the output of the CRC that is calculated from the data transfered by DMA Channel N. The output of the CRC generator is bit-reversed and inverted on reads, as required by the CRC-32-IEEE definition. A CRC can be accumulated across multiple DMA transactions on Channel N. If it is necessary to save the intermediate CRC value, the result of the read of this register must be bit-reversed and inverted before being written back to this register.	R/W	0h	DMA_ RESET

24.11.10 DMA CHANNEL N CRC POST STATUS REGISTER

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3	CRC_POST_TEST2 This is a test bit. Read back data is unpredictable.	R	0h	DMA_ RESET
2	CRC_POST_TRANSFER This bit is cleared to ‘0’ when a DMA transaction starts. If Post Transfer is enabled, and the CRC is successfully transferred following the completion of the DMA transaction, this bit is set to ‘1’. If the post transfer of the CRC is inhibited, because either firmware or the device terminated the transaction, this bit remains ‘0’.	R	0h	DMA_ RESET
1	CRC_POST_TEST1 This is a test bit. Read back data is unpredictable.	R	0h	DMA_ RESET
0	CRC_POST_TEST0 This is a test bit. Read back data is unpredictable.	R	0h	DMA_ RESET

amount determined by the LED_STEP register and at a rate determined by the **DELAY** counter. Once the duty cycle reaches its maximum value (determined by the field MAX), the duty cycle is held constant for a period determined by the field HD. Once the hold time is complete, the **DUTY CYCLE** register is decreased, again by an amount determined by the LED_STEP register and at a rate determined by the **DELAY** counter. When the duty cycle then falls at or below the minimum value (determined by the field MIN), the duty cycle is held constant for a period determined by the field HD. Once the hold time is complete, the cycle repeats, with the duty cycle oscillating between MIN and MAX.

The rising and falling ramp times as shown in on page 379 can be either symmetric or asymmetric depending on the setting of the SYMMETRY bit in the LED Configuration Register Register. In Symmetric mode the rising and falling ramp rates have mirror symmetry; both rising and falling ramp rates use the same (all) 8 segments fields in each of the following registers (see TABLE 28-7:): the LED Update Stepsize Register register and the LED Update Interval Register register. In Asymmetric mode the rising ramp rate uses 4 of the 8 segments fields and the falling ramp rate uses the remaining 4 of the 8 segments fields (see TABLE 28-7:).

The parameters MIN, MAX, HD, LD and the 8 fields in LED_STEP and LED_INT determine the brightness range of the LED and the rate at which its brightness changes. See the descriptions of the fields in Section 28.10, "EC-Only Registers", as well as the examples in Section 28.9.3, "Breathing Examples" for information on how to set these fields.

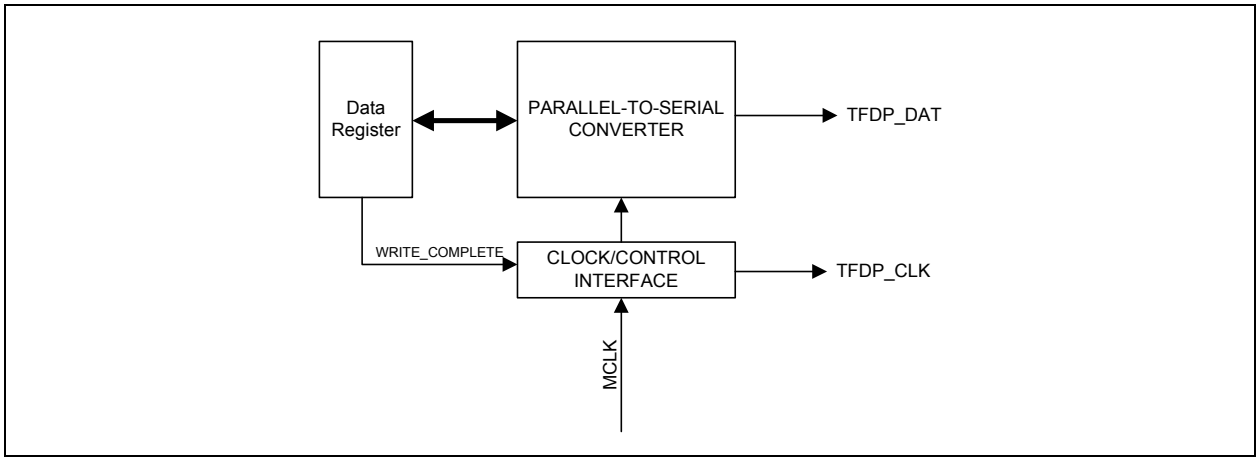
TABLE 28-7: SYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 28-3, "Clipping Example"	Duty Cycle	Segment Index	Symmetric Mode Register Fields Utilized	
X	000xxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
X	001xxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
X	010xxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]
X	011xxxxxb	011b	STEP[3]/INT[3]	Bits[15:12]
X	100xxxxxb	100b	STEP[4]/INT[4]	Bits[19:16]
X	101xxxxxb	101b	STEP[5]/INT[5]	Bits[23:20]
X	110xxxxxb	110b	STEP[6]/INT[6]	Bits[27:24]
X	111xxxxxb	111b	STEP[7]/INT[7]	Bits[31:28]
Note: In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]				

TABLE 28-8: ASYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 28-3, "Clipping Example"	Duty Cycle	Segment Index	Asymmetric Mode Register Fields Utilized	
Rising	00xxxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
Rising	01xxxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
Rising	10xxxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]
Rising	11xxxxxxb	011b	STEP[3]/INT[3]	Bits[15:12]
falling	00xxxxxxb	100b	STEP[4]/INT[4]	Bits[19:16]
falling	01xxxxxxb	101b	STEP[5]/INT[5]	Bits[23:20]

FIGURE 32-2: BLOCK DIAGRAM OF TFDP DEBUG PORT

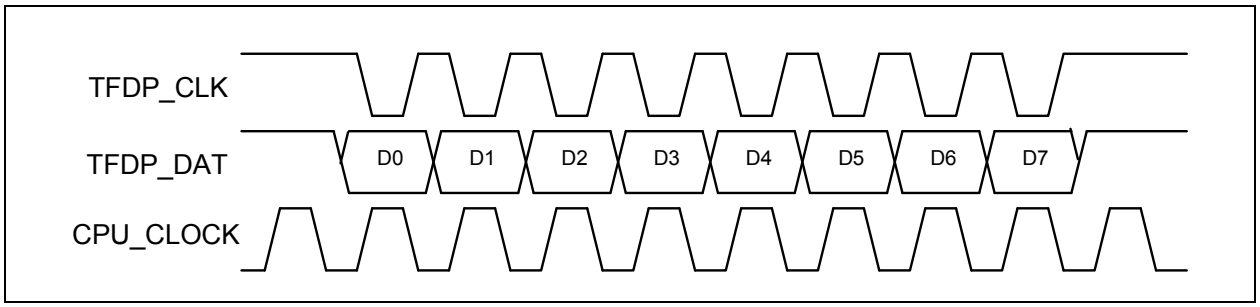


The firmware executing on the embedded controller writes to the Debug Data Register to initiate a transfer cycle (32.11). At first, data from the Debug Data Register is shifted into the LSB. Afterwards, it is transmitted at the rate of one byte per transfer cycle.

Data is transferred in one direction only from the Debug Data Register to the external interface. The data is shifted out at the clock edge. The clock edge is selected by the EDGE_SEL bit in the Debug Control Register. After being shifted out, valid data is guaranteed at the opposite edge of the TFDP_CLK. For example, when the EDGE_SEL bit is '0' (default), valid data is provided at the falling edge of TFDP_CLK. The Setup Time (to the falling edge of TFDP_CLK) is 10 ns, minimum. The Hold Time is 1 ns, minimum.

When the Serial Debug Port is inactive, the TFDP_CLK and TFDP_DAT outputs are '1.' The EC Bus Clock clock input is the transfer clock.

FIGURE 32-3: DATA TRANSFER



32.11 EC-Only Registers

The registers listed in the EC-Only Register Summary table are for a single instance of the Trace FIFO Debug Port (TFDP). The addresses of each register listed in this table are defined as a relative offset to the host "Base Address" defined in the EC-Only Register Base Address Table.

TABLE 32-2: EC-ONLY REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
TFDP Debug Port	0	EC	32-bit internal address space	0000_8C00h

TABLE 40-1: SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
CMP_VOUT0	Output	Comparator 0 output
CMP_VOUT1	Output	Comparator 1 output

40.6 Host Interface

The registers defined for the Comparator Interface are only accessible by the embedded controller. The Comparator Registers for both comparators are located in one register in the EC Subsystem register bank. See Section 34.8.2, "Comparator Control," on page 435.

40.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

40.7.1 POWER DOMAINS

Name	Description
VTR	The logic implemented in this block are powered by this power well.

40.7.2 CLOCK INPUTS

This component does not require a clock input.

40.7.3 RESETS

Name	Description
VTR_RESET#	This signal resets all the register in the EC Subsystem that interact with the comparators.

40.8 Interrupts

The comparators do not have a dedicated interrupt output event. An interrupt can be generated by the GPIO which shares the pin with the comparator output signal.

- GPIO124/CMP_VOUT0
- GPIO120/CMP_VOUT1

The GPIO interrupt is very configurable, thereby allowing CMP_VOUTx signal to generate an event when the CMP_VINx input is greater than the CMP_VREFx input or when it is less than the CMP_VREFx input. See the definition of Bits[7:4] of the Pin Control Register on page 329.

40.9 Low Power Modes

Each comparator is in its lowest powered state when its ENABLE bit is ‘0’.

TABLE 42-5: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
IO-2 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an O-2mA.
OD-2 mA Type Buffer Low Output Level Tolerance	V_{OL}			0.4	V	V_{OL} = 2 mA This buffer is not 5V tolerant.
IOD-2 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an OD-2mA.
O-4 mA Type Buffer Low Output Level High Output Level Tolerance	V_{OL} V_{OH}	 VTR-0.4		0.4	V V	I_{OL} = 4 mA I_{OH} = -4 mA This buffer is not 5V tolerant.
IO-4 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an O-4mA.
OD-4 mA Type Buffer Low Output Level Tolerance	V_{OL}			0.4	V	V_{OL} = 4 mA This buffer is not 5V tolerant.
IOD-4 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an OD-4mA.
O-8 mA Type Buffer Low Output Level High Output Level Tolerance	V_{OL} V_{OH}	 VTR-0.4		0.4	V V	I_{OL} = 8 mA I_{OH} = -8 mA This buffer is not 5V tolerant.
IO-8 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an O-8mA.
OD-8 mA Type Buffer Low Output Level Tolerance	V_{OL}			0.4	V	V_{OL} = 8 mA This buffer is not 5V tolerant.
IOD-8 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an OD-8mA.