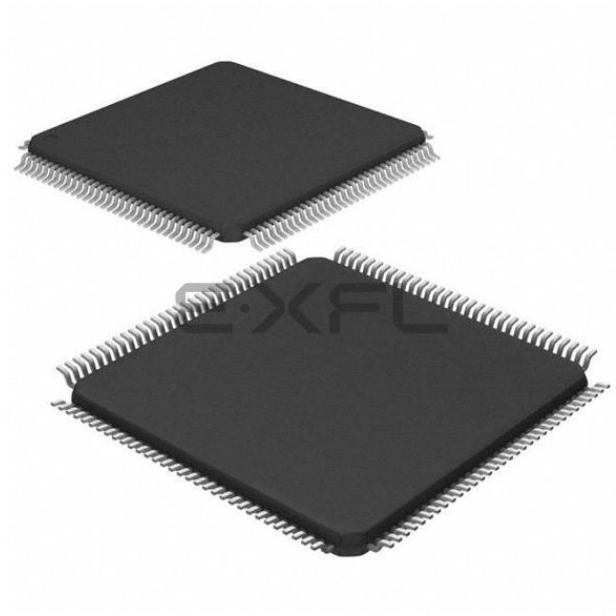

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Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	MIPS32® M14K™
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Controller Series	-
RAM Size	128KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1414-i-nu

Interface	Signal Name	Description	Notes
Analog Data Acquisition Interface	ADC3	ADC channel 3	Note 8
Analog Data Acquisition Interface	ADC4	ADC channel 4	Note 8
Analog Data Acquisition Interface	ADC5	ADC channel 5	Note 8
Analog Data Acquisition Interface	ADC6	ADC channel 6	Note 8
Analog Data Acquisition Interface	ADC7	ADC channel 7	Note 8
BC-Link Interface	BCM_CLK0	BC-Link Master clock	
BC-Link Interface	BCM_CLK1	BC-Link Master clock	
BC-Link Interface	BCM_DAT0	BC-Link Master data I/O	Note 7
BC-Link Interface	BCM_DAT1	BC-Link Master data I/O	Note 7
BC-Link Interface	BCM_INT0#	BC-Link Master interrupt	
BC-Link Interface	BCM_INT1#	BC-Link Master interrupt	
Comparator Interface	CMP_VIN0	Comparator 0 Positive Input	
Comparator Interface	CMP_VIN1	Comparator 1 Positive Input	
Comparator Interface	CMP_VOUT0	Comparator 0 Output	
Comparator Interface	CMP_VOUT1	Comparator 1 Output	
Comparator Interface	CMP_VREF0	Comparator 0 Negative Input	
Comparator Interface	CMP_VREF1	Comparator 1 Negative Input	
Digatal to Analog (DAC) Interface	DAC_0	DAC channel 0	
Digatal to Analog (DAC) Interface	DAC_1	DAC channel 1	
eSPI HOST INTERFACE	ESPI_ALERT#	eSPI Alert	
eSPI HOST INTERFACE	ESPI_CLK	eSPI Clock	
eSPI HOST INTERFACE	ESPI_CS#	eSPI Chip Select	
eSPI HOST INTERFACE	ESPI_IO0	eSPI Data Pin 0	
eSPI HOST INTERFACE	ESPI_IO1	eSPI Data Pin 1	
eSPI HOST INTERFACE	ESPI_IO2	eSPI Data Pin 2	
eSPI HOST INTERFACE	ESPI_IO3	eSPI Data Pin 3	
eSPI HOST INTERFACE	ESPI_RESET#	eSPI Reset	
GPIO Interface	GPIO	General Purpose Input Output Pins	
ICSP Interface	ICSP_CLOCK	2-Wire Debug Clock	
ICSP Interface	ICSP_DATA	2-Wire Debug Data	
ICSP Interface	ICSP_MCLR	2-Wire Debug Master Reset	Note 2
Keyboard Scan Interface	KSI0	Keyboard Scan Matrix Input 0	Note 15
Keyboard Scan Interface	KSI1	Keyboard Scan Matrix Input 1	Note 15
Keyboard Scan Interface	KSI2	Keyboard Scan Matrix Input 2	Note 15
Keyboard Scan Interface	KSI3	Keyboard Scan Matrix Input 3	Note 15
Keyboard Scan Interface	KSI4	Keyboard Scan Matrix Input 4	Note 15
Keyboard Scan Interface	KSI5	Keyboard Scan Matrix Input 5	Note 15
Keyboard Scan Interface	KSI6	Keyboard Scan Matrix Input 6	Note 15
Keyboard Scan Interface	KSI7	Keyboard Scan Matrix Input 7	Note 15
Keyboard Scan Interface	KSO00	Keyboard Scan Matrix Output 0	Note 15

MEC140x								
VTQFP Pin#	Mux	Signal Name	Buffer Type	Default Buffer Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
77	Strap							
78	Default: 0	GPIO114	PIO	I-4	VTR	VTR/VCC	No Gate	
78	1	PS2_CLK0	PIO		VTR	VTR/VCC	Low	
78	2	Reserved	Reserved		Reserved	Reserved		
78	3	Reserved	Reserved		Reserved	Reserved		
78	Strap							
79	Default: 0	GPIO115	PIO	I-4	VTR	VTR/VCC	No Gate	
79	1	PS2_DAT0	PIO		VTR	VTR/VCC	Low	
79	2	Reserved	Reserved		Reserved	Reserved		
79	3	Reserved	Reserved		Reserved	Reserved		
79	Strap							
80	Default: 0	GPIO116	PIO	I-4	VTR	VTR/VCC	No Gate	
80	1	TFDP_DATA	PIO		VTR	VTR	Reserved	
80	2	UART_RX	PIO		VTR	VTR	Low	
80	3	Reserved	Reserved		Reserved	Reserved		
80	Strap							
81	Default: 0	GPIO117	PIO	I-4	VTR	VTR/VCC	No Gate	
81	1	TFDP_CLK	PIO		VTR	VTR	Reserved	
81	2	UART_TX	PIO		VTR	VTR	Reserved	
81	3	Reserved	Reserved		Reserved	Reserved		
81	Strap							
82		VTR	PWR		PWR	PWR		
82								
82								
82								
82	Strap							
83	Default: 0	GPIO120	PIO	I-4	VTR	VTR/VCC	No Gate	
83	1	CMP_VOUT1	PIO		VTR	VTR	Reserved	
83	2	Reserved	Reserved		Reserved	Reserved		
83	3	Reserved	Reserved		Reserved	Reserved		
83	Strap							
84		VSS	PWR		PWR	PWR		
84								
84								
84								
84	Strap							
85	Default: 0	GPIO124	PIO	I-4	VTR	VTR/VCC	No Gate	
85	1	CMP_VOUT0	PIO		VTR	VTR	Reserved	
85	2	Reserved	Reserved		Reserved	Reserved		
85	3	Reserved	Reserved		Reserved	Reserved		
85	Strap							
86	Default: 0	GPIO125	PIO	I-4	VTR	VTR/VCC	No Gate	

MEC141x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
56	Strap							
57	Default: 0	GPIO034	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
57	1	PCI_CLK	PCI_IO		VTR	VCC	Low	
57	2	ESPI_CLK	PIO		VTR_33_18	VTR	Low	
57	3	Reserved	Reserved		Reserved	Reserved		
57	Strap							
58	Default: 0	GPIO044	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
58	1	LFRAME#	PCI_IO		VTR	VCC	High	
58	2	ESPI_CS#	PIO		VTR_33_18	VTR	High	
58	3	Reserved	Reserved		Reserved	Reserved		
58	Strap							
59	Default: 0	GPIO040	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
59	1	LAD0	PCI_IO		VTR	VCC	High	Note 1
59	2	ESPI_IO0	PIO		VTR_33_18	VTR	Low	
59	3	Reserved	Reserved		Reserved	Reserved		
59	Strap							
60	Default: 0	GPIO041	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
60	1	LAD1	PCI_IO		VTR	VCC	High	Note 1
60	2	ESPI_IO1	PIO		VTR_33_18	VTR	Low	
60	3	Reserved	Reserved		Reserved	Reserved		
60	Strap							
61	Default: 0	GPIO042	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
61	1	LAD2	PCI_IO		VTR	VCC	High	Note 1
61	2	ESPI_IO2	PIO		VTR_33_18	VTR	Low	
61	3	Reserved	Reserved		Reserved	Reserved		
61	Strap							
62	Default: 0	GPIO043	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
62	1	LAD3	PCI_IO		VTR	VCC	High	Note 1
62	2	ESPI_IO3	PIO		VTR_33_18	VTR	Low	
62	3	Reserved	Reserved		Reserved	Reserved		
62	Strap							
63	Default: 0	GPIO067	PCI_PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
63	1	CLKRUN#	PCI_IO		VTR	VCC	Low	
63	2	Reserved	Reserved		Reserved	Reserved		
63	3	Reserved	Reserved		Reserved	Reserved		
63	Strap							
64		VSS	PWR		PWR	PWR		
64								
64								
64								
64	Strap							
65		VTR	PWR		PWR	PWR		

MEC141x								
VTQFP Pin#	Mux	Signal Name	Buffer Type	Default Buffer Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
114	Strap							
115	0	Reserved	Reserved		Reserved	Reserved		
115	Default: 1	ADC_VREF	ADC_VREF		ADC_VREF	ADC_VREF	No Gate	Note 18
115	2	Reserved	Reserved		Reserved	Reserved		
115	3	Reserved	Reserved		Reserved	Reserved		
115	Strap							
116	Default: 0	GPIO022	PIO	I-2	VTR	VTR/VCC	No Gate	
116	1	ADC5	I_AN		I_AN	I_AN	No Gate	Note 8
116	2	Reserved	Reserved		Reserved	Reserved		
116	3	Reserved	Reserved		Reserved	Reserved		
116	Strap							
117	Default: 0	GPIO023	PIO	I-2	VTR	VTR/VCC	No Gate	
117	1	ADC6	I_AN		I_AN	I_AN	No Gate	Note 8
117	2	A20M	PIO		VTR	VCC	Reserved	
117	3	Reserved	Reserved		Reserved	Reserved		
117	Strap							
118	Default: 0	GPIO024	PIO	I-2	VTR	VTR/VCC	No Gate	
118	1	ADC7	I_AN		I_AN	I_AN	No Gate	Note 8
118	2	Reserved	Reserved		Reserved	Reserved		
118	3	Reserved	Reserved		Reserved	Reserved		
118	Strap							
119	0	GPIO004	PIO		VBAT	VTR/VCC	No Gate	
119	Default: 1	BGPO	PIO	O-4 mA	VBAT	VBAT	Reserved	
119	2	Reserved	Reserved		Reserved	Reserved		
119	3	Reserved	Reserved		Reserved	Reserved		
119	Strap							
120	0	GPIO003	PIO		VBAT	VTR/VCC	No Gate	
120	Default: 1	SYSPWR_PRES	ILLK	ILLK-4	VBAT	VBAT	Low	Note 12
120	2	Reserved	Reserved		Reserved	Reserved		
120	3	Reserved	Reserved		Reserved	Reserved		
120	Strap							
121	0	GPIO036	PIO		VBAT	VTR/VCC	No Gate	
121	Default: 1	VCI_OUT	PIO	O-8 mA	VBAT	VBAT	Reserved	
121	2	Reserved	Reserved		Reserved	Reserved		
121	3	Reserved	Reserved		Reserved	Reserved		
121	Strap							
122		VBAT	PWR		PWR	PWR		
122								
122								
122								
122	Strap							
123	Default: 0	XTAL1	OCLK	OCLK	VBAT	VBAT	No Gate	

TABLE 4-2: SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
LAD2	Input/Output	Bit[2] of the LPC multiplexed command, address, and data bus.
LAD3	Input/Output	Bit[3] of the LPC multiplexed command, address, and data bus.
LFRAME#	Input	Active low signal indicates start of new cycle and termination of broken cycle.
LRESET#	Input	Active low signal used as LPC Interface Reset. Same as PCI Reset on host. **Note:** LRESET# is typically connected to the host PCI RESET (PCIRST#) signal.
LCLK	Input	PCI clock input (PCI_CLK)
SERIRQ	Input/Output	Serial IRQ pin used with the LCLK signal to transfer interrupts to the host.
CLKRUN#	Open-Drain Output	Clock Control for LCLK
LPCPD#	Input	Power Down: Indicates that the device should prepare for power to be removed from the LPC I/F.

4.4.2 REGISTER INTERFACES

The registers defined for the LPC Interface block are accessible by the various hosts as indicated in Section 4.9, "LPC Configuration Registers", Section 4.11, "EC-Only Registers"and Section 4.10, "Runtime Registers".

4.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

4.5.1 POWER DOMAINS

Name	Description
VTR	The LPC Interface block and registers are powered by VTR.

4.5.2 CLOCK INPUTS

Name	Description
LCLK	This LPC Interface has a single clock input, called LCLK.

Note: The PCI_CLK input to LCLK can run at 24MHz or 33MHz. When the PCI_CLK input is 24MHz the Handshake bit in the EC Clock Control Register must be set to a '1' to capture LPC transactions properly. See Section 4.11.4, "EC Clock Control Register," on page 123.

TABLE 4-8: LPC I/O REGISTER MAP (CONTINUED)

Logical Device	BAR LPC Host Address	Example BAR LPC Host Address	LPC Address Mask	Offsets Claimed	Register Name
ACPI EC2	8 Byte Boundary	0030h	7	BAR+0	ACPI_OS_DATA_BYTE_0
				+1	ACPI_OS_DATA_BYTE_1
				+2	ACPI_OS_DATA_BYTE_2
				+3	ACPI_OS_DATA_BYTE_3
				+4	Write: ACPI_OS_COMMAND Read: OS STATUS OS
				+5	OS Byte Control
				+6	Reserved
				+7	Reserved
ACPI EC3	8 Byte Boundary	0038h	7	BAR+0	ACPI_OS_DATA_BYTE_0
				+1	ACPI_OS_DATA_BYTE_1
				+2	ACPI_OS_DATA_BYTE_2
				+3	ACPI_OS_DATA_BYTE_3
				+4	Write: ACPI_OS_COMMAND Read: OS STATUS OS
				+5	OS Byte Control
				+6	Reserved
				+7	Reserved
Port 80 BIOS Debug Port 0	Any I/O Byte Address	0080h	0	BAR+0	Host Data
Port 80 BIOS Debug Port 1	Any I/O Byte Address	0081h	0	BAR+0	Host Data

4.8.2.2 Device Memory Transactions

LPC Memory cycles are single byte read or writes that occur in a 32-bit address range. The LPC block will claim a memory transaction that is targeted for one of these logical devices. A Device Memory Base Address Register has been implemented for the logical devices listed in Table 4-16, “Device Memory Base Address Registers,” on page 119

On every LPC bus Memory access all Base Address Registers are checked in parallel and if any matches the LPC memory address the LPC Interface claims the bus cycle. The memory address is claimed as described in I/O Transactions on page 101 except that the LPC memory cycle address is 32 bits instead of the 16 bit I/O cycle address.

Software should insure that no two BARs map the same LPC memory address. If two BARs do map to the same address, the BAR_CONFLICT bit in the Host Bus Error Register is set when an LPC access targeting the BAR Conflict address. An EC interrupt can be generated.

Each Device Memory BAR is 48 bits wide. The format of each Device Memory BAR is summarized in Device Memory Base Address Register Format. An LPC memory request is translated by the Device Memory BAR into an 8-bit read or write transaction on the AHB bus. The 32-bit LPC memory address is translated into a 32-bit AHB address.

The Base Address Register Table is itself part of the AHB address space. It resides in the Configuration quadrant of Logical Device Ch, the LPC Interface.

4.8.2.3 SRAM Memory Transactions

In addition to mapping LPC Memory transactions into Logical Devices, Memory transactions can be mapped into internal address space, as configured by the SRAM Memory BARs. LPC Memory cycles are single byte read or writes that occur in a 32-bit address range. The LPC block will claim LPC memory cycles that match the programmed SRAM Memory BAR Register if the VALID in the SRAM Memory BAR Configuration is set to 1. No memory cycles will be claimed if this bit is cleared.

TABLE 12-3: RUNTIME REGISTER SUMMARY

Offset	Register Name (Mnemonic)
00h	HOST-to-EC Mailbox Register
01h	EC-to-HOST Mailbox Register
02h	EC Address LSB Register
03h	EC Address MSB Register
04h	EC Data Byte 0 Register
05h	EC Data Byte 1 Register
06h	EC Data Byte 2 Register
07h	EC Data Byte 3 Register
08h	Interrupt Source LSB Register
09h	Interrupt Source MSB Register
0Ah	Interrupt Mask LSB Register
0Bh	Interrupt Mask MSB Register
0Ch	Application ID Register

12.9.1 HOST-TO-EC MAILBOX REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	HOST_EC_MBOX 8-bit mailbox used communicate information from the system host to the embedded controller. Writing this register generates an event to notify the embedded controller. The embedded controller has the option of clearing some or all of the bits in this register. This is dependent on the protocol layer implemented using the EMI Mailbox. The host must know this protocol to determine the meaning of the value that will be reported on a read. This bit field is aliased to the HOST_EC_MBOX bit field in the HOST-to-EC Mailbox Register	R/W	0h	nSYSRST

When the FOUR_BYTE_ACCESS (see Note) bit in the OS Byte Control Register is cleared to '0', the following access rules apply:

1. Writes to the ACPI OS Data Register Byte 0 Register sets the IBF bit in the OS STATUS OS Register.
2. Reads from the ACPI OS Data Register Byte 0 Register clears the OBF bit in the OS STATUS OS Register.
3. All writes to ACPI-OS DATA BYTES[3:1] complete without error but the data are not registered.
4. All reads from ACPI-OS DATA BYTES[3:1] return 00h without error.
5. Access to ACPI-OS DATA BYTES[3:1] has no effect on the IBF & OBF bits in the OS STATUS OS Register.

When the Four Byte Access bit in the OS Byte Control Register is set to '1', the following access rules apply (see **Note**):

1. Writes to the ACPI OS Data Register Byte 3 Register sets the IBF bit in the OS STATUS OS Register.
2. Reads from the ACPI OS Data Register Byte 3 Register clears the OBF bit in the OS STATUS OS Register.

Note:	In eSPI mode, instance 0 of the ACPI Embedded Controller Interface (ACPI-EC0) only operates in Legacy Mode which provides single byte Full Duplex operation. Four-byte Mode is not supported for ACPI-EC0 in eSPI mode.

14.12.2 ACPI OS DATA REGISTER BYTE 1 REGISTER

This register is aliased; see ACPI-OS DATA BYTES[3:0] on page 227, OS2EC DATA BYTES[3:0] on page 234, and EC2OS DATA BYTES[3:0] on page 236 for detailed description of access rules.

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OS_DATA_BYTE_1 This is byte 1 of the 32-bit ACPI-OS DATA BYTES[3:0].	R/W	0h	nSYSRST

14.12.3 ACPI OS DATA REGISTER BYTE 2 REGISTER

This register is aliased; see ACPI-OS DATA BYTES[3:0] on page 227, OS2EC DATA BYTES[3:0] on page 234, and EC2OS DATA BYTES[3:0] on page 236 for detailed description of access rules.

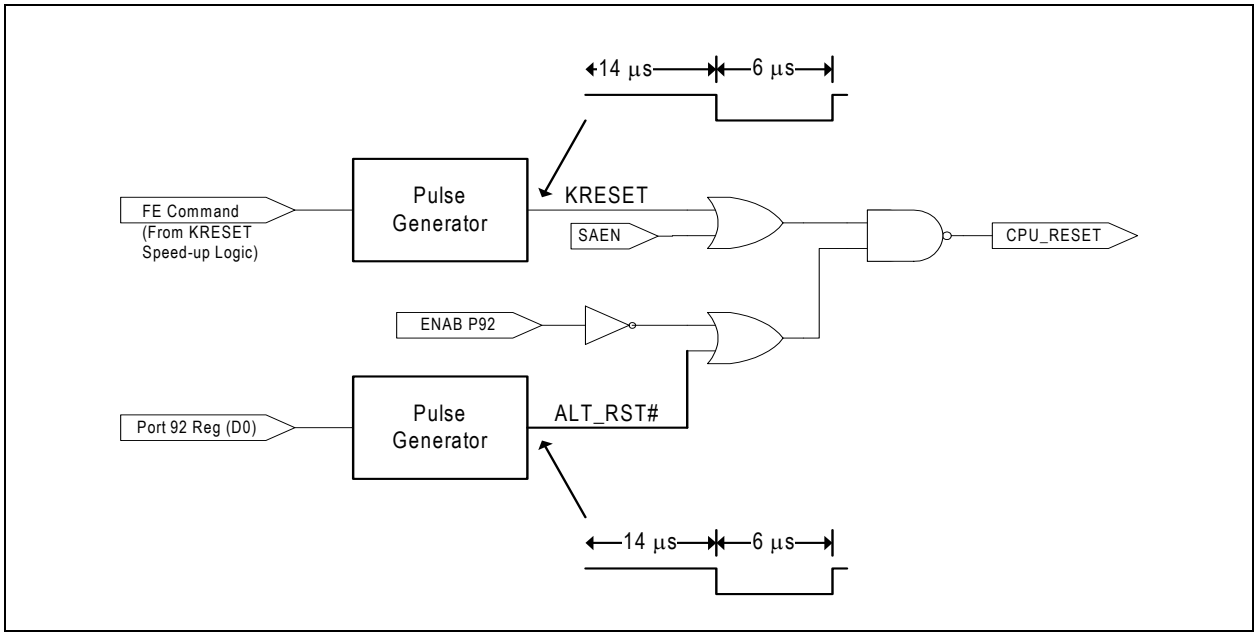
Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OS_DATA_BYTE_2 This is byte 2 of the 32-bit ACPI-OS DATA BYTES[3:0].	R/W	0h	nSYSRST

14.12.4 ACPI OS DATA REGISTER BYTE 3 REGISTER

This register is aliased; see ACPI-OS DATA BYTES[3:0] on page 227, OS2EC DATA BYTES[3:0] on page 234, and EC2OS DATA BYTES[3:0] on page 236 for detailed description of access rules.

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OS_DATA_BYTE_3 This is byte 3 of the 32-bit ACPI-OS DATA BYTES[3:0].	R/W	0h	nSYSRST

FIGURE 16-5: CPU_RESET IMPLEMENTATION DIAGRAM



16.12 Instance Description

There are two blocks defined in this chapter: Emulated 8042 Interface and the Legacy Port92/GATEA20 Support. The MEC140x/1x has one instance of each block.

16.13 Configuration Registers

The registers listed in the Configuration Register Summary table are for a single instance of the Emulated 8042 Interface. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the Configuration Register Base Address Table.

TABLE 16-5: CONFIGURATION REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Logical Device Number	Host	Address Space	Base Address
Emulated 8042 Interface	0	1	LPC	Configuration Port	INDEX = 00h
			EC	32-bit internal address space	000F_0700h

Each Configuration register access through the Host Access Port is via its LDN and its Host Access Port Index. EC access is a relative offset to the EC Base Address.

TABLE 16-6: CONFIGURATION REGISTER SUMMARY

Offset	Register Name (Mnemonic)
30h	Activate Register

TABLE 22-2: REGISTER SUMMARY (CONTINUED)

Offset	Register Name
3F8h	GPIO Lock 1
3FCh	GPIO Lock 0
500h	Reserved
504h - 51Ch	GPIO001-GPIO007 Pin Control Register 2
520h - 53Ch	GPIO010-GPIO017 Pin Control Register 2
540h - 55Ch	GPIO020-GPIO027 Pin Control Register 2
560h - 578h	GPIO030-GPIO036 Pin Control Register 2 (see Note 22-5 for limitations)
580h - 59Ch	GPIO040-GPIO047 Pin Control Register 2 (see Note 22-5 for limitations)
5A0h - 5BCh	GPIO050-GPIO057 Pin Control Register 2
5C0h - 5CCh	GPIO060-GPIO063 Pin Control Register 2 (see Note 22-5 for limitations)
5D0h	Reserved (GPIO064 not implemented - see Note 22-4)
5D4h - 5D8h	GPIO065-GPIO066 Pin Control Register 2
5DCh	Reserved (GPIO067 not implemented - see Note 22-4)
5E0h - 5F8h	Reserved (GPIO070-GPIO076 not implemented)
5E0h - 5FCh	GPIO100-GPIO107 Pin Control Register 2
600h - 61Ch	GPIO110-GPIO117 Pin Control Register 2
620h - 63Ch	GPIO120-GPIO127 Pin Control Register 2
640h - 658h	GPIO130-GPIO136 Pin Control Register 2
660h - 67Ch	GPIO140-GPIO147 Pin Control Register 2
680h - 69Ch	GPIO150-GPIO157 Pin Control Register 2
6A0h - 6B8h	GPIO160-GPIO166 Pin Control Register 2

Note 22-3 The GPIO input and output registers are LPC I/O accessible via Region 0 of the EMI block. This access is defined in the EMI Protocols chapter of the firmware specification.

Note 22-4 There is no Pin Control Register 2 for GPIO064 and GPIO067, which are PCI_PIO buffer type pins. The drive strength and slew rate are not configurable on these pins.

Note 22-5 The drive strength and slew rate are not configurable for the LPC functions on GPIO034, GPIO061, GPIO063, and GPIO40 - GPIO044 since they are controlled by the PCI_PIO type buffers.

26.6 Host Interface

The registers defined for the Tachometer are accessible by the various hosts as indicated in Section 26.11, "EC-Only Registers".

26.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

26.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

26.7.2 CLOCK INPUTS

Name	Description
100kHz_Clk	This is the clock input to the tachometer monitor logic. In Mode 1, the TACHx input is measured in the number of these clocks.

26.7.3 RESETS

Name	Description
nSYSRST	This signal resets all the registers and logic in this block to their default state.

26.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
TACH	This internal signal is generated from the OR'd result of the status events, as defined in the TACHx Status Register.

26.9 Low Power Modes

The Tachometer may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

26.10 Description

The Tachometer block monitors tachometer output signals (also referred to as TACH signals) or locked rotor signals generated by various types of fans. These signals can be used to determine the speed of the attached fan. This block is designed to monitor fans at fan speeds from 100 RPMs to 30,000 RPMs.

Typically, these are DC brushless fans that generate (with each revolution) a 50% duty cycle, two-period square wave, as shown in FIGURE 26-2: below.

29.12 PS/2 Port Physical Layer Byte Transmission Protocol

The PS/2 physical layer transfers a byte of data via an eleven bit serial stream as shown in TABLE 29-2:. A logic 1 is sent at an active high level. Data sent from a Keyboard or mouse device to the host is read on the falling edge of the clock signal. The Keyboard or mouse device always generates the clock signal. The Host may inhibit communication by pulling the Clock line low. The Clock line must be continuously high for at least 50 microseconds before the Keyboard or mouse device can begin to transmit its data. See Table 29-3, "PS/2 Port Physical Layer Bus States".

TABLE 29-2: PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

Bit	Function
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd parity)
11	Stop Bit (always 1)

FIGURE 29-3: PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

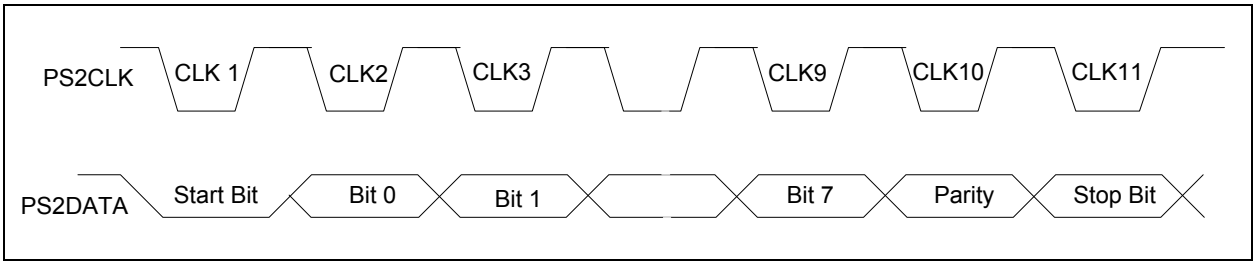


TABLE 29-3: PS/2 PORT PHYSICAL LAYER BUS STATES

Data	Clock	State
high	high	Idle
high	low	Communication Inhibited
low	low	Request to Send

37.6 Interrupts

TABLE 37-5: EC INTERRUPTS

Source	Description
VCI_IN0	This interrupt is routed to the Interrupt Controller It is only asserted when both VBAT and VTR are powered. Edge detection and assertion level for the interrupt are configured in the GPIO Pin Control Register for the GPIO that shares the pin with VCI_IN# input. This interrupt is equivalent to the GPIO interrupt for the GPIO that shares the pin, but appears on a different register in the Interrupt Aggregator.
VCI_IN1	This interrupt is routed to the Interrupt Controller It is only asserted when both VBAT and VTR are powered. Edge detection and assertion level for the interrupt are configured in the GPIO Pin Control Register for the GPIO that shares the pin with VCI_IN# input. This interrupt is equivalent to the GPIO interrupt for the GPIO that shares the pin, but appears on a different register in the Interrupt Aggregator.
VCI_OVRD_IN	This interrupt is routed to the Interrupt Controller It is only asserted when both VBAT and VTR are powered. Edge detection and assertion level for the interrupt are configured in the GPIO Pin Control Register for the GPIO that shares the pin with VCI_OVRD_IN input. This interrupt is equivalent to the GPIO interrupt for the GPIO that shares the pin, but appears on a different register in the Interrupt Aggregator.

37.7 Low Power Modes

The VBAT-powered Control Interface has no low-power modes. It runs continuously while the VBAT well is powered.

37.8 General Description

The VBAT-Powered Control Interface (VCI) is used to drive the VCI_OUT pin. The output pin can be controlled either by VBAT-powered inputs, or by firmware when the VTR is active and the EC is powered and running. When the VCI_OUT pin is controlled by hardware, either because VTR is inactive or because the VCI block is configured for hardware control, the VCI_OUT pin can be asserted by a number of inputs:

- When either the VCI_IN0# pin or the VCI_IN1# is asserted. By default, the VCI_IN# pins are active low, but firmware can switch each input individually to an active-high input. See Section 37.8.1, "Input Polarity".
- Wen the VCI_OVRD_IN pin is asserted. The VCI_OVRD_IN pin is always active high
- When the POWER_UP_EVENT from the RTC/Week Timer is asserted

Firmware can configure which of the hardware pin inputs contribute to the VCI_OUT output by setting the enable bits in the VCI Input Enable Register. Even if the input pins are not configured to affect VCI_OUT, firmware can monitor their current state through the status bits in the VCI Register. Firmware can also enable EC interrupts from the state of the input pins.

Each of the VCI_IN# pins can be configured for additional properties.

- By default, each of the VCI_IN# pins have an input glitch filter. All glitch filters can be disabled by the FILTERS_BYPASS bit in the VCI Register
- Assertions of each of the VCI_IN# pins can optionally be latched, so hardware can maintain the assertion of a VCI_IN# even after the physical pin is de-asserted, or so that firmware can determine which of the VCI_IN# inputs contributed to VCI_OUT assertion. See the Latch Enable Register and the Latch Resets Register.
- Rising edges and falling edges on the VCI_IN# pins are latched, so firmware can detect transitions on the VCI_IN# pins even if the transitions occurred while EC power was not available. See Section 37.8.2, "Edge Event Status".

When VTR power is present and the EC is operating, firmware can figure the VCI_OUT pin to operate as a general-purpose output pin. The VCI_OUT pin is firmware-controlled when the FW_EXT bit in the VCI Register is ‘1’. When firmware is controlling the output, the state of VCI_OUT is defined by the VCI_FW_CNTRL bit in the same register. When VTR is not present (the VTRGD input is low), the VCI_OUT pin is also determined by the hardware circuit.

38.8 Interrupts

Source	Description
ADC_Single_Int	Interrupt signal from ADC controller to EC for Single-Sample ADC conversion.
ADC_Repeat_Int	Interrupt signal from ADC controller to EC for Repeated ADC conversion.

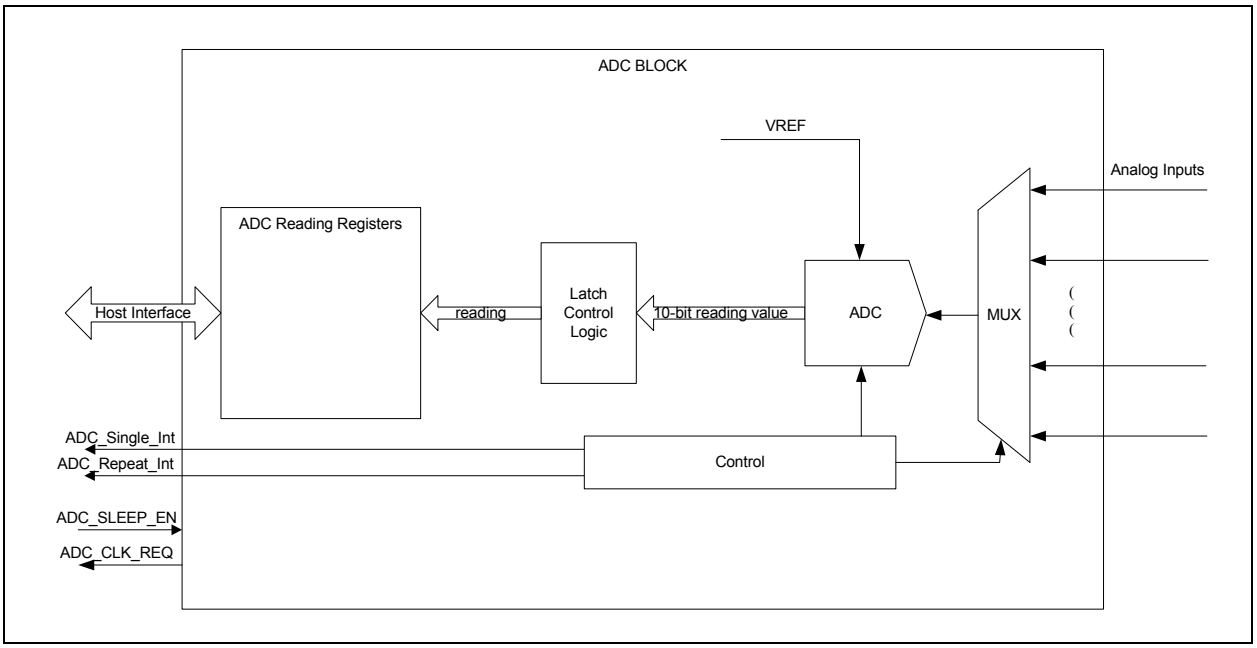
38.9 Low Power Modes

The ADC may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

The ADC is designed to conserve power when it is either sleeping or disabled. It is disabled via the Activate Bit and sleeps when the ADC_SLEEP_EN signal is asserted. The sleeping state only controls clocking in the ADC and does not power down the analog circuitry. For lowest power consumption, the ADC Activate bit must be set to '0.'

38.10 Description

FIGURE 38-2: ADC BLOCK DIAGRAM



The MEC140x/1x features successive approximation Analog to Digital Converter with up to sixteen channels. The ADC architecture features excellent linearity and converts analog signals to 10 bit words. Conversion takes less than 12 microseconds per 10-bit word. The sixteen channels are implemented with a single high speed ADC fed by a sixteen input analog multiplexer. The multiplexer cycles through the sixteen voltage channels, starting with the lowest-numbered channel and proceeding to the highest-number channel, selecting only those channels that are programmed to be active.

The input range on the voltage channels spans from 0V to the external voltage reference. With an external voltage reference of 3.0V, this provides resolutions of 2.9mV. The accuracy of any voltage reading depends on the accuracy and stability of the voltage reference input.

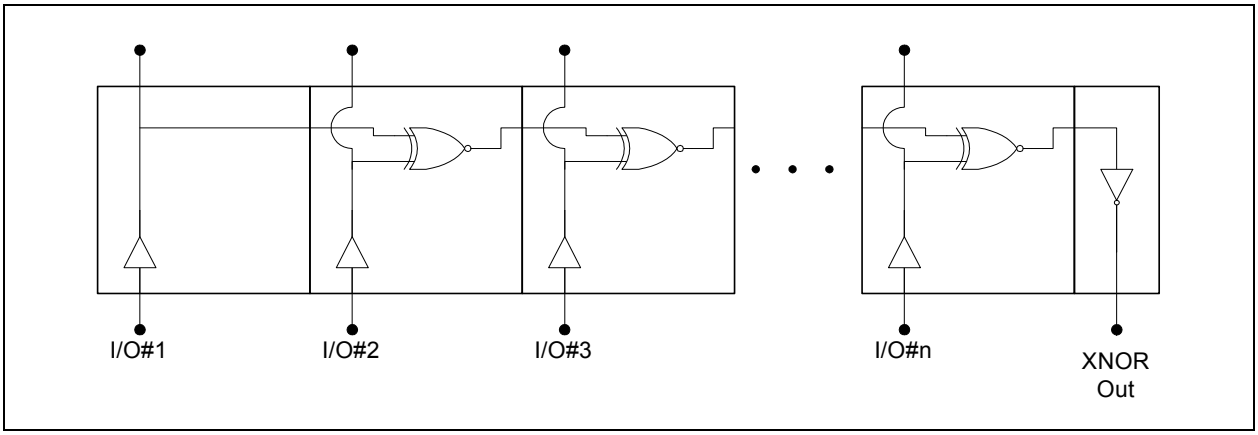
Note: The ADC pins are 3.3V tolerant.

41.5.2 EXCLUDED PINS

All pins in the pinout are included in the XNOR chain, except the following:

- Power Pins (VTR, VTR_33_18, VBAT, VREF_CPU)
- Ground Pins (VSS, AVSS, VSS_VBAT)
- Voltage Regulator Capacitor (VR_CAP)
- Crystal pins (XTAL1, XTAL2)
- Test Output Pin (XNOR_OUT): GPIO027/KSO00/PVT_IO1
- Pins (ICSP_MCLR)

FIGURE 41-2: XNOR CHAIN TEST STRUCTURE



41.5.3 TEST PROCEDURE

41.5.3.1 Setup

Warning: Ensure power supply is off during Setup.

1. Connect ICSP_MCLR to ground.
2. Connect the VSS, AVSS, VSS_VBAT pins to ground.
3. Connect the VTR, VTR_33_18, VBAT pins to an unpowered 3.3V power source.
4. Connect the VREF_CPU pin to an unpowered 1.8V power source.
5. Connect an oscilloscope or voltmeter to the Test Output pin.
6. All other pins should be tied to ground.

Note:	There are 107 pins in the XNOR Chain in the 128-pin package.

41.5.3.2 Testing

1. Turn on the 3.3V power source.
2. Enable the XNOR Chain as defined in Section 38.5.3.3, "Procedure to Enable the XNOR Chain".

Note:	Note that at this point all inputs to the XNOR Chain are low, except for the ICSP_MCLR pin, and the output on the Test Output pin is non-inverted from its initial state, which is dependent on the number of pins in the chain. If the number of input pins in the chain is an even number, the initial state of the Test Output Pin (XNOR_OUT): GPIO027/KSO00/PVT_IO1 is low. If the number of input pins in the chain is an odd number, the initial state of the Test Output Pin (XNOR_OUT): GPIO027/KSO00/PVT_IO1 is high.

42.2.7 COMPARATOR ELECTRICAL CHARACTERISTICS

TABLE 42-11: AC AND DC CHARACTERISTICS: COMPARATOR

CHARACTERISTICS		Standard Operating Conditions (unless otherwise noted)				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
V_{IN}	Input Voltage Range	0	-	VTR	V	
V_{HYST}	Input Hysteresis Voltage	15	30	45	mV	
CMRR	Common mode rejection ratio	44	-	-	dB	
T_{RESP}	Large signal response time	—	100	160	ns	VCM = VDD/2 100 mV step
TS_{RESP}	Small signal response time	—	160	320	ns	VCM = VDD/2 100 mV step
T_{ON}	Comparator Enable to Valid Output	—	—	0.1	µS	Note 42-6

Note 42-6 To prevent getting glitches on the comparator output, it is recommended to enable the comparator and wait for the output to be valid and stable before configuring the pin for the CMP_VOUTx function.

42.2.8 THERMAL CHARACTERISTICS

TABLE 42-12: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Consumer Temperature Devices					
Operating Junction Temperature Range	TJ	—	—	+125 (Note 1)	°C
Operating Ambient Temperature Range - Commercial	TA	0	—	+70	°C
Operating Ambient Temperature Range - Industrial	TA	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VTR x IVTR from Table 42-14 and Table 42-15 (e.g., 3.45V x 12.50mA = 43mW)	PD	PINT + PI/O			W
I/O Pin Power Dissipation: I/O = S (({VTR– VOH} x IOH) + S (VOL x IOL))					
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W
Note 1: TJ Max value is at ambient of 70°C					

TABLE 42-13: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 128-pin VTQFP	θJA	51.0	—	°C/W	1
	θJC	25.0	—	°C/W	1
Package Thermal Resistance, 144-pin WFBGA	θJA	50.0	—	°C/W	1
	θJC	17.0	—	°C/W	1
Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) and Junction to case thermal resistance, Theta-JC (θJC) numbers are achieved by package simulations.					

TABLE 44-1: REGISTER MEMORY MAP (CONTINUED)

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
1818	SMB Device Interface	0	SMB_EC_Only	DATA_TIMING2	1
1819	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1820	SMB Device Interface	0	SMB_EC_Only	Completion Register	4
1824	SMB Device Interface	0	SMB_EC_Only	Idle Scaling Register	4
1828	SMB Device Interface	0	SMB_EC_Only	Configuration Register	4
182C	SMB Device Interface	0	SMB_EC_Only	Bus Clock Register	2
182E	SMB Device Interface	0	SMB_EC_Only	Reserved	2
1830	SMB Device Interface	0	SMB_EC_Only	Block ID Register	1
1831	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1834	SMB Device Interface	0	SMB_EC_Only	Revision Register	1
1835	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1838	SMB Device Interface	0	SMB_EC_Only	Bit-Bang Control Register	1
1839	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1840	SMB Device Interface	0	SMB_EC_Only	Data Timing Register	4
1844	SMB Device Interface	0	SMB_EC_Only	Time-Out Scaling Register	4
1848	SMB Device Interface	0	SMB_EC_Only	SMBus Slave Transmit Buffer Register	1
1849	SMB Device Interface	0	SMB_EC_Only	Reserved	3
184C	SMB Device Interface	0	SMB_EC_Only	SMBus Slave Receive Buffer Register	1
184D	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1850	SMB Device Interface	0	SMB_EC_Only	SMBus Master Transmit Bufer Register	1
1851	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1854	SMB Device Interface	0	SMB_EC_Only	SMBus Master Receive Buffer Register	1
1855	SMB Device Interface	0	SMB_EC_Only	Reserved	3
1860	SMB Device Interface	0	SMB_EC_Only	Wake Status register	4
1864	SMB Device Interface	0	SMB_EC_Only	Wake Enable register	4
2400	DMA	0	DMA Main	DMA Main Control Register	1
2401	DMA	0	DMA Main	DMA Reserved	3
2404	DMA	0	DMA Main	DMA AFIFO Data Register	4
2440	DMA	0	DMA_CH0	DMA Activate Register	4
2444	DMA	0	DMA_CH0	DMA Memory Start Address Register	4
2448	DMA	0	DMA_CH0	DMA Memory End Address Register	4
244C	DMA	0	DMA_CH0	AHB Address Register	4
2450	DMA	0	DMA_CH0	DMA Control Register	4
2454	DMA	0	DMA_CH0	DMA Channel Interrupt Status	4
2458	DMA	0	DMA_CH0	DMA Channel Interrupt Enable	4

TABLE 44-1: REGISTER MEMORY MAP (CONTINUED)

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
AC2E	SMB Device Interface	1	SMB_EC_Only	Reserved	2
AC30	SMB Device Interface	1	SMB_EC_Only	Block ID Register	1
AC31	SMB Device Interface	1	SMB_EC_Only	Reserved	3
AC34	SMB Device Interface	1	SMB_EC_Only	Revision Register	1
AC35	SMB Device Interface	1	SMB_EC_Only	Reserved	3
AC38	SMB Device Interface	1	SMB_EC_Only	Bit-Bang Control Register	1
AC39	SMB Device Interface	1	SMB_EC_Only	Reserved	3
AC40	SMB Device Interface	1	SMB_EC_Only	Data Timing Register	4
AC44	SMB Device Interface	1	SMB_EC_Only	Time-Out Scaling Register	4
AC48	SMB Device Interface	1	SMB_EC_Only	SMBus Slave Transmit Buffer Register	1
AC49	SMB Device Interface	1	SMB_EC_Only	Reserved	3
AC4C	SMB Device Interface	1	SMB_EC_Only	SMBus Slave Receive Buffer Register	1
AC4D	SMB Device Interface	1	SMB_EC_Only	Reserved	3
AC50	SMB Device Interface	1	SMB_EC_Only	SMBus Master Transmit Bufer Register	1
AC51	SMB Device Interface	1	SMB_EC_Only	Reserved	3
AC54	SMB Device Interface	1	SMB_EC_Only	SMBus Master Receive Buffer Register	1
AC55	SMB Device Interface	1	SMB_EC_Only	Reserved	3
AC60	SMB Device Interface	1	SMB_EC_Only	Wake Status register	4
AC64	SMB Device Interface	1	SMB_EC_Only	Wake Enable register	4
B000	SMB Device Interface	2	SMB_EC_Only	Control Register	1
B000	SMB Device Interface	2	SMB_EC_Only	Status Register	1
B001	SMB Device Interface	2	SMB_EC_Only	Reserved	3
B004	SMB Device Interface	2	SMB_EC_Only	Own Address Register	2
B006	SMB Device Interface	2	SMB_EC_Only	Reserved	2
B008	SMB Device Interface	2	SMB_EC_Only	Data	1
B009	SMB Device Interface	2	SMB_EC_Only	Reserved	3
B00C	SMB Device Interface	2	SMB_EC_Only	SMBus Master Command Register	4
B010	SMB Device Interface	2	SMB_EC_Only	SMBus Slave Command Register	4
B014	SMB Device Interface	2	SMB_EC_Only	PEC Register	1
B015	SMB Device Interface	2	SMB_EC_Only	Reserved	3
B018	SMB Device Interface	2	SMB_EC_Only	DATA_TIMING2	1
B019	SMB Device Interface	2	SMB_EC_Only	Reserved	3
B020	SMB Device Interface	2	SMB_EC_Only	Completion Register	4
B024	SMB Device Interface	2	SMB_EC_Only	Idle Scaling Register	4
B028	SMB Device Interface	2	SMB_EC_Only	Configuration Register	4

TABLE 44-1: REGISTER MEMORY MAP (CONTINUED)

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
1FFFC 068	JTVIC	0	JTVIC Registers	GIRQ14 Enable Clear Register	4
1FFFC 070	JTVIC	0	JTVIC Registers	GIRQ15 Source Register	4
1FFFC 074	JTVIC	0	JTVIC Registers	GIRQ15 Enable Set Register	4
1FFFC 078	JTVIC	0	JTVIC Registers	GIRQ15 Enable Clear Register	4
1FFFC 07C	JTVIC	0	JTVIC Registers	GIRQ15 Result Register	4
1FFFC 080	JTVIC	0	JTVIC Registers	GIRQ16 Source Register	4
1FFFC 084	JTVIC	0	JTVIC Registers	GIRQ16 Enable Set Register	4
1FFFC 088	JTVIC	0	JTVIC Registers	GIRQ16 Enable Clear Register	4
1FFFC 08C	JTVIC	0	JTVIC Registers	GIRQ16 Result Register	4
1FFFC 090	JTVIC	0	JTVIC Registers	GIRQ17 Source Register	4
1FFFC 094	JTVIC	0	JTVIC Registers	GIRQ17 Enable Set Register	4
1FFFC 098	JTVIC	0	JTVIC Registers	GIRQ17 Enable Clear Register	4
1FFFC 09C	JTVIC	0	JTVIC Registers	GIRQ17 Result Register	4
1FFFC 0A0	JTVIC	0	JTVIC Registers	GIRQ18 Source Register	4
1FFFC 0A4	JTVIC	0	JTVIC Registers	GIRQ18 Enable Set Register	4
1FFFC 0A8	JTVIC	0	JTVIC Registers	GIRQ18 Enable Clear Register	4
1FFFC 0AC	JTVIC	0	JTVIC Registers	GIRQ18 Result Register	4
1FFFC 0B0	JTVIC	0	JTVIC Registers	GIRQ19 Source Register	4
1FFFC 0B4	JTVIC	0	JTVIC Registers	GIRQ19 Enable Set Register	4
1FFFC 0B8	JTVIC	0	JTVIC Registers	GIRQ19 Enable Clear Register	4
1FFFC 0BC	JTVIC	0	JTVIC Registers	GIRQ19 Result Register	4
1FFFC 0C0	JTVIC	0	JTVIC Registers	GIRQ20 Source Register	4
1FFFC 0C4	JTVIC	0	JTVIC Registers	GIRQ20 Enable Set Register	4

TABLE 44-1: REGISTER MEMORY MAP (CONTINUED)

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
1FFFC 360	JTVIC	0	JTVIC Registers	GIRQ14 [7:0] Interrupt Priority Register	4
1FFFC 364	JTVIC	0	JTVIC Registers	GIRQ14 [15:8] Interrupt Priority Register	4
1FFFC 368	JTVIC	0	JTVIC Registers	GIRQ14 [23:16] Interrupt Priority Register	4
1FFFC 36C	JTVIC	0	JTVIC Registers	GIRQ14 [31:24] Interrupt Priority Register	4
1FFFC 370	JTVIC	0	JTVIC Registers	GIRQ15 [7:0] Interrupt Priority Register	4
1FFFC 374	JTVIC	0	JTVIC Registers	GIRQ15 [15:8] Interrupt Priority Register	4
1FFFC 378	JTVIC	0	JTVIC Registers	GIRQ15 [23:16] Interrupt Priority Register	4
1FFFC 37C	JTVIC	0	JTVIC Registers	GIRQ15 [31:24] Interrupt Priority Register	4
1FFFC 380	JTVIC	0	JTVIC Registers	GIRQ16 [7:0] Interrupt Priority Register	4
1FFFC 384	JTVIC	0	JTVIC Registers	GIRQ16 [15:8] Interrupt Priority Register	4
1FFFC 388	JTVIC	0	JTVIC Registers	GIRQ16 [23:16] Interrupt Priority Register	4
1FFFC 38C	JTVIC	0	JTVIC Registers	GIRQ16 [31:24] Interrupt Priority Register	4
1FFFC 390	JTVIC	0	JTVIC Registers	GIRQ17 [7:0] Interrupt Priority Register	4
1FFFC 394	JTVIC	0	JTVIC Registers	GIRQ17 [15:8] Interrupt Priority Register	4
1FFFC 398	JTVIC	0	JTVIC Registers	GIRQ17 [23:16] Interrupt Priority Register	4
1FFFC 39C	JTVIC	0	JTVIC Registers	GIRQ17 [31:24] Interrupt Priority Register	4
1FFFC 3A0	JTVIC	0	JTVIC Registers	GIRQ18 [7:0] Interrupt Priority Register	4
1FFFC 3A4	JTVIC	0	JTVIC Registers	GIRQ18 [15:8] Interrupt Priority Register	4
1FFFC 3A8	JTVIC	0	JTVIC Registers	GIRQ18 [23:16] Interrupt Priority Register	4
1FFFC 3AC	JTVIC	0	JTVIC Registers	GIRQ18 [31:24] Interrupt Priority Register	4
1FFFC 3B0	JTVIC	0	JTVIC Registers	GIRQ19 [7:0] Interrupt Priority Register	4
1FFFC 3B4	JTVIC	0	JTVIC Registers	GIRQ19 [15:8] Interrupt Priority Register	4
1FFFC 3B8	JTVIC	0	JTVIC Registers	GIRQ19 [23:16] Interrupt Priority Register	4