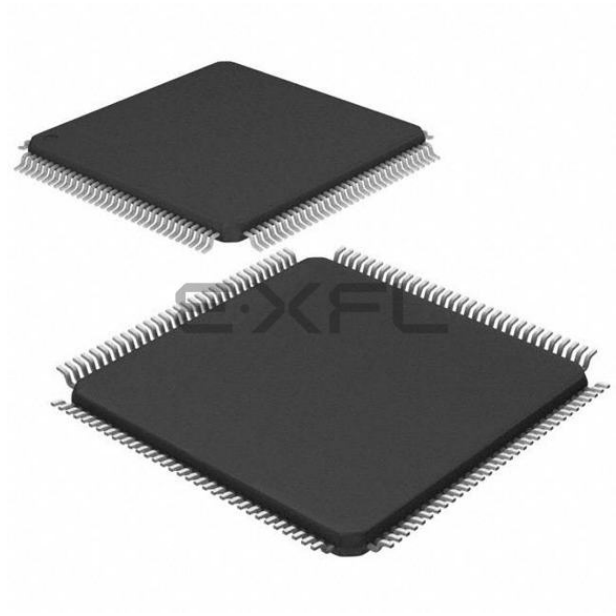

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	MIPS32® M14K™
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	128KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1414-nu

- GPIO061 Pin Control Register = 0x1000; //ALT FUNC1 – LPC_PD_N
- GPIO063 Pin Control Register = 0x1000; //ALT FUNC1 – SER_IRQ
- GPIO064 Pin Control Register = 0x1000; //ALT FUNC1 – PCI_RESET
- GPIO067 Pin Control Register = 0x1000; //ALT FUNC1 – CLKRUN
- LPC Interface (Configuration Port) BAR = 0x002E_8C01; //set bit 15
- LPC Activate Register = 0x01;

1.2.2 CONFIGURE ESPI INTERFACE

The downloaded firmware must configure the GPIO Pin Control registers for the eSPI alternate function, configure the eSPI I/O Component (Configuration Port) Base Address Register (BAR), and activate the eSPI block.

Example:

- GPIO034 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_CLK
- GPIO044 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_CS#
- GPIO040 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO0
- GPIO041 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO1
- GPIO042 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO2
- GPIO043 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO3
- GPIO063 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_ALERT#
- GPIO061 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_RESET#
- eSPI I/O Component (Configuration Port) BAR = 0x002E_0001; //set bit 15
- eSPI Activate Register = 0x01;

1.2.3 CONFIGURE I2C INTERFACE

Similar to the LPC and eSPI interfaces, the downloaded firmware must configure the GPIO Pin Control registers for the SMBus alternate function and activate the associated SMB/I2C Controller.

1.3 Initialize Peripheral Interfaces

This will be system dependent, however, this section outlines some recommendations when enabling certain interfaces.

1.3.1 KEYBOARD SCAN INTERFACE

The Keyboard Scan Interface has been multiplexed onto GPIO pins. Internal pull-up resistors, enabled via the GPIO Pin Control Registers", may be used on the KSI and KSO pins instead of external pull-ups. However, if internal pull-ups are used then the PreDrive Mode must be enabled. The GPIO Pin Control register format is defined in Section 22.6.1.1, "Pin Control Register," on page 329. The PreDrive Mode is defined in Section 30.10.2, "PreDrive Mode," on page 406.

1.4 System Block Diagrams

Note: Not all features shown are available on all devices. Refer to Products on page 3 for a list of the features by device.

MEC141x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
	J9	VSS
	K13	VSS
	E5	No Connect
	E6	No Connect
	E7	No Connect
	E8	No Connect
	E9	No Connect
	F5	No Connect
	F6	No Connect
	F7	No Connect
	F8	No Connect
	F9	No Connect
	G8	No Connect
	L8	No Connect

2.5 Non 5 Volt Tolerant Pins

There are no 5 Volt tolerant pins in the MEC140x/1x.

2.6 1.8V or 3.3V I/O Pins

The following signals are powered by the VTR_33_18 power supply. This supply determines the operating voltage range for these signals.

Note: The LPC Interface signals require the VTR_33_18 power pin to be connected to the 3.3V VTR rail. The eSPI Interface signals require the VTR_33_18 power pin to be connected to the 1.8V rail. The GPIO signals on these pins may operate at either 1.8V or 3.3V.

- GPIO061/LPCPD#/ESPI_RESET#
- VTR_33_18
- GPIO063/SER_IRQ/ESPI_ALERT#
- GPIO064/LRESET#
- GPIO034/PCI_CLK/ESPI_CLK
- GPIO044/LFRAME#/ESPI_CS#
- GPIO040/LAD0/ESPI_IO0
- GPIO041/LAD1/ESPI_IO1
- GPIO042/LAD2/ESPI_IO2
- GPIO043/LAD3/ESPI_IO3
- GPIO067/CLKRUN#

2.7 POR Glitch Protected Pins

All pins have POR output glitch protection. POR output glitch protection ensures that pins will have a steady-state output during a VTR POR.

MEC140x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
61	Default: 0	GPIO042	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
61	1	LAD2	PCI_IO		VTR	VCC	High	Note 1
61	2	Reserved	Reserved		Reserved	Reserved		
61	3	Reserved	Reserved		Reserved	Reserved		
61	Strap							
62	Default: 0	GPIO043	PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
62	1	LAD3	PCI_IO		VTR	VCC	High	Note 1
62	2	Reserved	Reserved		Reserved	Reserved		
62	3	Reserved	Reserved		Reserved	Reserved		
62	Strap							
63	Default: 0	GPIO067	PCI_PIO	I-4	VTR_33_18	VTR/VCC	No Gate	
63	1	CLKRUN#	PCI_IO		VTR	VCC	Low	
63	2	Reserved	Reserved		Reserved	Reserved		
63	3	Reserved	Reserved		Reserved	Reserved		
63	Strap							
64		VSS	PWR		PWR	PWR		
64								
64								
64								
64	Strap							
65		VTR	PWR		PWR	PWR		
65								
65								
65								
65	Strap							
66	Default: 0	GPIO100	PIO	I-4	VTR	VTR/VCC	No Gate	
66	1	nEC_SCI	PIO		VTR	VTR	Reserved	
66	2	Reserved	Reserved		Reserved	Reserved		
66	3	Reserved	Reserved		Reserved	Reserved		
66	Strap							
67	Default: 0	GPIO101	PIO	I-4	VTR	VTR/VCC	No Gate	
67	1	SPI_CLK	PIO		VTR	VTR	Reserved	
67	2	Reserved	Reserved		Reserved	Reserved		
67	3	Reserved	Reserved		Reserved	Reserved		
67	Strap							
68	Default: 0	GPIO102	PIO	I-4	VTR	VTR/VCC	No Gate	
68	1	KSO09	PIO		VTR	VTR	Reserved	Note 15
68	2	Reserved	Reserved		Reserved	Reserved		
68	3	Reserved	Reserved		Reserved	Reserved		
68	Strap	CR_STRAP						
69	Default: 0	GPIO103	PIO	I-4	VTR	VTR/VCC	No Gate	
69	1	SPI_IO0	PIO		VTR	VTR	Low	

MEC141x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
23	1	DAC_0	O_AN		VTR	VTR	Reserved	
23	2	Reserved	Reserved		Reserved	Reserved		
23	3	Reserved	Reserved		Reserved	Reserved		
23	Strap							
24	Default: 0	GPIO161	PIO	I-4	VTR	VTR/VCC	No Gate	
24	1	DAC_1	O_AN		VTR	VTR	Reserved	
24	2	Reserved	Reserved		Reserved	Reserved		
24	3	Reserved	Reserved		Reserved	Reserved		
24	Strap							
25	Default: 0	GPIO165	PIO	I-4	VTR	VTR/VCC	No Gate	
25	1	CMP_VREF0	CMP_VREF		CMP_VREF	CMP_VREF	No Gate	
25	2	Reserved	Reserved		Reserved	Reserved		
25	3	Reserved	Reserved		Reserved	Reserved		
25	Strap							
26	Default: 0	GPIO166	PIO	I-4	VTR	VTR/VCC	No Gate	
26	1	CMP_VREF1	CMP_VREF		CMP_VREF	CMP_VREF	No Gate	
26	2	UART_CLK	PIO		VTR	VTR/VCC	Low	
26	3	Reserved	Reserved		Reserved	Reserved		
26	Strap							
27	Default: 0	GPIO123	PIO	I-4	VTR	VTR/VCC	No Gate	Note 16
27	1	SHD_CS#	PIO		VTR	VTR	Reserved	Note 10
27	2	Reserved	Reserved		Reserved	Reserved		
27	3	Reserved	Reserved		Reserved	Reserved		
27	Strap	BSS_STRAP						
28	Default: 0	GPIO133	PIO	I-4	VTR	VTR/VCC	No Gate	
28	1	SHD_IO0	PIO		VTR	VTR	Low	Note 10
28	2	Reserved	Reserved		Reserved	Reserved		
28	3	Reserved	Reserved		Reserved	Reserved		
28	Strap							
29	Default: 0	GPIO134	PIO	I-4	VTR	VTR/VCC	No Gate	
29	1	SHD_IO1	PIO		VTR	VTR	Low	Note 10
29	2	Reserved	Reserved		Reserved	Reserved		
29	3	Reserved	Reserved		Reserved	Reserved		
29	Strap							
30	Default: 0	GPIO135	PIO	I-4	VTR	VTR/VCC	No Gate	Note 17
30	1	SHD_IO2	PIO		VTR	VTR	Low	Note 10
30	2	Reserved	Reserved		Reserved	Reserved		
30	3	Reserved	Reserved		Reserved	Reserved		
30	Strap							
31	Default: 0	GPIO136	PIO	I-4	VTR	VTR/VCC	No Gate	
31	1	SHD_IO3	PIO		VTR	VTR	Low	Note 10
31	2	Reserved	Reserved		Reserved	Reserved		

4.9.2.1 SIRQ Configuration Register Format

Offset	See Table 4-14, “SIRQ Interrupt Configuration Register Map,” on page 114.			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	SELECT If this bit is 0, the first interrupt signal from the Logical Device is selected for the SERIRQ vector. If this bit is 1, the second interrupt signal from the Logical Device is selected. **Note:** The Keyboard Controller is an example of a Logical Devices that requires a second interrupt signal. Most Logical Devices require only a single interrupt and ignore this field as result.	R/W	Note 4-10	nSIO_ RESET
6	DEVICE This field should always be set to 0 in order to enable a SERIRQ.	R/W	Note 4-10	nSIO_ RESET
5:0	FRAME These six bits select the Logical Device for on-chip devices as the source for the interrupt. **Note:** The LPC Logical Device (Logical Device Number 0Ch) can be used by the Embedded Controller to generate a Serial Interrupt Request to the Host under software control.	R/W	Note 4-10	nSIO_ RESET

Note 4-10 See Table 4-14, “SIRQ Interrupt Configuration Register Map,” on page 114.

4.9.2.2 SIRQ Configuration Registers

TABLE 4-14: SIRQ INTERRUPT CONFIGURATION REGISTER MAP

Offset	Type	Reset	Configuration Register Name
40h	R/W	FFh	IRQ0
41h	R/W	FFh	IRQ1
42h	R/W	FFh	IRQ2
43h	R/W	FFh	IRQ3
44h	R/W	FFh	IRQ4
45h	R/W	FFh	IRQ5
46h	R/W	FFh	IRQ6
47h	R/W	FFh	IRQ7
48h	R/W	FFh	IRQ8
49h	R/W	FFh	IRQ9
4Ah	R/W	FFh	IRQ10
4Bh	R/W	FFh	IRQ11

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	BAR_CONFLICT This bit is set to 1 whenever a BAR conflict occurs on an LPC address. A Bar conflict occurs when more than one BAR matches the address during of an LPC cycle access. Once this bit is set, it remains set until cleared by being written with a 1.	R/WC	0h	nSYSRST
1	EN_INTERNAL_ERR When this bit is 0, only a BAR conflict, which occurs when two BARs match the same LPC I/O address, will cause LPC_INTERNAL_ERR to be set. When this bit is 1, internal bus errors will also cause LPC_INTERNAL_ERR to be set.	R/W	0h	nSYSRST
0	LPC_INTERNAL_ERR This bit is set whenever a BAR conflict or an internal bus error occurs as a result of an LPC access. Once set, it remains set until cleared by being written with a 1. This signal may be used to generate interrupts. See Section 4.6, "Interrupts," on page 98.	R/WC	0h	nSYSRST

4.11.3 EC SERIRQ REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	RESERVED	RES	-	-
0	EC_IRQ If the LPC Logical Device is selected as the source for a Serial Interrupt Request by an Interrupt Configuration register (see Section 4.8.4.8, "SERIRQ Interrupts," on page 110), this bit is used as the interrupt source.	R/W	0h	nSYSRST

4.11.4 EC CLOCK CONTROL REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	RESERVED	RES	-	-
2	Handshake This bit controls throughput of LPC transactions. When this bit is a ‘0’ the part supports a 33MHz PCI Clock. When this bit is a ‘1’, the part supports a PCI Clock from 24MHz to 33MHz.	RES	1h	nSYSRST

6.11.14 QMSPI DESCRIPTION BUFFER 3 REGISTER

The format for this register is the same as the format o the QMSPI Description Buffer 0 Register.

6.11.15 QMSPI DESCRIPTION BUFFER 4 REGISTER

The format for this register is the same as the format o the QMSPI Description Buffer 0 Register.

7.0 CHIP CONFIGURATION

7.1 Introduction

This chapter defines the mechanism to configure the device.

7.2 Terminology

This section documents terms used locally in this chapter. Common terminology that is used in the chip specification is captured in the Chip-Level Terminology section.

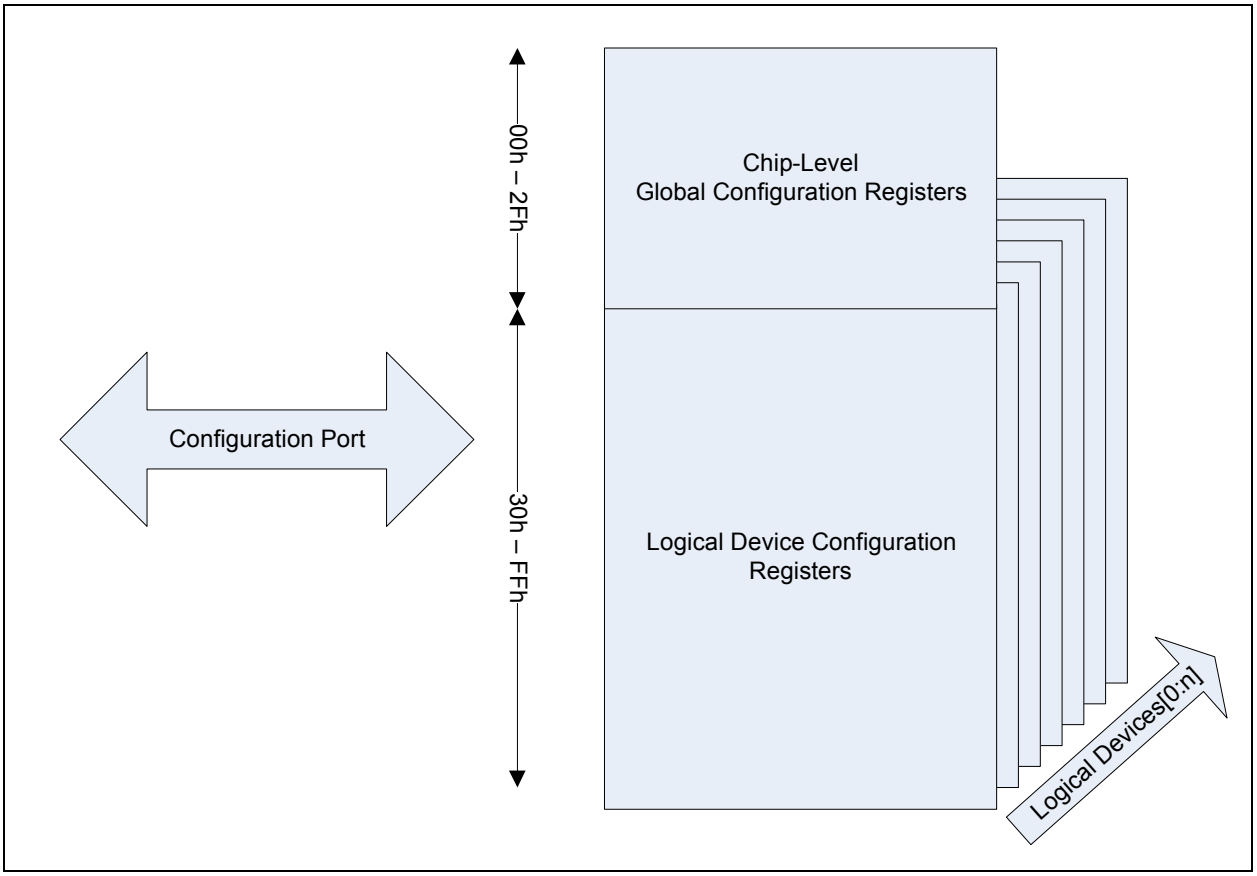
TABLE 7-1: TERMINOLOGY

Term	Definition
Global Configuration Registers	Registers used to configure the chip that are always accessible via the Configuration Port
Logical Device Configuration Registers	Registers used to configure a logical device in the chip. These registers are only accessible via the Configuration Port when enabled via the Global Configuration registers.

7.3 Interface

This block is designed to be accessed via the Host accessible Configuration Port.

FIGURE 7-1: BLOCK DIAGRAM OF CONFIGURATION PORT



8.7 Exceptions

Exceptions are synchronous to instructions, are not maskable, and have higher priority than interrupts.

Name	Description
Reset_Exception	The Reset_Exception is asserted when either an SI_RESET (i.e., Soft Reset) or a SI_ColdReset (i.e., POR) is asserted. Events that can cause a SI_RESET are a Soft Reset initiated by firmware or a WDT Event.
Debug_Exception	The Debug_Exception is asserted for an EJTAG command.
NMI	None - There are no NMI's implemented in this device.

8.8 Low Power Modes

The embedded controller may put itself and the chip into lower power states by configuring the chip's Sleep logic implemented in the chip's Power, Clocks, and Reset (PCR) circuitry and then executing the WAIT instruction.

The core provides two mechanisms for system-level, low-power support: Register-controlled power management and Instruction-controlled power management

8.8.1 REGISTER-CONTROLLED POWER MANAGEMENT

Register-Controlled Power Management is not supported.

8.8.2 INSTRUCTION-CONTROLLED POWER MANAGEMENT

In instruction-controlled power-down mode execution of the WAIT instruction is used to invoke low-power mode and put the chip into sleep mode. It stays in sleep mode until an interrupt or restart occurs. Power consumption is reduced during sleep mode since the pipeline ceases to change state, and the RAMs are disabled. More power reduction is achieved when clock gating option is used, whereby all non-essential clocks are switched off. The chip's Power, Clocks, and Reset (PCR) circuitry may be enabled to gate the clocks externally to the core when the embedded controller enters the sleep state.

8.9 Description

The block diagram shown in FIGURE 8-1: MIPS32 M14K Embedded Controller I/O Block Diagram on page 153 illustrates the IP configuration selected. This EC design includes the Fixed/Required M14K features, such as the Decode, Execution Unit, etc that are shaded light gray. The EC design has also opted to include the microMIPs instruction set and Debug capabilities. All other optional features have not been implemented.

The following sections define the optional features and configuration options selected. This chapter is intended to be used in combination with the MIPS documentation, such as the MIPS32® M14K™ Processor Core Software User's Manual, listed in the Section 8.2, "References," on page 152.

8.9.1 POWER ON RESET

Following a power on reset event the EC_PROC_RESET# signal is de-asserted and the embedded controller starts executing code from the first physical address of the Boot ROM.

8.9.2 INSTRUCTION SET

The M14K core defaults to the microMIPS instruction set and is runtime configurable as either microMIPS Instruction set.

This device does not support the following atomic instructions. A critical section should be used instead of these instructions. NOTE: A critical section will not protect a memory location from DMA access.

LL – Load Linked Word. LL and SC must be used together to implement an atomic transaction.

SC – Store Conditional Word

ACLR – Atomically Clear Bit within Byte

ASET - Atomically Set Bit within Byte

The device does not support the following interrupt return instruction. This instruction requires additional shadow register set. Use ERET instead.

IRET – Interrupt Return with automated interrupt epilog handling.

8.9.3 EJTAG HARDWARE DEBUG BREAK POINTS

This M14K core is configured for two data and four instruction breakpoints, without complex breakpoints

8.9.4 GENERAL PURPOSED REGISTER (GPR) SHADOW REGISTERS

The M14K core contains thirty-two 32-bit general-purpose registers used for integer operations and address calculation. No optional register sets were implemented.

8.9.5 MULTIPLY/DIVIDE UNIT (MDU)

This device is configured for the higher performance 32x16 array option.

8.9.6 SYSTEM CONTROL COPROCESSOR (CP0)

8.9.6.1 System Interface

The System Interface signals are defined in the Interfaces section. See Section 8.4.3, "System Interface," on page 154.

8.9.6.2 Interrupt Handling

This device is configured for External Interrupt Controller (EIC) mode.

8.9.7 MEMORY MANAGEMENT UNIT (MMU)

The M14K core implements a simple Fixed Mapping (FM) memory management unit.

TABLE 10-4: JTVIC REGISTER SUMMARY (CONTINUED)

Offset	Register Name
3CCh	GIRQ20 [31:24] Interrupt Priority Register
3D0h	GIRQ21 [7:0] Interrupt Priority Register
3D4h	GIRQ21 [15:8] Interrupt Priority Register
3D8h	GIRQ21 [23:16] Interrupt Priority Register
3DCh	GIRQ21 [31:24] Interrupt Priority Register
3E0h	GIRQ22 [7:0] Interrupt Priority Register
3E4h	GIRQ22 [15:8] Interrupt Priority Register
3E8h	GIRQ22 [23:16] Interrupt Priority Register
3ECh	GIRQ22 [31:24] Interrupt Priority Register
3F0h	GIRQ23 [7:0] Interrupt Priority Register
3F4h	GIRQ23 [15:8] Interrupt Priority Register
3F8h	GIRQ23 [23:16] Interrupt Priority Register
3FCh	GIRQ23 [31:24] Interrupt Priority Register
400h	GIRQ24 [7:0] Interrupt Priority Register
404h	GIRQ24 [15:8] Interrupt Priority Register
408h	GIRQ24 [23:16] Interrupt Priority Register
40Ch	GIRQ24 [31:24] Interrupt Priority Register
410h	GIRQ25 [7:0] Interrupt Priority Register
414h	GIRQ25 [15:8] Interrupt Priority Register
418h	GIRQ25 [23:16] Interrupt Priority Register
41Ch	GIRQ25 [31:24] Interrupt Priority Register
420h	GIRQ26 [7:0] Interrupt Priority Register
424h	GIRQ26 [15:8] Interrupt Priority Register
428h	GIRQ26 [23:16] Interrupt Priority Register
42Ch	GIRQ26 [31:24] Interrupt Priority Register
JTVIC Control Registers	
500h	JTVIC Control Register
504h	Interrupt Pending Register
508h	Aggregated Group Enable Set Register
50Ch	Aggregated Group Enabled Clear Register
510h	GIRQ Active Register

19.5 Power, Clocks and Resets

This section defines the Power, Clock, and Reset parameters of the block.

19.5.1 POWER DOMAINS

Name	Description
VTR	This power well sources all of the registers and logic in this block.

19.5.2 CLOCKS

This section describes all the clocks in the block, including those that are derived from the I/O Interface as well as the ones that are derived or generated internally.

Name	Description
32KHz_Clk	Timer Clock Source
48 MHz Ring Oscillator	System Clock used by Host Interface for register access

19.5.3 RESETS

Name	Description
nSYSRST	This power on reset (POR) signal resets all of the registers and logic in this block.

19.6 Interrupt Generation

This section defines the Interrupt Sources generated from this block.

Source	Description
RTOS_TIMER	**Note:** The RTOS Timer block generates a pulse anytime the RTOS Timer transitions from 1 to 0. This pulse is used to generate a wake-capable interrupt event that is latched by the Jump Table Vectored Interrupt Controller (JTVIC).

MEC141x						
GPIO Name (Octal)	**Pin Control Register Offset (Hex)**	**Pin Control Register Default (Hex)**	**Default Function**	**Pin Control Register 2 Offset (Hex)**	**Pin Control Register 2 Default (Hex)**	**Default Drive Strength (mA)**
GPIO014	0030	00001000	nRESET_IN	530	00000010	4
GPIO015	0034	00000000	GPIO015	534	00000010	4
GPIO016	0038	00000000	GPIO016	538	00000010	4
GPIO017	003C	00000000	GPIO017	53C	00000010	4
GPIO020	0040	00000000	GPIO020	540	00000010	4
GPIO021	0044	00000000	GPIO021	544	00000010	4
GPIO022	0048	00000000	GPIO022	548	00000000	2
GPIO023	004C	00000000	GPIO023	54C	00000000	2
GPIO024	0050	00000000	GPIO024	550	00000000	2
GPIO025	0054	00000000	GPIO025	554	00000010	4
GPIO026	0058	00000000	GPIO026	558	00000010	4
GPIO027	005C	00000000	GPIO027	55C	00000010	4
GPIO030	0060	00000000	GPIO030	560	00000010	4
GPIO031	0064	00000000	GPIO031	564	00000010	4
GPIO032	0068	00000000	GPIO032	568	00000010	4
GPIO033	006C	00000000	GPIO033	56C	00000010	4
GPIO034	0070	00000000	GPIO034	570	00000010	4
GPIO035	0074	00000000	GPIO035	574	00000010	4
GPIO036	0078	00001000	VCI_OUT	578	00000020	8
GPIO040	0080	00000000	GPIO040	580	00000010	4
GPIO041	0084	00000000	GPIO041	584	00000010	4
GPIO042	0088	00000000	GPIO042	588	00000010	4
GPIO043	008C	00000000	GPIO043	58C	00000010	4
GPIO044	0090	00000000	GPIO044	590	00000010	4
GPIO045	0094	00000000	GPIO045	594	00000010	4
GPIO046	0098	00000000	GPIO046	598	00000010	4
GPIO047	009C	00000000	GPIO047	59C	00000010	4
GPIO050	00A0	00000000	GPIO050	5A0	00000010	4
GPIO051	00A4	00000000	GPIO051	5A4	00000010	4
GPIO052	00A8	00000000	GPIO052	5A8	00000010	4
GPIO053	00AC	00000000	GPIO053	5AC	00000010	4
GPIO054	00B0	00000000	GPIO054	5B0	00000010	4
GPIO055	00B4	00000000	GPIO055	5B4	00000010	4
GPIO056	00B8	00000000	GPIO056	5B8	00000010	4
GPIO057	00BC	00000000	GPIO057	5BC	00000010	4
GPIO060	00C0	00000000	GPIO060	5C0	00000010	4
GPIO061	00C4	00000000	GPIO061	5C4	00000010	4
GPIO062	00C8	00000000	GPIO062	5C8	00000010	4
GPIO063	00CC	00000000	GPIO063	5CC	00000010	4
GPIO064	00D0	00000000	GPIO064	5D0	00000010	4
(GPIO065)	00D4	00001000	ADC_VREF	5D4	00000000	Reserved
(GPIO066)	00D8	00001000	DAC_VREF	5D8	00000010	Reserved

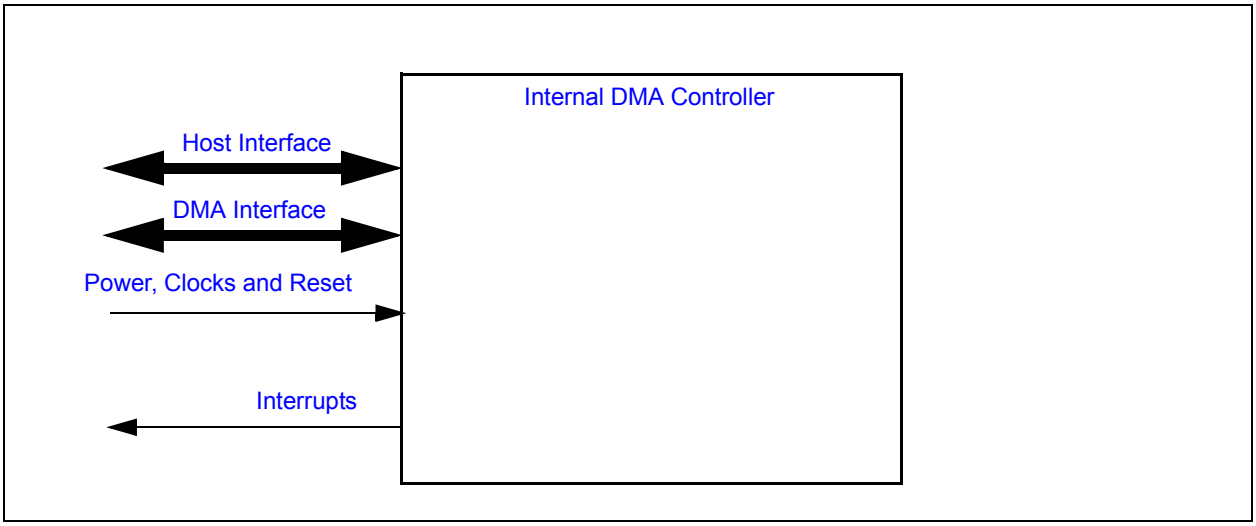
TABLE 24-1: TERMINOLOGY (CONTINUED)

Term	Definition
Source	The DMA Controller moves data from the Source to the Destination. The Source provides the data. The Source may be either the Master or Slave Controller.
Destination	The DMA Controller moves data from the Source to the Destination. The Destination receives the data. The Destination may be either the Master or Slave Controller.

24.5 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 24-1: INTERNAL DMA CONTROLLER I/O DIAGRAM



24.5.1 SIGNAL DESCRIPTION

This block doesn't have any external signals that may be routed to the pin interface. This DMA Controller is intended to be used internally to transfer large amounts of data without the embedded controller being actively involved in the transfer.

24.5.2 HOST INTERFACE

The registers defined for the Internal DMA Controller are accessible by the various hosts as indicated in Section 24.10, "DMA Main Registers".

24.5.3 DMA INTERFACE

Each DMA Master Device that may engage in a DMA transfer must have a compliant DMA interface. The following table lists the DMA Devices in the MEC140x/1x.

TABLE 24-2: DMA CONTROLLER DEVICE SELECTION

Device Name	Device Number (Note 1)	Controller Source
SMBus 0 Controller	0	Slave
	1	Master

25.0 PECI INTERFACE

25.1 Overview

The MEC140x/1x includes a PECI Interface to allow the EC to retrieve temperature readings from PECI-compliant devices. The PECI Interface implements the PHY and Link Layer of a PECI host controller as defined in References[1] and includes hardware support for the PECI 2.0 command set.

This chapter focuses on MEC140x/1x specific PECI Interface configuration information such as Power Domains, Clock Inputs, Resets, Interrupts, and other chip specific information. For a functional description of the MEC140x/1x PECI Interface refer to References [1].

25.2 References

1. PECI Interface Core, Rev. 1.31, Core-Level Architecture Specification, SMSC Confidential, 4/15/11

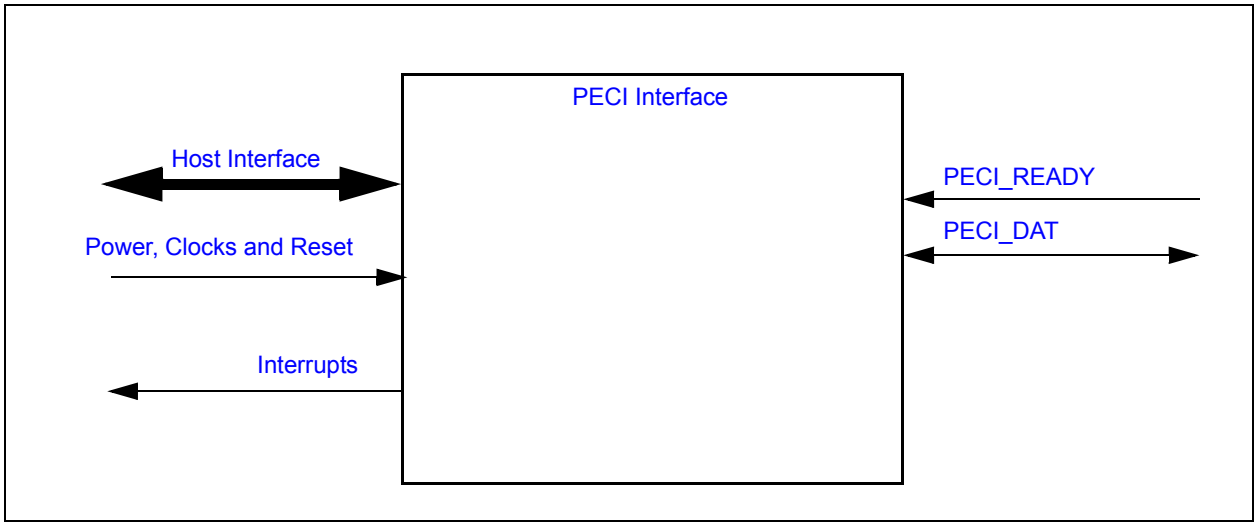
25.3 Terminology

No terminology has been defined for this chapter.

25.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 25-1: PECI INTERFACE I/O DIAGRAM



25.5 Signal Description

The Signal Description Table lists the signals that are typically routed to the pin interface.

TABLE 25-1: SIGNAL DESCRIPTION TABLE

Name	Direction	Description
PECI_READY	Input	PECI Ready input pin **Note:** This signal is optional. If this signal is not on the pin interface it is pulled high internally.
PECI_DAT	Input/Output	PECI Data signal pin

25.10 Instance Description

There is one instance of the PECI Core implemented in the PECI Interface in the MEC140x/1x. See PECI Interface Core, Rev. 1.31, Core-Level Architecture Specification, SMSC Confidential, 4/15/11 for a description of the PECI Core.

25.11 PECI Interface Registers

The registers listed in the PECI Interface Register Summary table are for a single instance of the PECI Interface. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the PECI Interface Register Base Address Table.

TABLE 25-3: EC-ONLY REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
PECI Interface	0	EC	32-bit Internal Address Space	0000_6400h

Note: The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

TABLE 25-4: PECI INTERFACE REGISTER SUMMARY

Offset	Register Name (Mnemonic)
00h	Write Data Register
04h	Read Data Register
08h	Control Register
0Ch	Status Register 1
10h	Status Register 2
14h	Error Register
18h	Interrupt Enable 1 Register
1Ch	Interrupt Enable 2 Register
20h	Optimal Bit Time Register (Low Byte)
24h	Optimal Bit Time Register (High Byte)
28h	Test
2Ch	Test
30h-3Ch	Reserved
40h	Block ID Register
44h	Revision Register
48h - 7Ch	Test

Note: Test registers are reserved for Microchip use only. Reading and writing Test registers may cause undesirable results

For register details see References [1].

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	UPDATE_INTERVAL7 The number of PWM periods between updates to current duty cycle when the segment index is equal to 111b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	nSYSRST
27:24	UPDATE_INTERVAL6 The number of PWM periods between updates to current duty cycle when the segment index is equal to 110b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	nSYSRST
23:20	UPDATE_INTERVAL5 The number of PWM periods between updates to current duty cycle when the segment index is equal to 101b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	nSYSRST
19:16	UPDATE_INTERVAL4 The number of PWM periods between updates to current duty cycle when the segment index is equal to 100b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	nSYSRST
15:12	UPDATE_INTERVAL3 The number of PWM periods between updates to current duty cycle when the segment index is equal to 011b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	nSYSRST
11:8	UPDATE_INTERVAL2 The number of PWM periods between updates to current duty cycle when the segment index is equal to 010b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	nSYSRST

36.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

36.7.1 POWER DOMAINS

Name	Description
VTR	The main power well used when the VBAT RAM is accessed by the EC.
VBAT	The power well used to retain memory state while the main power rail is unpowered.

36.7.2 CLOCK INPUTS

No special clocks are required for this block.

36.7.3 RESETS

Name	Description
VBAT_POR	This signal resets all the registers and logic in this block to their default state.

36.8 Interrupts

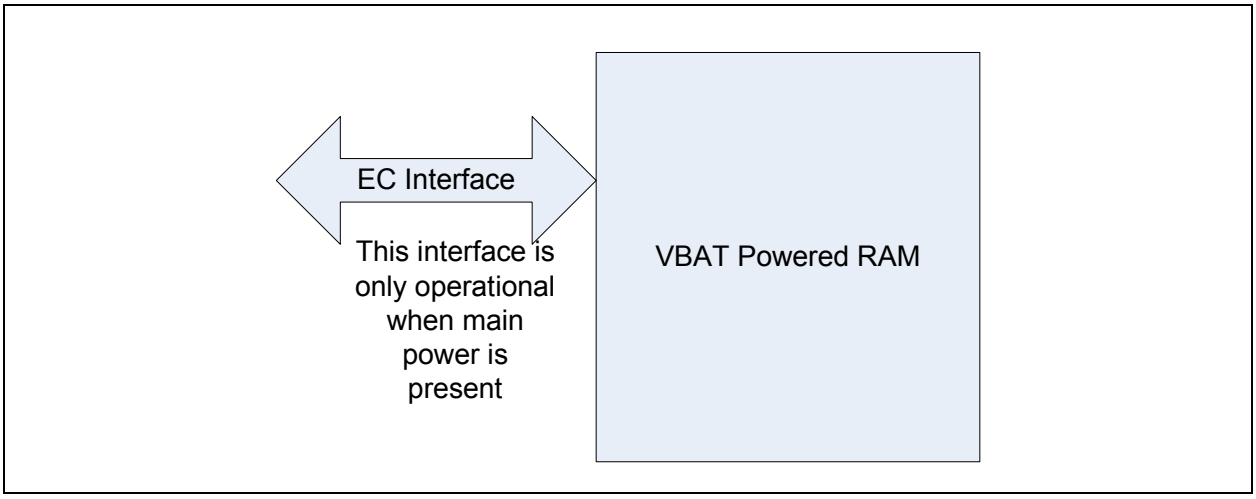
This block does not generate any interrupts.

36.9 Low Power Modes

The VBAT-Powered RAM automatically enters a low power mode whenever it is not being accessed by the EC. There is no chip-level Sleep Enable input.

36.10 Description

FIGURE 36-2: VBAT RAM BLOCK DIAGRAM



37.9.1 VCI REGISTER

Offset	00h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:13	Reserved	R	-	-
12	FILTERS_BYPASS The Filters Bypass bit is used to enable and disable the input filters on the VCI_IN# pins. See Section 43.24, "VBAT-Powered Control Interface Timing," on page 531. 1=Filters disabled 0=Filters enabled (default)	R/W	0	VBAT_POR
11	FW_EXT This bit controls selecting between the external VBAT-Powered Control Interface inputs, or the VCI_FW_CNTRL bit output to control the VCI_OUT pin. 1=VCI_OUT is determined by the VCI_FW_CNTRL field, when VTR is active 0=VCI_OUT is determined by the external inputs.	R/W	0	nSYSRST & VBAT_POR
10	VCI_FW_CNTRL This bit can allow EC firmware to control the state of the VCI_OUT pin. For example, when VTRGD is asserted and the FW_EXT bit is '1', clearing the VCI_FW_CNTRL bit de-asserts the active high VCI_OUT pin. BIOS must set this bit to '1' prior to setting the FW_EXT bit to '1' on power up, in order to avoid glitches on the VCI_OUT pin.	R/W	0	
9	VCI_OUT This bit provides the current status of the VCI_OUT pin.	R	See Note 1	–
8	VCI_OVRD_IN This bit provides the current status of the VCI_OVRD_IN pin.	R	See Note 1	
7:2	Reserved	R	-	-
1:0	VCI_IN# These bits provide the latched state of the associated VCI_IN# pin, if latching is enabled or the current state of the pin if latching is not enabled. In both cases, the value is determined after the action of the VCI Polarity Register.	R	See Note 1	

Note 1: The VCI_IN[1:0]# and VCI_OVRD_IN bits default to the state of their respective input pins. The VCI_OUT bit is determined by the VCI hardware circuit.

TABLE 42-15: ADDITIONAL VTR SUPPLY CURRENT WITH ANALOG BLOCKS ENABLED

VCC	VTR	LPC Clock	48 MHz Ring Oscillator Frequency	Typical (3.3V, 25° C)	Max (3.45V, 70° C)	Max (3.45V, 85° C)	Units	Comments
Off	On	Off	48MHz	0.90	1.00	1.10	mA	Additional I_{VTR} with DAC 0 enabled
Off	On	Off	48MHz	1.00	1.10	1.20	mA	Additional I_{VTR} with DAC 0 & Comparator 0 enabled
Off	On	Off	48MHz	0.90	1.00	1.10	mA	Additional I_{VTR} with DAC 1 enabled
Off	On	Off	48MHz	1.00	1.10	1.20	mA	Additional I_{VTR} with DAC 1 & Comparator 1 enabled
Off	On	Off	48MHz	0.60	0.70	0.80	mA	Additional I_{VTR} with ADC enabled
Note 1: The values in this table are added to the values in Table 42-14 excluding the sleep states.								

TABLE 42-16: VBAT SUPPLY CURRENT, I_VBAT (VBAT=3.0V)

VCC	VTR	LPC Clock	48 MHz Ring Oscillator Frequency	Typical (3.0V, 25° C)	Max (3.0V, 25° C)	Units	Comments
Off	Off	Off	Off	12.00	14.50	uA	Internal 32kHz oscillator
Off	Off	Off	Off	4.75	7.00	uA	32kHz crystal oscillator
Off	Off	Off	Off	4.00	6.50	uA	External 32kHz clock on XTAL2 pin

TABLE 42-17: VBAT SUPPLY CURRENT, I_VBAT (VBAT=3.3V)

VCC	VTR	LPC Clock	48 MHz Ring Oscillator Frequency	Typical (3.0V, 25° C)	Max (3.0V, 25° C)	Units	Comments
Off	Off	Off	Off	13.00	15.50	uA	Internal 32kHz oscillator
Off	Off	Off	Off	5.50	8.00	uA	32kHz crystal oscillator
Off	Off	Off	Off	4.75	7.50	uA	External 32kHz clock on XTAL2 pin