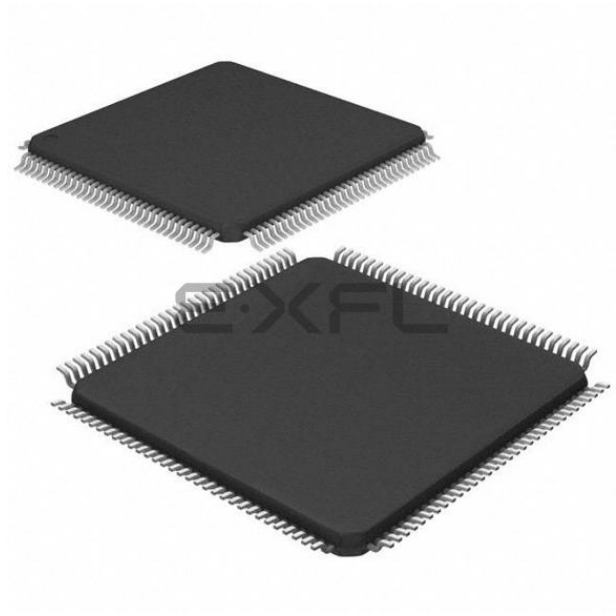

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Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	MIPS32® M14K™
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	160KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1416-i-nu

Note	Description
Note 15	The KSI and KSO Key Scan pins require pull-up resistors. The system designer may opt to use either use the internal pull-up resistors or populate external pull-up resistors.
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.
Note 17	If the eSPI Flash Channel is used for booting, the GPIO135/SHD_IO2 pin must be used to determine that the primary power rails are stable before RSMRST# can be de-asserted. See the MEC140X/1X eSPI Addendum document for more details.
Note 18	If certain blocks are not used, then the associated voltage reference pin may be connected to ground, as follows: • if the ADC is not used and the block is disabled, ADC_VREF can be connected to VSS • if the DAC is not used and the block is disabled, DAC_VREF can be connected to VSS • if both PECI and SB TSI are not used and the GPIO033/PECI_DAT/SB_TSI_DAT and GPIO035/ SB-TSI_CLK pins are configured as GPIOs, then VREF_CPU can be connected to VSS.

2.4 Pin Lists

Note: The GPIO Pin Control registers for the Pads that are not bonded out to pins or balls in the smaller package have been defaulted to their inactive state and are read-only. These pins cannot be modified by the downloaded firmware located in SRAM. No special handling required.

2.4.1 MEC140X PIN LIST

MEC140x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
1	L10	GPIO157/LED0/TST_CLK_OUT
2	N13	GPIO027/KSO00/PVT_IO1
3	M12	GPIO001/SPI_CS#/32KHZ_OUT
4	M10	GPIO002/PWM7
5	G5	VTR
6	M13	GPIO005/SMB00_DATA/SMB00_DATA18/KSI2
7	L12	GPIO006/SMB00_CLK/SMB00_CLK18/KSI3
8	K11	GPIO007/SMB01_DATA/SMB01_DATA18
9	J11	GPIO010/SMB01_CLK/SMB01_CLK18
10	G9	GPIO011/nSMI/nEMI_INT
11	J7	GPIO012/SMB02_DATA/SMB02_DATA18
12	H12	GPIO013/SMB02_CLK/SMB02_CLK18
13	H8	nRESET_IN/GPIO014
14	L11	GPIO015/KSO01/PVT_CS#
15	H11	GPIO016/KSO02/PVT_SCLK
16	J12	GPIO017/KSO03/PVT_IO0
17	C9	VSS
18	F1	VR_CAP
19	H5	VTR
20	G11	GPIO020/CMP_VIN0

MEC140x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
21	H13	GPIO021/CMP_VIN1
22	G12	DAC_VREF
23	G13	GPIO160/DAC_0
24	F12	GPIO161/DAC_1
25	F11	GPIO165/CMP_VREF0
26	E11	GPIO166/CMP_VREF1/UART_CLK
27	F13	GPIO123/SHD_CS#
28	E12	GPIO133/SHD_IO0
29	D12	GPIO134/SHD_IO1
30	E13	GPIO135/SHD_IO2
31	C11	GPIO136/SHD_IO3
32	D13	GPIO126/SHD_SCLK
33	D11	GPIO062/SPI_IO3
34	C12	GPIO030/BCM_INT0#/PWM4
35	C13	GPIO031/BCM_DAT0/PWM5
36	B13	GPIO032/BCM_CLK0/PWM6
37	B11	GPIO045/BCM_INT1#/KSO04
38	B12	GPIO046/BCM_DAT1/KSO05
39	B10	GPIO047/BCM_CLK1/KSO06
40	A13	GPIO050/TACH0
41	A12	GPIO051/TACH1
42	A11	GPIO052/SPI_IO2
43	H6	VTR
44	C8	GPIO053/PWM0
45	B9	GPIO054/PWM1
46	A10	GPIO055/PWM2/KSO08/PVT_IO3
47	A9	GPIO056/PWM3
48	B8	GPIO057/VCC_PWRGD
49	B7	GPIO060/KBRST
50	A8	GPIO025/KSO07/PVT_IO2
51	C10	VSS
52	C7	GPIO026/PS2_CLK1B
53	A7	GPIO061/LPCPD#
54	H7	VTR_33_18
55	C6	GPIO063/SER_IRQ
56	B6	GPIO064/LRESET#
57	A6	GPIO034/PCI_CLK
58	B5	GPIO044/LFRAME#
59	A5	GPIO040/LAD0
60	A4	GPIO041/LAD1
61	C5	GPIO042/LAD2
62	C4	GPIO043/LAD3
63	B4	GPIO067/CLKRUN#
64	D1	VSS

2.8 Non Backdrive Protected Pins

TABLE 2-1: lists pins which do not have backdrive protection. If the power supply used to power the buffer of the pin (VTR or VTR_33_18) is off none of these pins are allowed to be above 0V to prevent back-drive onto the associated power supply. The Power Supply used to power the buffer is shown in the Signal Power Well column of the Pin Multiplexing Tables in **Section 2.0 "Pin Configuration"**.

TABLE 2-1: MEC140X/1X NON BACKDRIVE PROTECTED PINS

Pin Name
DAC_VREF
GPIO160/DAC_0
GPIO161/DAC_1
GPIO165/CMP_VREF0
GPIO166/CMP_VREF1/UART_CLK
GPIO020/CMP_VIN0
GPIO021/CMP_VIN1
GPIO035/SB-TSI_CLK
GPIO033/PECI_DAT/SB_TSI_DAT
VREF_CPU
ADC_VREF
GPIO153/ADC4
GPIO154/ADC3
GPIO155/ADC2
GPIO122/ADC1
GPIO121/ADC0
GPIO022/ADC5
GPIO023/ADC6/A20M
GPIO024/ADC7
GPIO040/LAD0
GPIO041/LAD1
GPIO042/LAD2
GPIO043/LAD3
GPIO063/SER_IRQ
XTAL1
XTAL2

2.9 Pin Description

Note: See Section 2.3, "Notes for Tables in this Chapter," on page 13 for notes that are referenced in the Pin Description table.

Interface	Signal Name	Description	Notes
Analog Data Acquisition Interface	ADC0	ADC channel 0	Note 8
Analog Data Acquisition Interface	ADC1	ADC channel 1	Note 8
Analog Data Acquisition Interface	ADC2	ADC channel 2	Note 8

MEC140x								
VTQFP Pin#	**Mux**	**Signal Name**	**Buffer Type**	**Default Buffer Operation**	**Signal Power Well**	**Emulated Power Well**	**Gated State**	**Notes**
19		VTR	PWR		PWR	PWR		
19								
19								
19								
19	Strap							
20	Default: 0	GPIO020	PIO	I-4	VTR	VTR/VCC	No Gate	
20	1	CMP_VIN0	I_AN		I_AN	I_AN	No Gate	
20	2	Reserved	Reserved		Reserved	Reserved		
20	3	Reserved	Reserved		Reserved	Reserved		
20	Strap							
21	Default: 0	GPIO021	PIO	I-4	PWR	VTR/VCC	No Gate	
21	1	CMP_VIN1	I_AN		I_AN	I_AN	No Gate	
21	2	Reserved	Reserved		Reserved	Reserved		
21	3	Reserved	Reserved		Reserved	Reserved		
21	Strap							
22	0	Reserved	Reserved		Reserved	Reserved		
22	Default: 1	DAC_VREF	DAC_VREF		DAC_VREF	DAC_VREF	No Gate	Note 18
22	2	Reserved	Reserved		Reserved	Reserved		
22	3	Reserved	Reserved		Reserved	Reserved		
22	Strap							
23	Default: 0	GPIO160	PIO	I-4	VTR	VTR/VCC	No Gate	
23	1	DAC_0	O_AN		VTR	VTR	Reserved	
23	2	Reserved	Reserved		Reserved	Reserved		
23	3	Reserved	Reserved		Reserved	Reserved		
23	Strap							
24	Default: 0	GPIO161	PIO	I-4	VTR	VTR/VCC	No Gate	
24	1	DAC_1	O_AN		VTR	VTR	Reserved	
24	2	Reserved	Reserved		Reserved	Reserved		
24	3	Reserved	Reserved		Reserved	Reserved		
24	Strap							
25	Default: 0	GPIO165	PIO	I-4	VTR	VTR/VCC	No Gate	
25	1	CMP_VREF0	CMP_VREF		CMP_VREF	CMP_VREF	No Gate	
25	2	Reserved	Reserved		Reserved	Reserved		
25	3	Reserved	Reserved		Reserved	Reserved		
25	Strap							
26	Default: 0	GPIO166	PIO	I-4	VTR	VTR/VCC	No Gate	
26	1	CMP_VREF1	CMP_VREF		CMP_VREF	CMP_VREF	No Gate	
26	2	UART_CLK	PIO		VTR	VTR/VCC	Low	
26	3	Reserved	Reserved		Reserved	Reserved		
26	Strap							
27	Default: 0	GPIO123	PIO	I-4	VTR	VTR/VCC	No Gate	
27	1	SHD_CS#	PIO		VTR	VTR	Reserved	Note 10

MEC140x								
VTQFP Pin#	Mux	Signal Name	Buffer Type	Default Buffer Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
77	Strap							
78	Default: 0	GPIO114	PIO	I-4	VTR	VTR/VCC	No Gate	
78	1	PS2_CLK0	PIO		VTR	VTR/VCC	Low	
78	2	Reserved	Reserved		Reserved	Reserved		
78	3	Reserved	Reserved		Reserved	Reserved		
78	Strap							
79	Default: 0	GPIO115	PIO	I-4	VTR	VTR/VCC	No Gate	
79	1	PS2_DAT0	PIO		VTR	VTR/VCC	Low	
79	2	Reserved	Reserved		Reserved	Reserved		
79	3	Reserved	Reserved		Reserved	Reserved		
79	Strap							
80	Default: 0	GPIO116	PIO	I-4	VTR	VTR/VCC	No Gate	
80	1	TFDP_DATA	PIO		VTR	VTR	Reserved	
80	2	UART_RX	PIO		VTR	VTR	Low	
80	3	Reserved	Reserved		Reserved	Reserved		
80	Strap							
81	Default: 0	GPIO117	PIO	I-4	VTR	VTR/VCC	No Gate	
81	1	TFDP_CLK	PIO		VTR	VTR	Reserved	
81	2	UART_TX	PIO		VTR	VTR	Reserved	
81	3	Reserved	Reserved		Reserved	Reserved		
81	Strap							
82		VTR	PWR		PWR	PWR		
82								
82								
82								
82	Strap							
83	Default: 0	GPIO120	PIO	I-4	VTR	VTR/VCC	No Gate	
83	1	CMP_VOUT1	PIO		VTR	VTR	Reserved	
83	2	Reserved	Reserved		Reserved	Reserved		
83	3	Reserved	Reserved		Reserved	Reserved		
83	Strap							
84		VSS	PWR		PWR	PWR		
84								
84								
84								
84	Strap							
85	Default: 0	GPIO124	PIO	I-4	VTR	VTR/VCC	No Gate	
85	1	CMP_VOUT0	PIO		VTR	VTR	Reserved	
85	2	Reserved	Reserved		Reserved	Reserved		
85	3	Reserved	Reserved		Reserved	Reserved		
85	Strap							
86	Default: 0	GPIO125	PIO	I-4	VTR	VTR/VCC	No Gate	

3.9.4 HOST CLOCK REQUIRED STATUS REGISTERS (HOST_CLK_REQ)

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:21	RESERVED	RES		
20	Reserved	R	0h	nSYSRST
19	eSPI Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
18	RESERVED	RES		
17	Mailbox Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
16	8042EM Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
15	ACPI PM1 Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
14	ACPI EC 1 Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
13	ACPI EC 0 Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
12	GLBL_CFG Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	-	nSYSRST
11	ACPI EC 3 Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
10	ACPI EC 2 Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	nSYSRST
9:4	RESERVED	RES		
3	BIOS1 Clock Required 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R	-	nSYSRST
2	BIOS0 Clock Required 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R	-	nSYSRST

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3	RECEIVE_BUFFER_ERROR 1=Underflow error occurred (attempt to read from an empty Receive Buffer) 0=No underflow occurred	R/WC	0h	RESET
2	TRANSMIT_BUFFER_ERROR 1=Overflow error occurred (attempt to write to a full Transmit Buffer) 0=No overflow occurred	R/WC	0h	RESET
1	DMA_COMPLETE This field has no meaning if DMA is not enabled. This bit will be set to '1' when the DMA controller asserts the DONE signal to the SPI controller. This occurs either when the SPI controller has closed the DMA transfer, or the DMA channel has completed its count. If both Transmit and Receive DMA transfers are active, then this bit will only assert after both have completed. If CLOSE_TRANSFER_ENABLE is enabled, DMA_COMPLETE and TRANSFER_COMPLETE will be asserted simultaneously. This status is not inhibited by the description buffers, so it can fire on all valid description buffers while operating in that mode. 1=DMA completed 0=DMA not completed	R/WC	0h	RESET
0	TRANSFER_COMPLETE In Manual Mode (neither DMA nor Description Buffers are enabled), this bit will be set to '1' when the transfer matches TRANSFER_LENGTH. If DMA Mode is enabled, this bit will be set to '1' when DMA_COMPLETE is set to '1'. In Description Buffer Mode, this bit will be set to '1' only when the Last Buffer completes its transfer. In all cases, this bit will be set to '1' if the STOP bit is set to '1' and the controller has completed the current 8 bits being copied. 1=Transfer completed 0=Transfer not complete	R/WC	0h	RESET

For example, in order to enable LPC transactions to MEC140x/1x Logical Devices while the MEC140x/1x is in a Sleep mode in which the main oscillator is shut off, just before entering sleep EC firmware must enable one of the LPC_WAKE interrupts. The firmware designer may choose either the LPC_WAKE located in GIRQ16 or in GIRQ22. When responding to the GIRQ16 interrupt EC firmware should disable the LPC_WAKE interrupt until firmware determines that it is again appropriate to enter a Deep Sleep mode. GIRQ22 handles this automatically in hardware.

10.11.4 LIST OF INTERRUPT EVENTS

The following table lists all the Interrupt Source, Enable, and Result bits and indicates if they are wake-capable.

TABLE 10-2: INTERRUPT SOURCE, ENABLE SET, ENABLE CLEAR, AND RESULT BIT ASSIGNMENTS

Aggregator IRQ	Aggregator Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description
GIRQ8	0	GPIO140	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	1	GPIO141	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	2	GPIO142	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	3	GPIO143	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	4	GPIO144	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	5	GPIO145	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	6	GPIO146	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	7	GPIO147	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	8	GPIO150	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	9	GPIO151	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	10	GPIO152	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	11	GPIO153	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	12	GPIO154	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	13	GPIO155	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	14	GPIO156	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	15	GPIO157	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	16	GPIO160	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	17	GPIO161	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	18	GPIO162	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	19	GPIO163	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	20	GPIO164	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	21	GPIO165	GPIO Event	Yes	GPIO Interrupt Event
GIRQ8	22	GPIO166	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	0	GPIO100	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	1	GPIO101	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	2	GPIO102	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	3	GPIO103	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	4	GPIO104	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	5	GPIO105	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	6	GPIO106	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	7	GPIO107	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	8	GPIO110	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	9	GPIO111	GPIO Event	Yes	GPIO Interrupt Event
GIRQ9	10	GPIO112	GPIO Event	Yes	GPIO Interrupt Event

Offset	103h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC2OS_DATA_BYTE_3 This is byte 3 of the 32-bit EC2OS DATA BYTES[3:0].	R/W	0h	nSYSRST

14.13.9 EC STATUS REGISTER

This register is aliased to the OS STATUS OS Register on page 229. The OS STATUS OS Register is a read only version of this register.

Offset	104h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	UD0A User Defined	R/W	0b	nSYSRST
6	SMI_EVT See SMI_EVT bit in OS STATUS OS Register on page 229 for bit description.	R/W	0b	nSYSRST
5	SCI_EVT See SMI_EVT bit in OS STATUS OS Register on page 229 for bit description.	R/W	0b	nSYSRST
4	BURST See BURST bit in OS STATUS OS Register on page 229 for bit description.	R/W	0b	nSYSRST
3	CMD See CMD bit in OS STATUS OS Register on page 229 for bit description.	R	0b	nSYSRST
2	UD1A User Defined	R/W	0b	nSYSRST
1	IBF See IBF bit in OS STATUS OS Register on page 229 for bit description.	R	0h	nSYSRST
0	OBF See OBF bit in OS STATUS OS Register on page 229 for bit description.	R	0h	nSYSRST

Note: The IBF and OBF bits are not de-asserted by hardware when the host is powered off, or the LPC interface powers down; for example, following system state changes S3->S0, S5->S0, G3-> S0. For further information on how these bits are cleared, refer to IBF and OBF bit descriptions in the STATUS OS-Register definition.

17.8 Low Power Modes

The UART may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

17.9 Description

The UART is compatible with the 16450, the 16450 ACE registers and the 16C550A. The UART performs serial-to-parallel conversions on received characters and parallel-to-serial conversions on transmit characters. Two sets of baud rates are provided. When the 1.8432 MHz source clock is selected, standard baud rates from 50 to 115.2K are available. When the source clock is 32.26 MHz, baud rates from 126K to 2,016K are available. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock signal by 1 to 65535. The UART is also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, powering down and changing the base address of the UART. The UART interrupt is enabled by programming OUT2 of the UART to logic "1." Because OUT2 is logic "0," it disables the UART's interrupt. The UART is accessible by both the Host and the EC.

17.9.1 PROGRAMMABLE BAUD RATE

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal clock source by any divisor from 1 to 65535. The clock source is either the 1.8432MHz_Clk clock source or the 24MHz_Clk clock source. The output frequency of the Baud Rate Generator is 16x the Baud rate. Two eight bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers, the output divides the clock by the number 3. If a 1 is loaded, the output is the inverse of the input oscillator. If a two is loaded, the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded, the output is low for 2 bits and high for the remainder of the count.

The following tables show possible baud rates.

TABLE 17-2: UART BAUD RATES USING CLOCK SOURCE 1.8432MHz_Clk

Desired Baud Rate	BAUD_CLOCK_SEL	Divisor Used to Generate 16X Clock
50	0	2304
75	0	1536
110	0	1047
134.5	0	857
150	0	768
300	0	384
600	0	192
1200	0	96
1800	0	64
2000	0	58
2400	0	48
3600	0	32
4800	0	24
7200	0	16
9600	0	12

MEC140x						
GPIO Name (Octal)	**Pin Control Register Offset (Hex)**	**Pin Control Register Default (Hex)**	**Default Function**	**Pin Control Register 2 Offset (Hex)**	**Pin Control Register 2 Default (Hex)**	**Default Drive Strength (mA)**
GPIO142	0188	00000000	GPIO142	668	00000010	4
GPIO143	018C	00000000	GPIO143	66C	00000010	4
GPIO144	0190	00000000	GPIO144	670	00000010	4
GPIO145	0194	00000000	GPIO145	674	00000010	4
GPIO146	0198	00000000	GPIO146	678	00000010	4
GPIO147	019C	00000000	GPIO147	67C	00000010	4
GPIO150	01A0	00000000	GPIO150	680	00000010	4
GPIO151	01A4	00000000	GPIO151	684	00000010	4
GPIO152	01A8	00000000	GPIO152	688	00000010	4
GPIO153	01AC	00000000	GPIO153	68C	00000000	2
GPIO154	01B0	00000000	GPIO154	690	00000000	2
GPIO155	01B4	00000000	GPIO155	694	00000000	2
GPIO156	01B8	00000000	GPIO156	698	00000010	4
GPIO157	01BC	00000000	GPIO157	69C	00000010	4
GPIO160	01C0	00000000	GPIO160	6A0	00000010	4
GPIO161	01C4	00000000	GPIO161	6A4	00000010	4
GPIO162	01C8	00001000	VCI_IN1#	6A8	00000010	4
GPIO163	01CC	00001000	VCI_IN0#	6AC	00000010	4
GPIO164	01D0	00001000	VCI_OVRD_IN	6B0	00000010	4
GPIO165	01D4	00000000	GPIO165	6B4	00000010	4
GPIO166	01D8	00000000	GPIO166	6B8	00000010	4

22.5.4.2 MEC141x Pin Control Registers Defaults

MEC141x						
GPIO Name (Octal)	**Pin Control Register Offset (Hex)**	**Pin Control Register Default (Hex)**	**Default Function**	**Pin Control Register 2 Offset (Hex)**	**Pin Control Register 2 Default (Hex)**	**Default Drive Strength (mA)**
GPIO001	0004	00000000	GPIO001	504	00000010	4
GPIO002	0008	00000000	GPIO002	508	00000010	4
GPIO003	000C	00001000	SYS-PWR_PRES	50C	00000010	4
GPIO004	0010	00001000	BGPO	510	00000020	8
GPIO005	0014	00000000	GPIO005	514	00000010	4
GPIO006	0018	00000000	GPIO006	518	00000010	4
GPIO007	001C	00000000	GPIO007	51C	00000010	4
GPIO010	0020	00000000	GPIO010	520	00000010	4
GPIO011	0024	00000000	GPIO011	524	00000010	4
GPIO012	0028	00000000	GPIO012	528	00000010	4
GPIO013	002C	00000000	GPIO013	52C	00000010	4

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	INVERT 1= PWM_OUTPUT ON State is active low 0=PWM_OUTPUT ON State is active high	R/W	0b	nSYSRST
1	CLOCK_SELECT This bit determines the clock source used by the PWM duty cycle and frequency control logic. 1=CLOCK_LOW 0=CLOCK_HIGH	R/W	0b	nSYSRST
0	PWM_ENABLE 1=Enabled (default) 0=Disabled (gates clocks to save power) **Note:** When the PWM enable bit is set to 0 the internal counters are reset and the internal state machine is set to the OFF state. In addition, the PWM_OUTPUT signal is set to the inactive state as determined by the Invert bit. The PWMx Counter ON Time Register and PWMx Counter OFF Time Register are not affected by the PWM enable bit and may be read and written while the PWM enable bit is 0.	R/W	0b	nSYSRST

28.10 EC-Only Registers

The registers listed in the EC-Only Register Summary table are for a single instance of the Blinking/Breathing PWM. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the EC-Only Register Base Address Table.

TABLE 28-11: EC-ONLY REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
Blinking/Breathing PWM	0	EC	32-bit internal address space	0000_B800h
Blinking/Breathing PWM	1	EC	32-bit internal address space	0000_B900h
Blinking/Breathing PWM	2	EC	32-bit internal address space	0000_BA00h

The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

TABLE 28-12: EC-ONLY REGISTER SUMMARY

Offset	Register Name (Mnemonic)
00h	LED Configuration Register
04h	LED Limits Register
08h	LED Delay Register
0Ch	LED Update Stepsize Register
10h	LED Update Interval Register

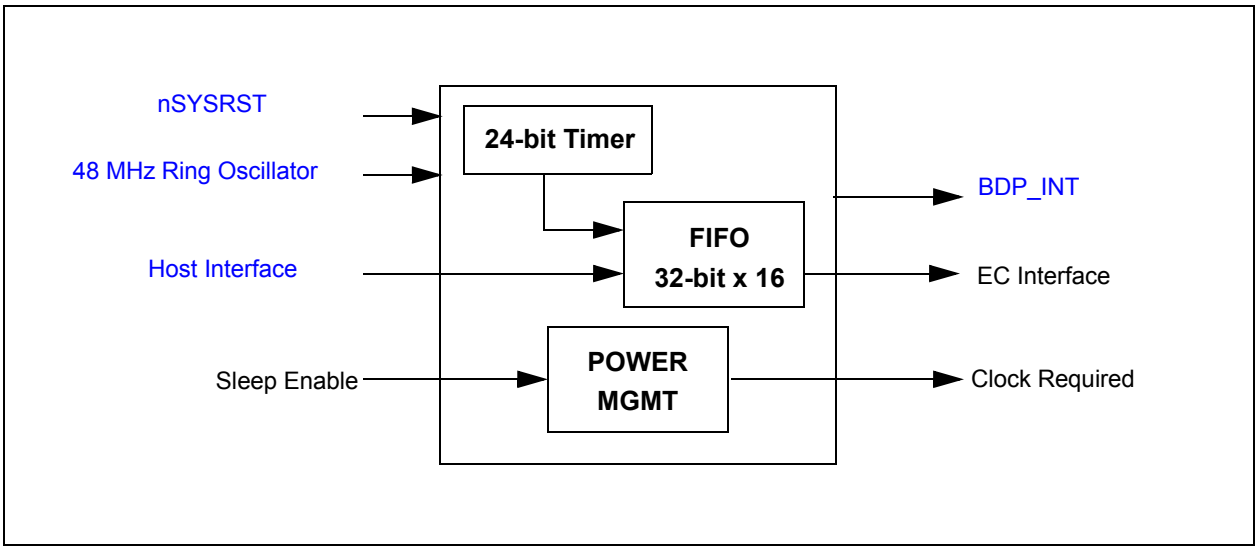
In the following register definitions, a “PWM period” is defined by time the PWM counter goes from 000h to its maximum value (FFh in 8-bit mode, FEh in 7-bit mode and FCh in 6-bit mode, as defined by the PSCALE field in register LED_CFG). The end of a PWM period occurs when the PWM counter wraps from its maximum value to 0.

The registers in this block can be written 32-bits, 16-bits or 8-bits at a time. Writes to LED Configuration Register take effect immediately. Writes to LED Limits Register are held in a holding register and only take effect only at the end of a PWM period. The update takes place at the end of every period, even if only one byte of the register was updated. This means that in blink/PWM mode, software can change the duty cycle with a single 8-bit write to the MIN field in the LED_LIMIT register. Writes to LED Delay Register, LED Update Stepsize Register and LED Update Interval Register also go initially into a holding register. The holding registers are copied to the operating registers at the end of a PWM period only if the Enable Update bit in the LED Configuration Register is set to 1. If LED_CFG is 0, data in the holding registers is retained but not copied to the operating registers when the PWM period expires. To change an LED breathing configuration, software should write these three registers with the desired values and then set LED_CFG to 1. This mechanism ensures that all parameters affecting LED breathing will be updated consistently, even if the registers are only written 8 bits at a time.

33.9 Description

33.9.1 BLOCK DIAGRAM

FIGURE 33-2: Port 80 BIOS Debug Port BLOCK DIAGRAM



The Port 80 BIOS Debug Port consists of a 32-bit wide x 16 deep FIFO and a 24-bit free running timer. Host and EC access to the Port 80 device is through a set of registers. The Host can write the FIFO via the Runtime Registers and the EC can read the FIFO can control the device via the EC-Only Registers.

Writes to the Host Data Register are concatenated with the 24-bit timestamp and written to the FIFO. Reads of the Host Data Register return zero. If writes to the Host Data Register overrun the FIFO, the oldest data are discarded and the OVERRUN status bit in the Status Register is asserted.

Only the EC can read data from the FIFO, using the EC Data Register. The use of this data is determined by EC Firmware alone.

Note:	The Port 80 BIOS Debug Port operates in byte mode. It does not support word writes when locating the two instances at contiguous base addresses.

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	JTAG_EN This bit enables the JTAG debug port. 0 = JTAG port disabled. JTAG cannot be enabled (i.e., the TRST# pin is ignored and the JTAG signals remain in their non-JTAG state). 1= JTAG port enabled. A high on TRST# enables JTAG	R/W	0b	nSYSRST

34.8.4 WDT EVENT COUNT

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3:0	WDT_COUNT These EC R/W bits are cleared to 0 on VTR POR, but not on a WDT. **Note:** This field is written by Boot ROM firmware to indicate the number of times a WDT fired before loading a good EC code image.	R/W	0b	VTR_RESET#

34.8.5 VREF_CPU DISABLE

Offset	40h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:7	Reserved	R	-	-
6:2	Test	R/W	0b	nSYSRST
1	VREF_CPU Disable 0: Enable 1: Disable **Note:** In order to achieve the lowest leakage current when both PECI and SB TSI are not used, set the VREF_CPU Disable bit to 1.	R/W	0b	nSYSRST
0	Test	R	0b	nSYSRST

42.2.7 COMPARATOR ELECTRICAL CHARACTERISTICS

TABLE 42-11: AC AND DC CHARACTERISTICS: COMPARATOR

CHARACTERISTICS		Standard Operating Conditions (unless otherwise noted)				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
V_{IN}	Input Voltage Range	0	-	VTR	V	
V_{HYST}	Input Hysteresis Voltage	15	30	45	mV	
CMRR	Common mode rejection ratio	44	-	-	dB	
T_{RESP}	Large signal response time	—	100	160	ns	VCM = VDD/2 100 mV step
TS_{RESP}	Small signal response time	—	160	320	ns	VCM = VDD/2 100 mV step
T_{ON}	Comparator Enable to Valid Output	—	—	0.1	µS	Note 42-6

Note 42-6 To prevent getting glitches on the comparator output, it is recommended to enable the comparator and wait for the output to be valid and stable before configuring the pin for the CMP_VOUTx function.

42.2.8 THERMAL CHARACTERISTICS

TABLE 42-12: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Consumer Temperature Devices					
Operating Junction Temperature Range	TJ	—	—	+125 (Note 1)	°C
Operating Ambient Temperature Range - Commercial	TA	0	—	+70	°C
Operating Ambient Temperature Range - Industrial	TA	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VTR x IVTR from Table 42-14 and Table 42-15 (e.g., 3.45V x 12.50mA = 43mW)	PD	PINT + PI/O			W
I/O Pin Power Dissipation: I/O = S (({VTR– VOH} x IOH) + S (VOL x IOL))					
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W
Note 1: TJ Max value is at ambient of 70°C					

TABLE 42-13: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 128-pin VTQFP	θJA	51.0	—	°C/W	1
	θJC	25.0	—	°C/W	1
Package Thermal Resistance, 144-pin WFBGA	θJA	50.0	—	°C/W	1
	θJC	17.0	—	°C/W	1
Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) and Junction to case thermal resistance, Theta-JC (θJC) numbers are achieved by package simulations.					

43.4 Pin Reset Timing

43.4.1 RESET_IN# TIMING

Note: The GPIO pins will float after the RESET_IN# pin is asserted low in less than 9 usec (max).

FIGURE 43-3: RESET_IN# TIMING

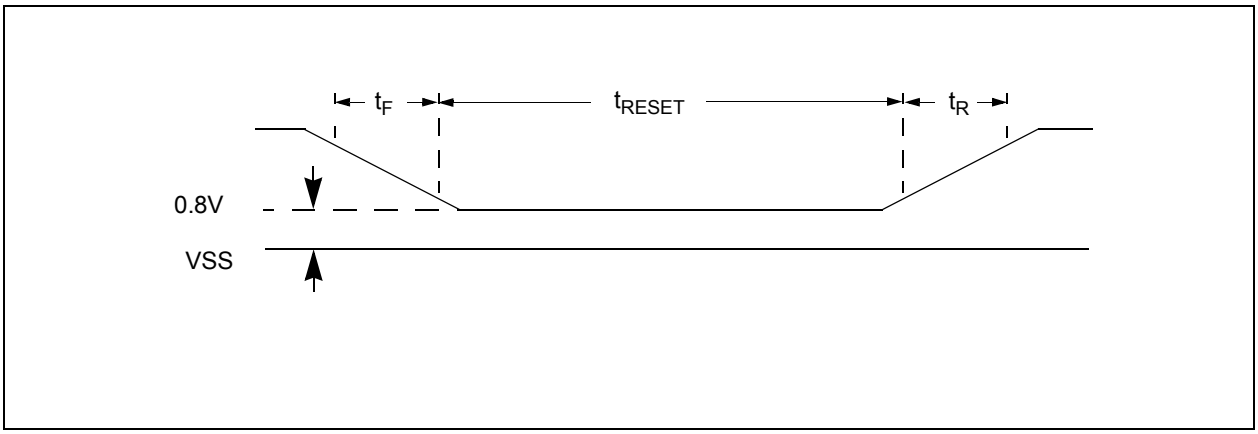


TABLE 43-7: RESETI# TIMING PARAMETERS

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
t_F	RESET_IN# Fall time	0	10	µs	
t_R	RESET_IN# Rise time	0	10	µs	
t_{RESET}	Minimum Reset Time	1		µs	Note 43-8

Note 43-8 The RESET_IN# input can tolerate glitches of no more than 50ns.

43.4.2 RESET_OUT# TIMING

The minimum reset output time is determined by the RESET_IN# pin.

TABLE 44-1: REGISTER MEMORY MAP (CONTINUED)

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
1FFFC 124	JTVIC	0	JTVIC Registers	GIRQ26 Enable Set Register	4
1FFFC 128	JTVIC	0	JTVIC Registers	GIRQ26 Enable Clear Register	4
1FFFC 12C	JTVIC	0	JTVIC Registers	GIRQ26 Result Register	4
1FFFC 200	JTVIC	0	JTVIC Registers	GIRQ8 Aggregator Control Register	4
1FFFC 204	JTVIC	0	JTVIC Registers	GIRQ9 Aggregator Control Register	4
1FFFC 208	JTVIC	0	JTVIC Registers	GIRQ10 Aggregator Control Register	4
1FFFC 20C	JTVIC	0	JTVIC Registers	GIRQ11 Aggregator Control Register	4
1FFFC 210	JTVIC	0	JTVIC Registers	GIRQ12 Aggregator Control Register	4
1FFFC 214	JTVIC	0	JTVIC Registers	GIRQ13 Aggregator Control Register	4
1FFFC 218	JTVIC	0	JTVIC Registers	GIRQ14 Aggregator Control Register	4
1FFFC 21C	JTVIC	0	JTVIC Registers	GIRQ15 Aggregator Control Register	4
1FFFC 220	JTVIC	0	JTVIC Registers	GIRQ16 Aggregator Control Register	4
1FFFC 224	JTVIC	0	JTVIC Registers	GIRQ17 Aggregator Control Register	4
1FFFC 228	JTVIC	0	JTVIC Registers	GIRQ18 Aggregator Control Register	4
1FFFC 22C	JTVIC	0	JTVIC Registers	GIRQ19 Aggregator Control Register	4
1FFFC 230	JTVIC	0	JTVIC Registers	GIRQ20 Aggregator Control Register	4
1FFFC 234	JTVIC	0	JTVIC Registers	GIRQ21 Aggregator Control Register	4
1FFFC 238	JTVIC	0	JTVIC Registers	GIRQ22 Aggregator Control Register	4
1FFFC 23C	JTVIC	0	JTVIC Registers	GIRQ23 Aggregator Control Register	4
1FFFC 240	JTVIC	0	JTVIC Registers	GIRQ24 Aggregator Control Register	4
1FFFC 244	JTVIC	0	JTVIC Registers	GIRQ25 Aggregator Control Register	4
1FFFC 248	JTVIC	0	JTVIC Registers	GIRQ26 Aggregator Control Register	4
1FFFC 300	JTVIC	0	JTVIC Registers	GIRQ8 [7:0] Interrupt Priority Register	4

TABLE 44-1: REGISTER MEMORY MAP (CONTINUED)

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
1FFFC 304	JTVIC	0	JTVIC Registers	GIRQ8 [15:8] Interrupt Priority Register	4
1FFFC 308	JTVIC	0	JTVIC Registers	GIRQ8 [23:16] Interrupt Priority Register	4
1FFFC 30C	JTVIC	0	JTVIC Registers	GIRQ8 [31:24] Interrupt Priority Register	4
1FFFC 310	JTVIC	0	JTVIC Registers	GIRQ9 [7:0] Interrupt Priority Register	4
1FFFC 314	JTVIC	0	JTVIC Registers	GIRQ9 [15:8] Interrupt Priority Register	4
1FFFC 318	JTVIC	0	JTVIC Registers	GIRQ9 [23:16] Interrupt Priority Register	4
1FFFC 31C	JTVIC	0	JTVIC Registers	GIRQ9 [31:24] Interrupt Priority Register	4
1FFFC 320	JTVIC	0	JTVIC Registers	GIRQ10 [7:0] Interrupt Priority Register	4
1FFFC 324	JTVIC	0	JTVIC Registers	GIRQ10 [15:8] Interrupt Priority Register	4
1FFFC 328	JTVIC	0	JTVIC Registers	GIRQ10 [23:16] Interrupt Priority Register	4
1FFFC 32C	JTVIC	0	JTVIC Registers	GIRQ10 [31:24] Interrupt Priority Register	4
1FFFC 330	JTVIC	0	JTVIC Registers	GIRQ11 [7:0] Interrupt Priority Register	4
1FFFC 334	JTVIC	0	JTVIC Registers	GIRQ11 [15:8] Interrupt Priority Register	4
1FFFC 338	JTVIC	0	JTVIC Registers	GIRQ11 [23:16] Interrupt Priority Register	4
1FFFC 33C	JTVIC	0	JTVIC Registers	GIRQ11 [31:24] Interrupt Priority Register	4
1FFFC 340	JTVIC	0	JTVIC Registers	GIRQ12 [7:0] Interrupt Priority Register	4
1FFFC 344	JTVIC	0	JTVIC Registers	GIRQ12 [15:8] Interrupt Priority Register	4
1FFFC 348	JTVIC	0	JTVIC Registers	GIRQ12 [23:16] Interrupt Priority Register	4
1FFFC 34C	JTVIC	0	JTVIC Registers	GIRQ12 [31:24] Interrupt Priority Register	4
1FFFC 350	JTVIC	0	JTVIC Registers	GIRQ13 [7:0] Interrupt Priority Register	4
1FFFC 354	JTVIC	0	JTVIC Registers	GIRQ13 [15:8] Interrupt Priority Register	4
1FFFC 358	JTVIC	0	JTVIC Registers	GIRQ13 [23:16] Interrupt Priority Register	4
1FFFC 35C	JTVIC	0	JTVIC Registers	GIRQ13 [31:24] Interrupt Priority Register	4

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