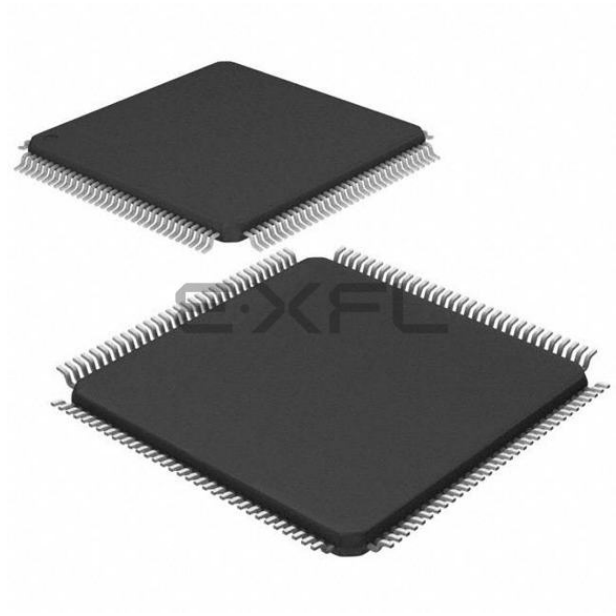

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Product Status	Active
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Controller Series	-
RAM Size	192KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1418-nu

MEC140x								
VTQFP Pin#	Mux	Signal Name	Buffer Type	Default Buffer Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
27	2	Reserved	Reserved		Reserved	Reserved		
27	3	Reserved	Reserved		Reserved	Reserved		
27	Strap							
28	Default: 0	GPIO133	PIO	I-4	VTR	VTR/VCC	No Gate	
28	1	SHD_IO0	PIO		VTR	VTR	Low	Note 10
28	2	Reserved	Reserved		Reserved	Reserved		
28	3	Reserved	Reserved		Reserved	Reserved		
28	Strap							
29	Default: 0	GPIO134	PIO	I-4	VTR	VTR/VCC	No Gate	
29	1	SHD_IO1	PIO		VTR	VTR	Low	Note 10
29	2	Reserved	Reserved		Reserved	Reserved		
29	3	Reserved	Reserved		Reserved	Reserved		
29	Strap							
30	Default: 0	GPIO135	PIO	I-4	VTR	VTR/VCC	No Gate	
30	1	SHD_IO2	PIO		VTR	VTR	Low	Note 10
30	2	Reserved	Reserved		Reserved	Reserved		
30	3	Reserved	Reserved		Reserved	Reserved		
30	Strap							
31	Default: 0	GPIO136	PIO	I-4	VTR	VTR/VCC	No Gate	
31	1	SHD_IO3	PIO		VTR	VTR	Low	Note 10
31	2	Reserved	Reserved		Reserved	Reserved		
31	3	Reserved	Reserved		Reserved	Reserved		
31	Strap							
32	Default: 0	GPIO126	PIO	I-4	VTR	VTR/VCC	No Gate	
32	1	SHD_SCLK	PIO		VTR	VTR	Reserved	Note 10
32	2	Reserved	Reserved		Reserved	Reserved		
32	3	Reserved	Reserved		Reserved	Reserved		
32	Strap							
33	Default: 0	GPIO062	PIO	I-4	VTR	VTR/VCC	No Gate	
33	1	SPI_IO3	PIO		VTR	VTR	Low	
33	2	Reserved	Reserved		Reserved	Reserved		
33	3	Reserved	Reserved		Reserved	Reserved		
33	Strap							
34	Default: 0	GPIO030	PIO	I-4	VTR	VTR/VCC	No Gate	
34	1	BCM_INT0#	PIO		VTR	VTR	High	
34	2	PWM4	PIO		VTR	VTR	Reserved	
34	3	Reserved	Reserved		Reserved	Reserved		
34	Strap							
35	Default: 0	GPIO031	PIO	I-4	VTR	VTR/VCC	No Gate	
35	1	BCM_DAT0	PIO		VTR	VTR	Low	Note 7
35	2	PWM5	PIO		VTR	VTR	Reserved	
35	3	Reserved	Reserved		Reserved	Reserved		

MEC140x								
VTQFP Pin#	Mux	Signal Name	Buffer Type	Default Buffer Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
44	1	PWM0	PIO		VTR	VTR	Reserved	
44	2	Reserved	Reserved		Reserved	Reserved		
44	3	Reserved	Reserved		Reserved	Reserved		
44	Strap							
45	Default: 0	GPIO054	PIO	I-4	VTR	VTR/VCC	No Gate	
45	1	PWM1	PIO		VTR	VTR	Reserved	
45	2	Reserved	Reserved		Reserved	Reserved		
45	3	Reserved	Reserved		Reserved	Reserved		
45	Strap							
46	Default: 0	GPIO055	PIO	I-4	VTR	VTR/VCC	No Gate	
46	1	PWM2	PIO		VTR	VTR	Reserved	
46	2	KSO08	PIO		VTR	VTR	Reserved	Note 15
46	3	PVT_IO3	PIO		VTR	VTR	Low	Note 10
46	Strap							
47	Default: 0	GPIO056	PIO	I-4	VTR	VTR/VCC	No Gate	
47	1	PWM3	PIO		VTR	VTR	Reserved	
47	2	Reserved	Reserved		Reserved	Reserved		
47	3	Reserved	Reserved		Reserved	Reserved		
47	Strap							
48	Default: 0	GPIO057	PIO	I-4	VTR	VTR/VCC	No Gate	
48	1	VCC_PWRGD	PIO		VTR	VTR	High	
48	2	Reserved	Reserved		Reserved	Reserved		
48	3	Reserved	Reserved		Reserved	Reserved		
48	Strap							
49	Default: 0	GPIO060	PIO	I-4	VTR	VTR/VCC	No Gate	
49	1	KBRST	PIO		VTR	VCC	Reserved	
49	2	Reserved	Reserved		Reserved	Reserved		
49	3	Reserved	Reserved		Reserved	Reserved		
49	Strap							
50	Default: 0	GPIO025	PIO	I-4	VTR	VTR/VCC	No Gate	
50	1	KSO07	PIO		VTR	VTR	Reserved	Note 15
50	2	PVT_IO2	PIO		VTR	VTR	Low	Note 10
50	3	Reserved	Reserved		Reserved	Reserved		
50	Strap							
51		VSS	PWR		PWR	PWR		
51								
51								
51								
51	Strap							
52	Default: 0	GPIO026	PIO	I-4	VTR	VTR/VCC	No Gate	
52	1	PS2_CLK1B	PIO		VTR	VTR/VCC	Low	
52	2	Reserved	Reserved		Reserved	Reserved		

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	BAR_CONFLICT This bit is set to 1 whenever a BAR conflict occurs on an LPC address. A Bar conflict occurs when more than one BAR matches the address during of an LPC cycle access. Once this bit is set, it remains set until cleared by being written with a 1.	R/WC	0h	nSYSRST
1	EN_INTERNAL_ERR When this bit is 0, only a BAR conflict, which occurs when two BARs match the same LPC I/O address, will cause LPC_INTERNAL_ERR to be set. When this bit is 1, internal bus errors will also cause LPC_INTERNAL_ERR to be set.	R/W	0h	nSYSRST
0	LPC_INTERNAL_ERR This bit is set whenever a BAR conflict or an internal bus error occurs as a result of an LPC access. Once set, it remains set until cleared by being written with a 1. This signal may be used to generate interrupts. See Section 4.6, "Interrupts," on page 98.	R/WC	0h	nSYSRST

4.11.3 EC SERIRQ REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	RESERVED	RES	-	-
0	EC_IRQ If the LPC Logical Device is selected as the source for a Serial Interrupt Request by an Interrupt Configuration register (see Section 4.8.4.8, "SERIRQ Interrupts," on page 110), this bit is used as the interrupt source.	R/W	0h	nSYSRST

4.11.4 EC CLOCK CONTROL REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	RESERVED	RES	-	-
2	Handshake This bit controls throughput of LPC transactions. When this bit is a ‘0’ the part supports a 33MHz PCI Clock. When this bit is a ‘1’, the part supports a PCI Clock from 24MHz to 33MHz.	RES	1h	nSYSRST

6.0 QUAD SPI MASTER CONTROLLER

6.1 Overview

The Quad SPI Master Controller may be used to communicate with various peripheral devices that use a Serial Peripheral Interface, such as EEPROMS, DACs and ADCs. The controller can be configured to support advanced SPI Flash devices with multi-phase access protocols. Data can be transfered in Half Duplex, Single Data Rate, Dual Data Rate and Quad Data Rate modes. In all modes and all SPI clock speeds, the controller supports back-to-back reads and writes without clock stretching if internal bandwidth permits.

6.2 References

No references have been cited for this feature.

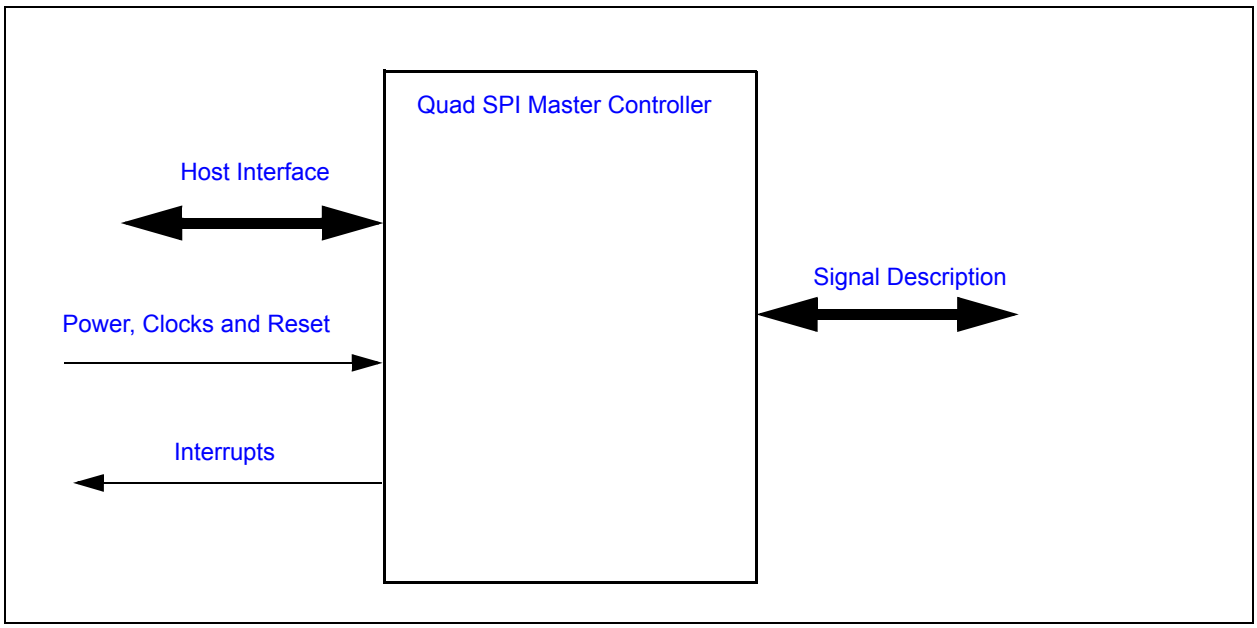
6.3 Terminology

No terminology for this block.

6.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 6-1: I/O DIAGRAM OF BLOCK



6.5 Signal Description

TABLE 6-1: SIGNAL DESCRIPTION

Name	Direction	Description
SPI_CLK	Output	SPI Clock output used to drive the SPCLK pin.
SPI_CS#	Output	SPI chip select

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3	HOLD_OUT_ENABLE 1=HOLD SPI Output Port is driven 0=HOLD SPI Output Port is not driven	R/W	0h	RESET
2	HOLD_OUT_VALUE This bit sets the value on the HOLD SPI Output Port if it is driven. 1=HOLD is driven to 1 0=HOLD is driven to 0	R/W	1h	RESET
1	WRITE_PROTECT_OUT_ENABLE 1=WRITE PROTECT SPI Output Port is driven 0=WRITE PROTECT SPI Output Port is not driven	R/W	0h	RESET
0	WRITE_PROTECT_OUT_VALUE This bit sets the value on the WRITE PROTECT SPI Output Port if it is driven. 1=WRITE PROTECT is driven to 1 0=WRITE PROTECT is driven to 0	R/W	1h	RESET

6.11.5 QMSPI STATUS REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	Reserved	R	-	-
27:24	CURRENT_DESCRIPTION_BUFFER This field shows the Description Buffer currently active. This field has no meaning if Description Buffers are not enabled.	R	0h	RESET
23:17	Reserved	R	-	-
16	TRANSFER_ACTIVE 1=A transfer is currently executing 0=No transfer currently in progress	R	0h	RESET
15	RECEIVE_BUFFER_STALL 1=The SPI interface had been stalled due to a flow issue (an attempt by the interface to write to a full Receive Buffer) 0=No stalls occurred	R/WC	0h	RESET

12.9.4 EC ADDRESS MSB REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	REGION The field specifies which of two segments in the 32-bit internal address space is to be accessed by the EC_Address[14:2] to generate accesses to the memory. 1= The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 1 Register. 0= The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 0 Register.	R/W	0h	nSYSRST
6:0	EC_ADDRESS_MSB This field defines bits[14:8] of EC_Address. Bits[1:0] of the EC_Address are always forced to 00b. The EC_Address is aligned on a DWord boundary. It is the address of the memory being accessed by EC Data Byte 0 Register, which is an offset from the programmed base address of the selected REGION.	R/W	0h	nSYSRST

12.9.5 EC DATA BYTE 0 REGISTER

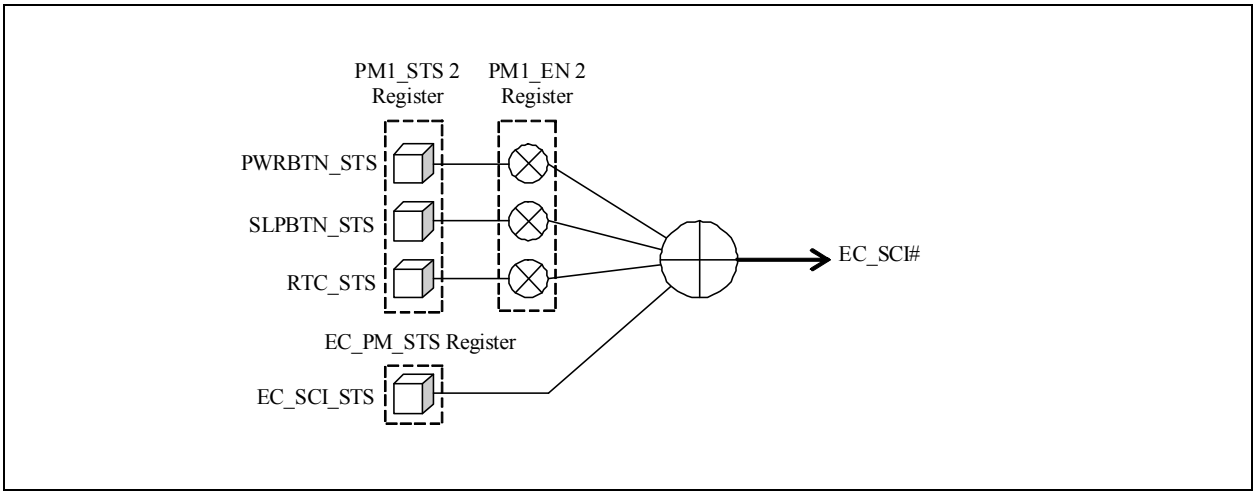
Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_0 This is byte 0 (Least Significant Byte) of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 12.8.2, "EC Data Register".	R/W	0h	nSYSRST

12.9.6 EC DATA BYTE 1 REGISTER

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_1 This is byte 1 of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 12.8.2, "EC Data Register".	R/W	0h	nSYSRST

FIGURE 15-2: describes the relationship of PM1 Status and Enable bits to the EC_SCI# pin.

FIGURE 15-2: EC_SCI# INTERFACE



15.11 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the ACPI PM1 interface. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the Runtime Register Base Address Table.

TABLE 15-2: RUNTIME REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
ACPI PM1 Interface	0	LPC	I/O	Programmed BAR
	0	EC	32-bit internal address space	000F_1400h

The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

All the registers in Table 15-3, "Runtime Registers Summary" may be accessed by the Host and EC with the exception of the EC_PM_STS Register register which is EC-accessed only.

TABLE 15-3: RUNTIME REGISTERS SUMMARY

Offset	Register Name
00h	Power Management 1 Status 1 Register
01h	Power Management 1 Status 2 Register
02h	Power Management 1 Enable 1 Register
03h	Power Management 1 Enable 2 Register
04h	Power Management 1 Control 1 Register
05h	Power Management 1 Control 2 Register
06h	Power Management 2 Control 1 Register

17.11.1 RECEIVE BUFFER REGISTER

Offset	0h (DLAB=0)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	RECEIVED_DATA This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.	R	0h	RESET

17.11.2 TRANSMIT BUFFER REGISTER

Offset	0h (DLAB=0)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	TRANSMIT_DATA This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.	W	0h	RESET

17.11.3 PROGRAMMABLE BAUD RATE GENERATOR LSB REGISTER

Offset	00h (DLAB=1)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	BAUD_RATE_DIVISOR_LSB See Section 17.9.1, "Programmable Baud Rate".	R/W	0h	RESET

TABLE 21-7: SUB-WEEK ALARM COUNTER CLOCK (CONTINUED)

SUBWEEK_ TICK	Source	SPISR	Frequency	Minimum Duration	Maximum Duration
5	Week Counter bit 5	n/a	31.25 Hz	32 sec	272.5 min
6	Week Counter bit 7	n/a	7.8125 Hz	128 sec	18.17 hour
7	Week Counter bit 9	n/a	1.95 Hz	512 sec	72.68 hour

Note 1: The Week Alarm Counter **must not** be modified by firmware if Sub-Week Alarm Counter is using the Week Alarm Counter as its clock source (i.e., the SUBWEEK_TICK field is set to any of the values 4, 5, 6 or 7). The Sub-Week Alarm Counter must be disabled before changing the Week Alarm Counter. For example, the following sequence may be used:

1. Write 0h to the Sub-Week Alarm Counter Register (disabling the Sub-Week Counter)
2. Write the Week Alarm Counter Register
3. Write a new value to the Sub-Week Alarm Counter Register, restarting the Sub-Week Counter

21.9.1.3 15-bit Clock Divider

This counter is 15 bits wide. The clock for this counter is 32KHz_Clk, and as long as the RTC/Week Timer is enabled, it is incremented at 32.768KHz rate. The Clock Divider automatically The Clock Divider generates a clock out of 1 Hz when the counter wraps from 7FFFh to 0h.

By selecting one of the 15 bits of the counter, using the Sub-Second Programmable Interrupt Select Register, the Clock Divider can be used either to generate a time base for the Sub-Week Alarm Counter or as an isochronous interrupt to the EC, the SUB_SECOND interrupt.. See Table 21-10, "SPISR Encoding" for a list of available frequencies.

21.9.2 TIMER VALID STATUS

If power on reset occurs on the VBAT power rail while the main device power is off, the counters in the RTC/Week Alarm are invalid. If firmware detects a POR on the VBAT power rail after a system boot, by checking the status bits in the Power, Clocks and Resets registers, the RTC/Week Alarm block must be reinitialized.

21.9.3 APPLICATION NOTE: REGISTER TIMING

Register writes in the RTC/Week Alarm complete within two cycles of the 32KHz_Clk clock.The write completes even if the main system clock is stopped before the two cycles of the 32K clock complete. Register reads complete in one cycle of the internal bus clock.

All RTC/Week Alarm interrupts that are asserted within the same cycle of the 32KHz_Clk clock are synchronously asserted to the EC.

21.9.4 APPLICATION NOTE: USE OF THE WEEK TIMER AS A 43-BIT COUNTER

The Week Timer cannot be directly used as a 42-bit counter that is incremented directly by the 32.768KHz clock domain. The upper 28 bits (28-bit Week Alarm Counter) are incremented at a 1Hz rate and the lower 16 bits (15-bit Clock Divider) are incremented at a 32.768KHz rate, but the increments are not performed in parallel. In particular, the upper 28 bits are incremented when the lower 15 bits increment from 0 to 1, so as long as the Clock Divider Register is 0 the two registers together, treated as a single value, have a smaller value then before the lower register rolled over from 7FFFh to 0h.

The following code can be used to treat the two registers as a single large counter. This example extracts a 32-bit value from the middle of the 43-bit counter:

```
dword TIME_STAMP(void)
{
    AHB_dword wct_value;
    AHB_dword cd_value1;
    AHB_dword cd_value2;
    dword irqEnableSave;
```

Offset	See Table 22-2, "Register Summary"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
6:4	Interrupt Detection (int_det) The interrupt detection bits determine the event that generates a GPIO_Event. **Note:** See Table 22-3, "Edge Enable and Interrupt Detection Bits Definition". **Note:** Since the GPIO input is always available, even when the GPIO is not selected as the alternate function, the GPIO interrupts may be used for detecting pin activity on alternate functions. The only exception to this is the analog functions (e.g., ADC, DAC, Comparator inputs)	R/W	Note 22-6	nSYSRST
3:2	Power Gating Signals The Power Gating Signals provide the chip Power Emulation options. The pin will be tristated when the selected power well is off (i.e., gated) as indicated. The Emulated Power Well column defined in Pin Multiplexing tables indicates the emulation options supported for each signal. The Signal Power Well column defines the buffer power supply per function. **Note:** Note that all GPIOs support Power Gating unless otherwise noted. 00 = VTR The output buffer is tristated when VTRGD = 0. 01 = VCC The output buffer is tristate when VCC_PWRGD = 0. 10 = Reserved 11 = Reserved	R/W	Note 22-6	nSYSRST
1:0	PU/PD (PU_PD) These bits are used to enable an internal pull-up or pull-down resistor device on the pin. 00 = None. Pin tristates when no active driver is present on the pin. 01 = Pull Up Enabled 10 = Pull Down Enabled (Note 22-7) 11 = Repeater mode. Pin is kept at previous voltage level when no active driver is present on the pin.	R/W	Note 22-6	nSYSRST

Note 22-6 See Section 22.5.4, "Pin Control Registers," on page 320 for the offset and default values for each GPIO Pin Control Register.

Note 22-7 The internal pull-down control should not be selected when configured for an LPC function, which uses the PCI_PIO buffer. Signals with PCI_PIO buffer type do not have an internal pull-down. This configuration option has no effect on the pin.

23.12 SMBus Registers

The registers listed in the *SMBus Core Register Summary* table in the SMBus Controller Core Interface specification (Ref [1]) are for a single instance of the SMBus Controller Core. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the following table:

TABLE 23-2: EC-ONLY REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
SMBus Controller	0	EC	32-bit internal address space	0000_1800h
SMBus Controller	1	EC	32-bit internal address space	0000_AC00h
SMBus Controller	2	EC	32-bit internal address space	0000_B000h

Note: The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

24.10 DMA Main Registers

The addresses of each register listed in these tables are defined as a relative offset to the “Base Address” defined in the DMA Main Register Base Address. The Base Address indicates where the first register can be accessed in a particular bank of registers.

TABLE 24-3: DMA MAIN REGISTER BASE ADDRESS

Instance Name	Channel Number	Host	Address Space	Base Address
DMA Controller	Main Block	EC	32-bit internal address space	0000_2400h

TABLE 24-4: DMA MAIN REGISTER SUMMARY

Offset	REGISTER NAME (Mnemonic)
00h	DMA Main Control Register
04h	DMA Data Packet Register

24.10.1 DMA MAIN CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Reserved	R	-	-
1	SOFT_RESET Soft reset the entire module. This bit is self-clearing.	W	0b	-
0	ACTIVATE Enable the blocks operation. 1=Enable block. Each individual channel must be enabled separately. 0=Disable all channels.	R/WS	0b	DMA_RESET

24.10.2 DMA DATA PACKET REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	DATA_PACKET Debug register that has the data that is stored in the Data Packet. This data is read data from the currently active transfer source.	R	0000h	-

32.0 TRACE FIFO DEBUG PORT (TFDP)

32.1 Introduction

The TFDP serially transmits Embedded Controller (EC)-originated diagnostic vectors to an external debug trace system.

32.2 References

No references have been cited for this chapter.

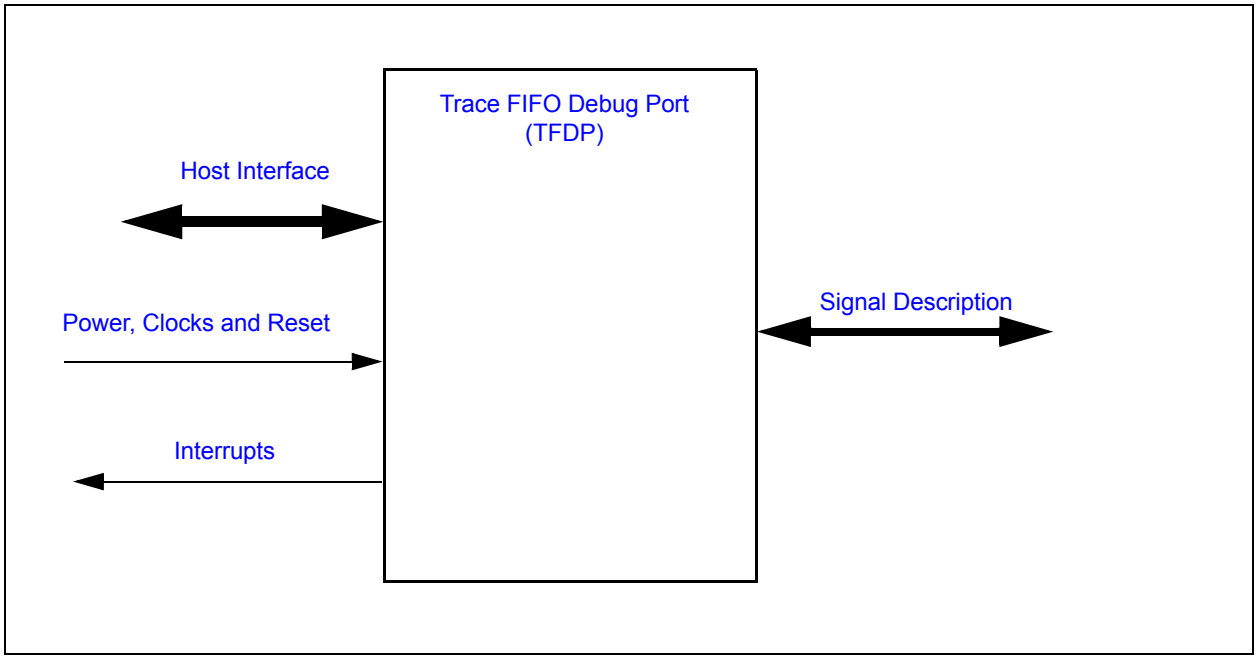
32.3 Terminology

There is no terminology defined for this chapter.

32.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 32-1: I/O DIAGRAM OF BLOCK



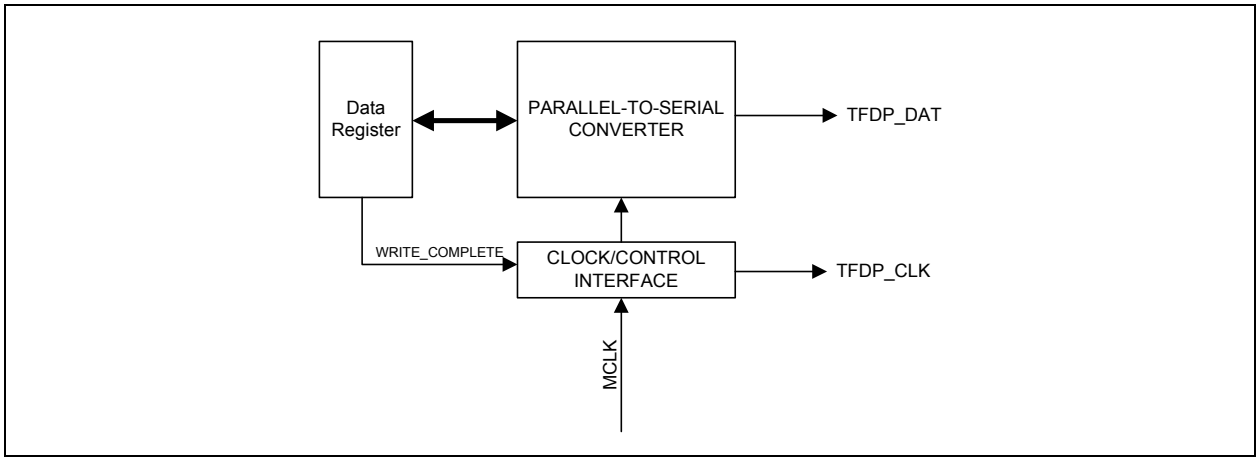
32.5 Signal Description

The Signal Description Table lists the signals that are typically routed to the pin interface.

TABLE 32-1: SIGNAL DESCRIPTION

Name	Direction	Description
TFDP Clk	Output	Derived from EC Bus Clock.
TFDP Data	Output	Serialized data shifted out by TFDP Clk.

FIGURE 32-2: BLOCK DIAGRAM OF TFDP DEBUG PORT

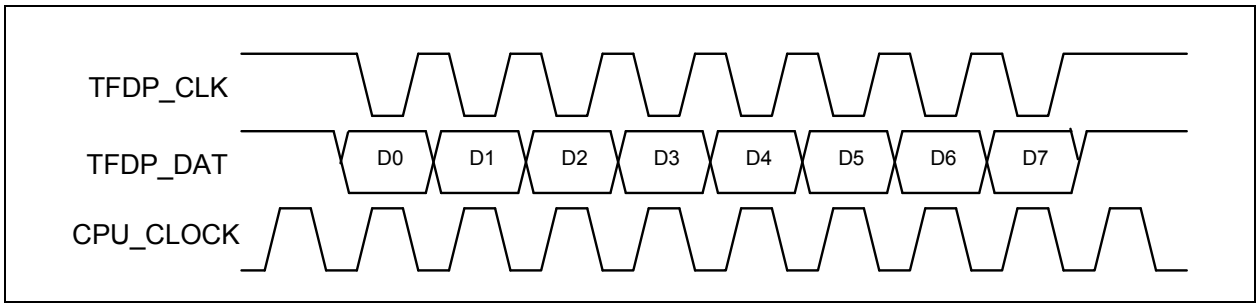


The firmware executing on the embedded controller writes to the Debug Data Register to initiate a transfer cycle (32.11). At first, data from the Debug Data Register is shifted into the LSB. Afterwards, it is transmitted at the rate of one byte per transfer cycle.

Data is transferred in one direction only from the Debug Data Register to the external interface. The data is shifted out at the clock edge. The clock edge is selected by the EDGE_SEL bit in the Debug Control Register. After being shifted out, valid data is guaranteed at the opposite edge of the TFDP_CLK. For example, when the EDGE_SEL bit is '0' (default), valid data is provided at the falling edge of TFDP_CLK. The Setup Time (to the falling edge of TFDP_CLK) is 10 ns, minimum. The Hold Time is 1 ns, minimum.

When the Serial Debug Port is inactive, the TFDP_CLK and TFDP_DAT outputs are '1.' The EC Bus Clock clock input is the transfer clock.

FIGURE 32-3: DATA TRANSFER



32.11 EC-Only Registers

The registers listed in the EC-Only Register Summary table are for a single instance of the Trace FIFO Debug Port (TFDP). The addresses of each register listed in this table are defined as a relative offset to the host "Base Address" defined in the EC-Only Register Base Address Table.

TABLE 32-2: EC-ONLY REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
TFDP Debug Port	0	EC	32-bit internal address space	0000_8C00h

TABLE 40-1: SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
CMP_VOUT0	Output	Comparator 0 output
CMP_VOUT1	Output	Comparator 1 output

40.6 Host Interface

The registers defined for the Comparator Interface are only accessible by the embedded controller. The Comparator Registers for both comparators are located in one register in the EC Subsystem register bank. See Section 34.8.2, "Comparator Control," on page 435.

40.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

40.7.1 POWER DOMAINS

Name	Description
VTR	The logic implemented in this block are powered by this power well.

40.7.2 CLOCK INPUTS

This component does not require a clock input.

40.7.3 RESETS

Name	Description
VTR_RESET#	This signal resets all the register in the EC Subsystem that interact with the comparators.

40.8 Interrupts

The comparators do not have a dedicated interrupt output event. An interrupt can be generated by the GPIO which shares the pin with the comparator output signal.

- GPIO124/CMP_VOUT0
- GPIO120/CMP_VOUT1

The GPIO interrupt is very configurable, thereby allowing CMP_VOUTx signal to generate an event when the CMP_VINx input is greater than the CMP_VREFx input or when it is less than the CMP_VREFx input. See the definition of Bits[7:4] of the Pin Control Register on page 329.

40.9 Low Power Modes

Each comparator is in its lowest powered state when its ENABLE bit is ‘0’.

42.0 ELECTRICAL SPECIFICATIONS

42.1 Maximum Ratings*

*Stresses exceeding those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note:	When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

42.1.1 ABSOLUTE MAXIMUM THERMAL RATINGS

TABLE 42-1: ABSOLUTE MAXIMUM THERMAL RATINGS

Parameter	Maximum Limits
Operating Temperature Range	0^{o}C to +70^{o}C Commercial -40^{o}C to +85^{o}C Industrial
Storage Temperature Range	-55^{o} to +150^{o}C
Lead Temperature Range	Refer to JEDEC Spec J-STD-020B

42.1.2 ABSOLUTE MAXIMUM SUPPLY VOLTAGE RATINGS

TABLE 42-2: ABSOLUTE POWER SUPPLY RATINGS

Symbol	Parameter	Maximum Limits
VBAT	3.0V Battery Backup Power Supply with respect to ground	-0.3V to +3.63V
VTR	3.3V Suspend Power Supply with respect to ground	-0.3V to +3.465V
VTR_33_18	3.3V or 1.8V Power Supply with respect to ground	-0.3V to +3.465V
VCC	3.3V Main Power Supply with respect to ground (Connected to VCC_PWRGD pin)	-0.3V to +3.465V

42.1.3 ABSOLUTE MAXIMUM I/O VOLTAGE RATINGS

Parameter	Maximum Limits
Voltage with respect to ground on any pin without backdrive protection	-0.3V to (Power Supply used to power the buffer) + 0.3V (Note 42-1)

Note 42-1 The Power Supply used to power the buffer is shown in the Signal Power Well column of the Pin Multiplexing Tables in **Section 2.0 "Pin Configuration"**.

43.2 Clocking AC Timing Characteristics

FIGURE 43-2: CLOCK TIMING DIAGRAM

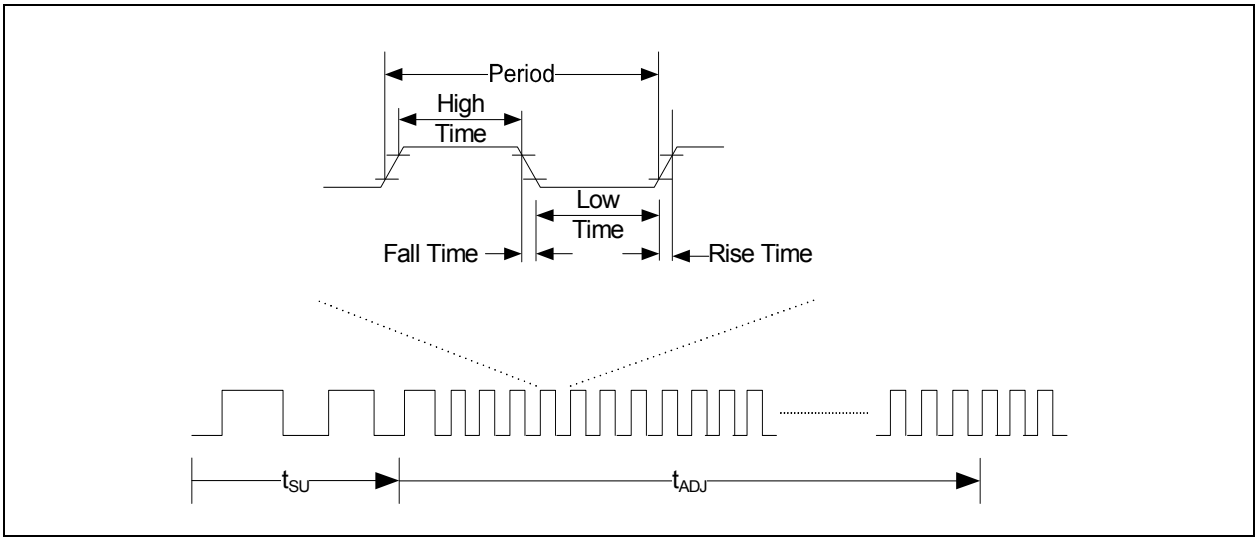


TABLE 43-5: CLOCK TIMING PARAMETERS

Clock	Parameters	Symbol	MIN	TYP	MAX	Units
48 MHz Ring Oscillator	Start-up accuracy (without 32 kHz present)	f_{SU}	22	-	53	MHz
	Start-up delay from 0 MHz to Start-up accuracy	t_{SU}	-	-	6	µs
	Operating Frequency (with external 32kHz clock source present after frequency lock to 48 MHz)	f_{OP}	47.04	48	48.95	MHz
	Operating Frequency (with internal 32 kHz oscillator present after frequency lock to 48 MHz) Note 43-3	f_{OP}	46.08	48	49.92	MHz
	Adjustment Delay from Start-up accuracy to Operating accuracy (time to attain frequency lock - with 32 kHz present)	t_{ADJ}	0.03	-	4 (Note 43-3)	ms
	Adjustment Delay when resuming from Heavy Sleep 3 and System Deepest Sleep state. (time to re-attain frequency lock - with external 32 kHz present)	t_{ADJ}	-	0.60	1 (Note 43-3)	ms
	Operating Frequency (with external 32 kHz removed after frequency locked to 48 MHz)	f_{OP}	43.2 (Note 43-5)	-	52.8 (Note 43-5)	MHz

43.13 I2C/SMBus Timing

FIGURE 43-11: I2C/SMBUS TIMING

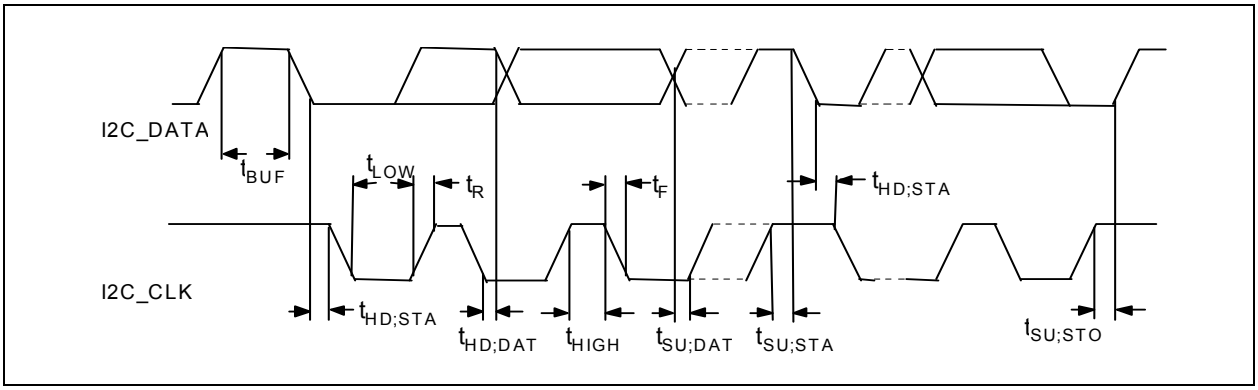


TABLE 43-14: I2C/SMBUS TIMING PARAMETERS

Symbol	Parameter	Standard-Mode		Fast-Mode		Fast-Mode Plus		Units
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCL}	SCL Clock Frequency		100		400		1000	kHz
t_{BUF}	Bus Free Time	4.7		1.3		0.5		µs
$t_{SU;STA}$	START Condition Set-Up Time	4.7		0.6		0.26		µs
$t_{HD;STA}$	START Condition Hold Time	4.0		0.6		0.26		µs
t_{LOW}	SCL LOW Time	4.7		1.3		0.5		µs
t_{HIGH}	SCL HIGH Time	4.0		0.6		0.26		µs
t_R	SCL and SDA Rise Time		1.0		0.3		0.12	µs
t_F	SCL and SDA Fall Time		0.3		0.3		0.12	µs
$t_{SU;DAT}$	Data Set-Up Time	0.25		0.1		0.05		µs
$t_{HD;DAT}$	Data Hold Time	0		0		0		µs
$t_{SU;STO}$	STOP Condition Set-Up Time	4.0		0.6		0.26		µs

FIGURE 43-24: PS/2 RECEIVE TIMING

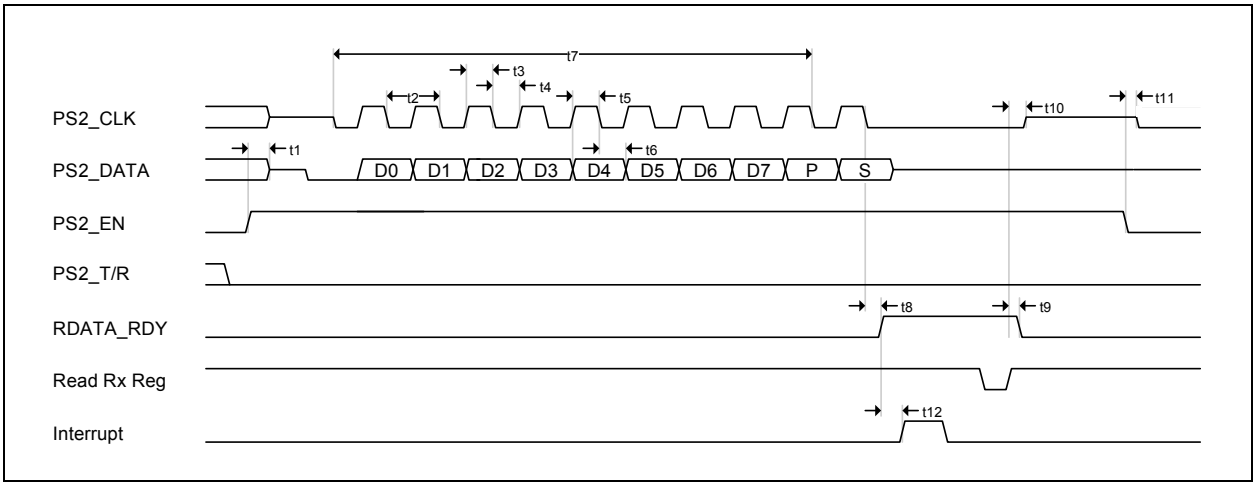


TABLE 43-25: PS/2 CHANNEL RECEIVE TIMING DIAGRAM PARAMETERS

Name	Descritpion	MIN	TYP	MAX	Units
t1	The PS/2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			1000	ns
t2	Period of CLK	60		302	µs
t3	Duration of CLK high (active)	30		151	
t4	Duration of CLK low (inactive)				
t5	DATA setup time to falling edge of CLK. MEC140x/1x samples the data line on the falling CLK edge.	1			
t6	DATA hold time from falling edge of CLK. MEC140x/1x samples the data line on the falling CLK edge.	2			
t7	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t8	Falling edge of 11th CLK to RDATA_RDY asserted.			1.6	µs

PRODUCT IDENTIFICATION SYSTEM

Not all of the possible combinations of Device, Temperature Range and Package may be offered for sale. To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.[1]	-	[X/]	XXX[2]	-	[XX]	-	[X][3]
Device		Temperature Range	Package		ROM Version		Tape and Reel Option

Note: [ ] indicate designators that have blank options

Devices:	MEC1404[1] = 128KB SRAM, LPC Interface MEC1406[1] = 160KB SRAM, LPC Interface MEC1408[1] = 192KB SRAM, LPC Interface MEC1414[1] = 128KB SRAM, eSPI or LPC Interface MEC1416[1] = 160KB SRAM, eSPI or LPC Interface MEC1418[1] = 192KB SRAM, eSPI or LPC Interface		
Temperature Range Option:	Blank	=	0°C to +70°C (Commercial)
	I/	=	-40°C to +85°C (Industrial)
Package:	NU	=	128 pin VTQFP[2]
	SZ	=	144 pin WFBGA[2]
ROM Version:	Blank	=	Standard ROM
Tape and Reel Option:	Blank	=	Tray packaging
	TR	=	Tape and Reel[3]

Examples:

a) MEC1404-NU = 128KB SRAM, LPC Interface, Commercial temperature, 128 VTQFP

b) MEC1406-SZ = 160KB SRAM, LPC Interface, Commercial temperature, 144 WFBGA

c) MEC1418-NU-TR = 192KB SRAM, eSPI or LPC Interface, Commercial temperature, 128 VTQFP, tape and

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html.

Note 3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.