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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	MIPS32® M14K™
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	192KB
Interface	I²C, LPC, SMBus, SPI, UART
Number of I/O	106
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	144-WFBGA
Supplier Device Package	144-WFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1418-sz

Interface	Signal Name	Description	Notes
Quad SPI Master Controller Interface	SPI_IO3	General Purpose SPI Data 3 (SPI_IO3)	
UART Port	CTS#	Clear to Send Input	
UART Port	DCD#	Data Carrier Detect Input	
UART Port	DSR#	Data Set Ready Input	
UART Port	DTR#	Data Terminal Ready Output	
UART Port	RI#	Ring Indicator Input	
UART Port	RTS#	Request to Send Output	
UART Port	UART_CLK	UART Baud Clock Input	
UART Port	UART_RX	UART Receive Data (RXD)	
UART Port	UART_TX	UART Transmit Data (TXD)	
VBAT-Powered Control Interface	BGPO	Battery Powered General Purpose Output	
VBAT-Powered Control Interface	SYSPWR_PRES	Battery Powered System Power Present Input	Note 12
VBAT-Powered Control Interface	VCI_IN0#	Input can cause wakeup or interrupt event	Note 14
VBAT-Powered Control Interface	VCI_IN1#	Input can cause wakeup or interrupt event	Note 14
VBAT-Powered Control Interface	VCI_OUT	Output from combinatorial logic and/or EC	
VBAT-Powered Control Interface	VCI_OVRD_IN	Input can cause wakeup or interrupt event	Note 14

2.10 Pin Multiplexing

Multifunction Pin Multiplexing in the MEC140x/1x is controlled by the GPIO Interface and illustrated in the Pin Multiplexing Table in this section. See Section 2.3, "Notes for Tables in this Chapter," on page 13 for notes that are referenced in the Pin Multiplexing Table. See Pin Control Register on page 329 for Pin Multiplexing programming details.

Pin signal functions that exhibit power domain emulation (see Pin Multiplexing Table below) have a different power supply designation in the “Emulated Power Well” column and “Signal Power Well“ columns.

2.10.1 VCC POWER DOMAIN EMULATION

The System Runtime Supply power VCC is not connected to the MEC140x/1x. The VCC_PWRGD signal is used to indicate when power is applied to the System Runtime Supply.

Pin signal functions with VCC power domain emulation are documented in the Pin Multiplexing Table as “Signal Power Well“= VTR and “Emulated Power Well” = VCC. These pins are powered by VTR and controlled by the VCC_PWRGD signal input. Outputs on VCC power domain emulation pin signal functions are tri-stated when VCC_PWRGD is not asserted and are functional when VCC_PWRGD is active. Inputs on VCC power domain emulation pin signal functions are gated according as defined by the Gated State column in the following tables.

Power well emulation for GPIOs and for signals that are multiplexed with GPIO signals is controlled by the Power Gating Signals field in the GPIO Pin Control Register.

TABLE 4-8: LPC I/O REGISTER MAP (CONTINUED)

Logical Device	BAR LPC Host Address	Example BAR LPC Host Address	LPC Address Mask	Offsets Claimed	Register Name
8042 Emulated Keyboard Controller	Byte Boundary	0060h	4	BAR+0	Write: WRITE_DATA Read: READ_DATA
				+4	Write: WRITE_CMD Read: STATUS
ACPI EC0	Byte Boundary	0062h	4	BAR+0	ACPI_OS_DATA_BYTE_0
				+4	Write: ACPI_OS_COMMAND Read: OS STATUS OS
ACPI EC1	8 Byte Boundary	0070h	7	BAR+0	ACPI_OS_DATA_BYTE_0
				+1	ACPI_OS_DATA_BYTE_1
				+2	ACPI_OS_DATA_BYTE_2
				+3	ACPI_OS_DATA_BYTE_3
				+4	Write: ACPI_OS_COMMAND Read: OS STATUS OS
				+5	OS Byte Control
				+6	Reserved
				+7	Reserved
ACPI PM1	8 Byte Boundary	0078h	7	BAR+0	Power Management 1 Status 1
				+1	Power Management 1 Status 2
				+2	Power Management 1 Enable 1
				+3	Power Management 1 Enable 2
				+4	Power Management 1 Control 1
				+5	Power Management 1 Control 2
				+6	Power Management 2 Control 1
				+7	Power Management 2 Control 2
Legacy Port92/GateA20	Any I/O Byte Address	0092h	0	BAR+0	Port 92
UART 0	8 Byte Boundary	03F0h	7	BAR+0	Write (DLAB=0): Transmit Buffer Read (DLAB=0): Receive Buffer R/W (DLAB=1): Programmable BAUD Rate Generator LSB
				+1	R/W (DLAB=0): Interrupt Enable Register R/W (DLAB=1): Programmable BAUD Rate Generator MSB
				+2	Write: FIFO Control Read: Interrupt Identification
				+3	Line Control
				+4	Modem Control
				+5	Line Status
				+6	Modem Status
				+7	Scratchpad Register
Mailbox Interface	2 Byte Boundary	0100h	1	BAR+0	MBX_INDEX
				+1	MBX_DATA

12.9.4 EC ADDRESS MSB REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	REGION The field specifies which of two segments in the 32-bit internal address space is to be accessed by the EC_Address[14:2] to generate accesses to the memory. 1= The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 1 Register. 0= The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 0 Register.	R/W	0h	nSYSRST
6:0	EC_ADDRESS_MSB This field defines bits[14:8] of EC_Address. Bits[1:0] of the EC_Address are always forced to 00b. The EC_Address is aligned on a DWord boundary. It is the address of the memory being accessed by EC Data Byte 0 Register, which is an offset from the programmed base address of the selected REGION.	R/W	0h	nSYSRST

12.9.5 EC DATA BYTE 0 REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_0 This is byte 0 (Least Significant Byte) of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 12.8.2, "EC Data Register".	R/W	0h	nSYSRST

12.9.6 EC DATA BYTE 1 REGISTER

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_1 This is byte 1 of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 12.8.2, "EC Data Register".	R/W	0h	nSYSRST

12.9.10 INTERRUPT SOURCE MSB REGISTER

Offset	09h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_SWI_MSB EC Software Interrupt Most Significant Bits. These bits are software interrupt bits that may be set by the EC to notify the host of an event. The meaning of these bits is dependent on the firmware implementation. Each bit in this field is cleared when written with a '1b'. The ability to clear the bit can be disabled by the EC. if the corresponding bit in the Host Clear Enable Register is set to '0b'. This may be used by firmware for events that cannot be cleared while the event is still active.	R/WC	0h	nSYSRST

12.9.11 INTERRUPT MASK LSB REGISTER

Offset	0Ah			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	EC_SWI_EN_LSB EC Software Interrupt Enable Least Significant Bits. Each bit that is set to '1b' in this field enables the generation of a Host_SWI_Event interrupt by the corresponding bit in the EC_SWI field in the Interrupt Source LSB Register.	R/W	0h	nSYSRST
0	EC_WR_EN EC Mailbox Write.Interrupt Enable. If this bit is '1b', the interrupt generated by bit EC_WR in the Interrupt Source LSB Register is enabled to generate a EC-to-Host interrupt event.	R/W	0h	nSYSRST

12.9.12 INTERRUPT MASK MSB REGISTER

Offset	0Bh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_SWI_EN_MSB EC Software Interrupt Enable Most Significant Bits. Each bit that is set to '1b' in this field enables the generation of a Host_SWI_Event interrupt by the corresponding bit in the EC_SWI field in the Interrupt Source MSB Register.	R/W	0h	nSYSRST

13.11 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the Mailbox. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the Runtime Register Base Address Table.

TABLE 13-2: RUNTIME REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
Mailbox Interface	0	LPC	I/O	Programmed BAR
		EC	32-bit address space	000F_2400h

The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

TABLE 13-3: RUNTIME REGISTER SUMMARY

Offset	Register Name (Mnemonic)
0h	MBX_INDEX Register
4h	MBX_DATA Register

13.11.1 MBX_INDEX REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	INDEX The index into the mailbox registers listed in Table 13-5, "EC-Only Register Summary".	R/W	0h	nSYSRST and VCC_PWRGD= 0

13.11.2 MBX_DATA REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DATA Data port used to access the registers listed in Table 13-5, "EC-Only Register Summary".	R/W	0h	nSYSRST and VCC_PWRGD= 0

13.12.2 EC-TO-HOST MAILBOX REGISTER

Offset	4h			
MBX_ INDEX	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_HOST_MBOX An EC write to this register will set bit EC_WR in the SMI Interrupt Source Register to ‘1b’. If enabled, this will’ generate a Host SMI. This register is cleared when written with FFh.	R	0h	nSYSRST

13.12.3 SMI INTERRUPT SOURCE REGISTER

Offset	8h			
MBX_ INDEX	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	EC_SWI EC Software Interrupt. An SIRQ to the Host is generated when any bit in this register when this bit is set to ‘1b’ and the corresponding bit in the SMI Interrupt Mask Register register is ‘1b’. This field is Read/Write when accessed by the EC at the EC offset. When written through the Host Access Port, each bit in this field is cleared when written with a ‘1b’. Writes of ‘0b’ have no effect.	Host Access Port: R/WC EC: R/W	0h	nSYSRST
0	EC_WR EC Mailbox Write. This bit is set automatically when the EC-to-Host Mailbox Register has been written. An SMI or SIRQ to the Host is generated when n this bit is ‘1b’ and the corresponding bit in the SMI Interrupt Mask Register register is ‘1b’. This bit is automatically cleared by a read of the EC-to-Host Mail-box Register through the Host Access Port. This bit is read-only when read through the Host Access Port. It is neither readable nor writable directly by the EC when accessed at the EC offset.	Host Access Port: R EC: -	0h	nSYSRST

19.9.2 RTOS TIMER PRE-LOAD

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	Timer Pre-Load Count Value This is the pre load value for the counter. This value is loaded in the timer counter after setting the Timer Start bit or when the counter reloads if the Auto Reload bit is set. **Note:** This register must be programmed with new Pre-Load count value before Timer Start bit is enabled. If this sequence is not followed, the new Pre-Load count value will only take effect when the counter expires if the Auto Reload bit is set. **Note:** Programming this register with 0's will disable the counter and clear the "start" bit if set.	R/W	0h	nSYSRST

19.9.3 TIMER CONTROL

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:5	RESERVED	RES	-	-
4	Firmware Timer Halt This bit gives the firmware the ability to halt the counter without the use of the hardware Halt signal. 0: Do not halt the counter 1: Halt the counter	R/W	0h	nSYSRST
3	Ext Hardware Halt Enable 0: Do not allow hardware Halt signal to stop the counter. 1: Allow hardware Halt signal to stop the counter.	R/W	0h	nSYSRST

21.10.1 CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:7	Reserved	R	-	-
6	POWERUP_EN This bit controls the state of the Power-Up Event Output and enables Week POWER-UP Event decoding in the VBAT-Powered Control Interface on page 462 . See Section 2.5.8, "Power-Up Event Output," on page 307 for a functional description of the POWER-UP_EN bit. 1=Power-Up Event Output Enabled 0=Power-Up Event Output Disabled and Reset	R/W	00h	VBAT_POR
5	BGPO VBAT-powered General Purpose Output Control that is used as part of the VBAT-Powered Control Interface. 1=Output high 0=Output low	R/W	00h	VBAT_POR
4:1	Reserved	R	-	-
0	WT_ENABILE The WT_ENABLE bit is used to start and stop the Week Alarm Counter Register and the Clock Divider Register. The value in the Counter Register is held when the WT_ENABLE bit is not asserted (‘0’) and the count is resumed from the last value when the bit is asserted (‘1’). The 15-Bit Clock Divider is reset to 00h and the RTC/Week Alarm Interface is in its lowest power consumption state when the WT_ENABLE bit is not asserted.	R/W	00h	VBAT_POR

21.10.2 WEEK ALARM COUNTER REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	Reserved	R	-	-
27:0	WEEK_COUNTER While the WT_ENABLE bit is ‘1’, this register is incremented at a 1 Hz rate. Writes of this register may require one second to take effect. Reads return the current state of the register. Reads and writes complete independently of the state of WT_ENABLE.	R/W	00h	VBAT_POR

MEC140x						
GPIO Name (Octal)	**Pin Control Register Offset (Hex)**	**Pin Control Register Default (Hex)**	**Default Function**	**Pin Control Register 2 Offset (Hex)**	**Pin Control Register 2 Default (Hex)**	**Default Drive Strength (mA)**
GPIO004	0010	00001000	BGPO	510	00000010	4
GPIO005	0014	00000000	GPIO005	514	00000010	4
GPIO006	0018	00000000	GPIO006	518	00000010	4
GPIO007	001C	00000000	GPIO007	51C	00000010	4
GPIO010	0020	00000000	GPIO010	520	00000010	4
GPIO011	0024	00000000	GPIO011	524	00000010	4
GPIO012	0028	00000000	GPIO012	528	00000010	4
GPIO013	002C	00000000	GPIO013	52C	00000010	4
GPIO014	0030	00001000	nRESET_IN	530	00000010	4
GPIO015	0034	00000000	GPIO015	534	00000010	4
GPIO016	0038	00000000	GPIO016	538	00000010	4
GPIO017	003C	00000000	GPIO017	53C	00000010	4
GPIO020	0040	00000000	GPIO020	540	00000010	4
GPIO021	0044	00000000	GPIO021	544	00000010	4
GPIO022	0048	00000000	GPIO022	548	00000000	2
GPIO023	004C	00000000	GPIO023	54C	00000000	2
GPIO024	0050	00000000	GPIO024	550	00000000	2
GPIO025	0054	00000000	GPIO025	554	00000010	4
GPIO026	0058	00000000	GPIO026	558	00000010	4
GPIO027	005C	00000000	GPIO027	55C	00000010	4
GPIO030	0060	00000000	GPIO030	560	00000010	4
GPIO031	0064	00000000	GPIO031	564	00000010	4
GPIO032	0068	00000000	GPIO032	568	00000010	4
GPIO033	006C	00000000	GPIO033	56C	00000010	4
GPIO034	0070	00000000	GPIO034	570	00000010	4
GPIO035	0074	00000000	GPIO035	574	00000010	4
GPIO036	0078	00001000	VCI_OUT	578	00000020	8
GPIO040	0080	00000000	GPIO040	580	00000010	4
GPIO041	0084	00000000	GPIO041	584	00000010	4
GPIO042	0088	00000000	GPIO042	588	00000010	4
GPIO043	008C	00000000	GPIO043	58C	00000010	4
GPIO044	0090	00000000	GPIO044	590	00000010	4
GPIO045	0094	00000000	GPIO045	594	00000010	4
GPIO046	0098	00000000	GPIO046	598	00000010	4
GPIO047	009C	00000000	GPIO047	59C	00000010	4
GPIO050	00A0	00000000	GPIO050	5A0	00000010	4
GPIO051	00A4	00000000	GPIO051	5A4	00000010	4
GPIO052	00A8	00000000	GPIO052	5A8	00000010	4
GPIO053	00AC	00000000	GPIO053	5AC	00000010	4
GPIO054	00B0	00000000	GPIO054	5B0	00000010	4
GPIO055	00B4	00000000	GPIO055	5B4	00000010	4
GPIO056	00B8	00000000	GPIO056	5B8	00000010	4

TABLE 22-3: EDGE ENABLE AND INTERRUPT DETECTION BITS DEFINITION

Edge Enable	Interrupt Detection Bits			Selected Function
D7	D6	D5	D4	
0	0	0	0	Low Level Sensitive
0	0	0	1	High Level Sensitive
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Interrupt events are disabled
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	1	0	1	Rising Edge Triggered
1	1	1	0	Falling Edge Triggered
1	1	1	1	Either edge triggered

Note: Only edge triggered interrupts can wake up the main ring oscillator. The GPIO must be enabled for edge-triggered interrupts and the GPIO interrupt must be enabled in the interrupt aggregator in order to wake up the ring when the ring is shut down.

APPLICATION NOTE: All GPIO interrupt detection configurations default to '0000', which is low level interrupt. Having interrupt detection enabled will un-gated the clock to the GPIO module whenever the interrupt is active, which increases power consumption. Interrupt detection should be disabled when not required to save power; this is especially true for pin interfaces (i.e., LPC).

22.6.1.2 Pin Control Register 2

Offset	See Note 22-6			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:6	RESERVED	RES	-	-
5:4	Drive Strength These bits are used to select the drive strength on the pin. 00 = 2mA 01 = 4mA 10 = 8mA 11 = 12mA	R/W	00	nSYSRST

23.12 SMBus Registers

The registers listed in the *SMBus Core Register Summary* table in the SMBus Controller Core Interface specification (Ref [1]) are for a single instance of the SMBus Controller Core. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the following table:

TABLE 23-2: EC-ONLY REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
SMBus Controller	0	EC	32-bit internal address space	0000_1800h
SMBus Controller	1	EC	32-bit internal address space	0000_AC00h
SMBus Controller	2	EC	32-bit internal address space	0000_B000h

Note: The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

24.10 DMA Main Registers

The addresses of each register listed in these tables are defined as a relative offset to the “Base Address” defined in the DMA Main Register Base Address. The Base Address indicates where the first register can be accessed in a particular bank of registers.

TABLE 24-3: DMA MAIN REGISTER BASE ADDRESS

Instance Name	Channel Number	Host	Address Space	Base Address
DMA Controller	Main Block	EC	32-bit internal address space	0000_2400h

TABLE 24-4: DMA MAIN REGISTER SUMMARY

Offset	REGISTER NAME (Mnemonic)
00h	DMA Main Control Register
04h	DMA Data Packet Register

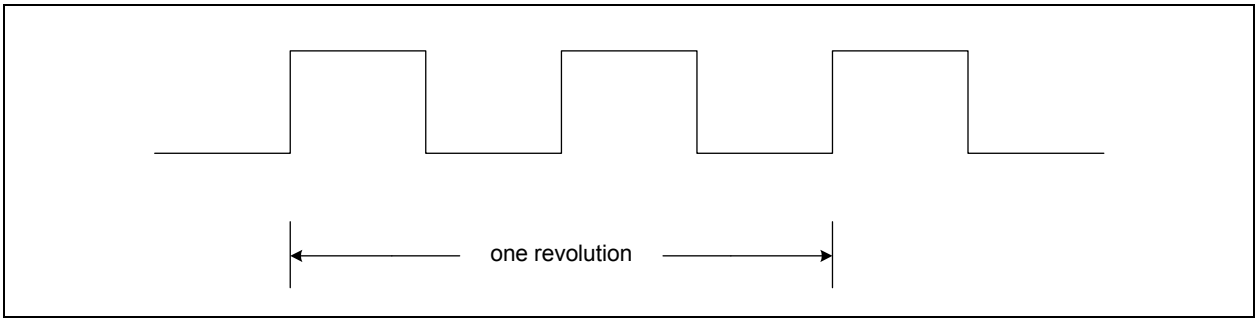
24.10.1 DMA MAIN CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Reserved	R	-	-
1	SOFT_RESET Soft reset the entire module. This bit is self-clearing.	W	0b	-
0	ACTIVATE Enable the blocks operation. 1=Enable block. Each individual channel must be enabled separately. 0=Disable all channels.	R/WS	0b	DMA_RESET

24.10.2 DMA DATA PACKET REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	DATA_PACKET Debug register that has the data that is stored in the Data Packet. This data is read data from the currently active transfer source.	R	0000h	-

FIGURE 26-2: FAN GENERATED 50%DUTY CYCLE WAVEFORM



In typical systems, the fans are powered by the main power supply. Firmware may disable this block when it detects that the main power rail has been turned off by either clearing the <enable> TACH_ENABLE bit or putting the block to sleep via the supported Low Power Mode interface (see Low Power Modes).

26.10.1 MODES OF OPERATION

The Tachometer block supports two modes of operation. The mode of operation is selected via the TACH_READING_-MODE_SELECT bit.

26.10.1.1 Free Running Counter

In Mode 0, the Tachometer block uses the TACHx input as the clock source for the internal TACH pulse counter (see TACHX_COUNTER). The counter is incremented when it detects a rising edge on the TACH input. In this mode, the firmware may periodically poll the TACHX_COUNTER field to determine the average speed over a period of time. The firmware must store the previous reading and the current reading to compute the number of pulses detected over a period of time. In this mode, the counter continuously increments until it reaches FFFFh. It then wraps back to 0000h and continues counting. The firmware must ensure that the sample rate is greater than the time it takes for the counter to wrap back to the starting point.

Note:	Tach interrupts should be disabled in Mode 0.

26.10.1.2 Mode 1 -- Number of Clock Pulses per Revolution

In Mode 1, the Tachometer block uses its 100kHz_Clk clock input to measure the programmable number of TACHx pulses. In this mode, the internal TACH pulse counter (TACHX_COUNTER) returns the value in number of 100kHz_Clk pulses per programmed number of TACH_EDGES. For fans that generate two square waves per revolution, these bits should be configured to five edges.

When the number of edges is detected, the counter is latched and the COUNT_READY_STATUS bit is asserted. If the COUNT_READY_INT_EN bit is set a TACH interrupt event will be generated.

26.10.2 OUT-OF-LIMIT EVENTS

The Tachometer Block has a pair of limit registers that may be configured to generate an event if the Tachometer indicates that the fan is operating too slow or too fast. If the TACHX_COUNTER exceeds one of the programmed limits, the TACHx High Limit Register and the TACHx Low Limit Register, the bit TACH_OUT_OF_LIMIT_STATUS will be set. If the TACH_OUT_OF_LIMIT_STATUS bit is set, the Tachometer block will generate an interrupt event.

28.10.3 LED DELAY REGISTER

This register may be written at any time. Values written into the register are held in an holding register, which is transferred into the actual register at the end of a PWM period if the Enable Update bit in the LED Configuration register is set to 1. Reads of this register return the current contents and not the value of the holding register.

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:24	Reserved	R	-	-
23:12	HIGH_DELAY In breathing mode, the number of PWM periods to wait before updating the current duty cycle when the current duty cycle is greater than or equal to the value MAX in register LED_LIMIT. 4095=The current duty cycle is decremented after 4096 PWM periods … 1=The delay counter is bypassed and the current duty cycle is decremented after two PWM period 0=The delay counter is bypassed and the current duty cycle is decremented after one PWM period	R/W	000h	nSYSRST
11:0	LOW_DELAY The number of PWM periods to wait before updating the current duty cycle when the current duty cycle is greater than or equal to the value MIN in register LED_LIMIT. 4095=The current duty cycle is incremented after 4096 PWM periods … 0=The delay counter is bypassed and the current duty cycle is incremented after one PWM period In blinking mode, this field defines the prescalar for the PWM clock	R/W	000h	nSYSRST

28.10.4 LED UPDATE STEPSIZE REGISTER

This register has eight segment fields which provide the amount the current duty cycle is adjusted at the end of every PWM period. Segment field selection is decoded based on the segment index. The segment index equation utilized depends on the SYMMETRY bit in the LED Configuration Register Register).

- In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]
- In Asymmetric Mode the Segment_Index[2:0] is the bit concatenation of following: Segment_Index[2] = (FALLING RAMP TIME in Figure 28-3, "Clipping Example") and Segment_Index[1:0] = Duty Cycle Bits[7:6].

This register may be written at any time. Values written into the register are held in an holding register, which is transferred into the actual register at the end of a PWM period if the Enable Update bit in the LED Configuration register is set to 1. Reads of this register return the current contents and not the value of the holding register.

In 8-bit mode, each 4-bit STEPSIZE field represents 16 possible duty cycle modifications, from 1 to 16 as the duty cycle is modified between 0 and 255:

15: Modify the duty cycle by 16

...

1: Modify the duty cycle by 2

0: Modify the duty cycle by 1

In 7-bit mode, the least significant bit of the 4-bit field is ignored, so each field represents 8 possible duty cycle modifications, from 1 to 8, as the duty cycle is modified between 0 and 127:

14, 15: Modify the duty cycle by 8

...

2, 3: Modify the duty cycle by 2

33.10 Configuration Registers

The registers listed in the Configuration Register Summary table are for a single instance of the Port 80 BIOS Debug Port. The addresses of each register listed in this table are defined as a relative offset to the host “Base Address” defined in the Configuration Register Base Address Table.

FIGURE 33-3: CONFIGURATION REGISTER BASE ADDRESS

Block Instance	Instance Number	Host	Address Space	Base Address
Port 80 BIOS Debug Port	0	LPC	Configuration Port	INDEX = 00h
		EC	32-bit internal address space	000F_5400h
	1	LPC	Configuration Port	INDEX = 00h
		EC	32-bit internal address space	000F_5800h

Each Configuration register access through the Host Access Port is via its LDN and its Host Access Port Index. EC access is a relative offset to the EC Base Address.

TABLE 33-1: CONFIGURATION REGISTER SUMMARY

EC Offset	Host Index	Register Name (Mnemonic)
330h	30h	Activate Register

33.10.1 ACTIVATE REGISTER

Offset	330h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	ACTIVATE When this bit is asserted ‘1’, the block is enabled. When this bit is ‘0’, writes by the Host interface to the Host Data Register are not claimed, the FIFO is flushed, the 24-bit Timer is reset, and the timer clock is stopped. Control bits in the Configuration Register are not affected by the state of ACTIVATE.	R/W	0h	nSYSRST

38.11.2 ADC DELAY REGISTER

The ADC Delay register determines the delay from setting Start_Repeat in the ADC Control Register and the start of a conversion cycle. This register also controls the interval between conversion cycles in repeat mode.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	**Repeat_Delay[15:0]** This field determines the interval between conversion cycles when Start_Repeat is 1. The delay is in units of 40µs. A value of 0 means no delay between conversion cycles, and a value of 0xFFFF means a delay of 2.6 seconds. This field has no effect when Start_Single is written with a 1.	R/W	0000h	nSYSRST
15:0	**Start_Delay[15:0]** This field determines the starting delay before a conversion cycle is begun when Start_Repeat is written with a 1. The delay is in units of 40µs. A value of 0 means no delay before the start of a conversion cycle, and a value of 0xFFFF means a delay of 2.6 seconds. This field has no effect when Start_Single is written with a 1.	R/W	0000h	nSYSRST

38.11.3 ADC STATUS REGISTER

The ADC Status Register indicates whether the ADC has completed a conversion cycle.

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	RESERVED	RES		
7:0	**ADC_Ch_Status[7:0]** **All bits are cleared by being written with a '1'.** 0: conversion of the corresponding ADC channel is not complete 1: conversion of the corresponding ADC channel is complete Note: for enabled single cycles, the Single_Done_Status bit in the ADC Control Register is also set after all enabled channel conversion are done; for enabled repeat cycles, the Repeat_Done_Status in the ADC Control Register is also set after all enabled channel conversion are done. See Note 38-2.	R/WC	00h	nSYSRST

Note 38-2 Bits that correspond to the unused channels are reserved. See Products on page 3 for the specific number of channels supported for a particular device.

Offset	See Table 38-3, "Analog to Digital Converter Register Summary"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	RESERVED	RES		
9:0	**ADCx_[9:0]** This read-only field reports the 10-bit output reading of the Input ADCx.	R/W	000h	nSYSRST

TABLE 39-3: EC-ONLY REGISTER SUMMARY (CONTINUED)

Offset	Register Name
28h	Microchip Reserved
2Ch	Microchip Reserved
30h	Microchip Reserved

Microchip Reserved registers must not be modified.

39.11.1 DAC ACTIVATE REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	ACTIVATE 1=Block is active. The DAC may be turned on 0=Block disabled. The DAC is in its lowest power state and cannot be enabled	R/W	0h	nSYSRST

39.11.2 DAC CONFIGURATION REGISTER

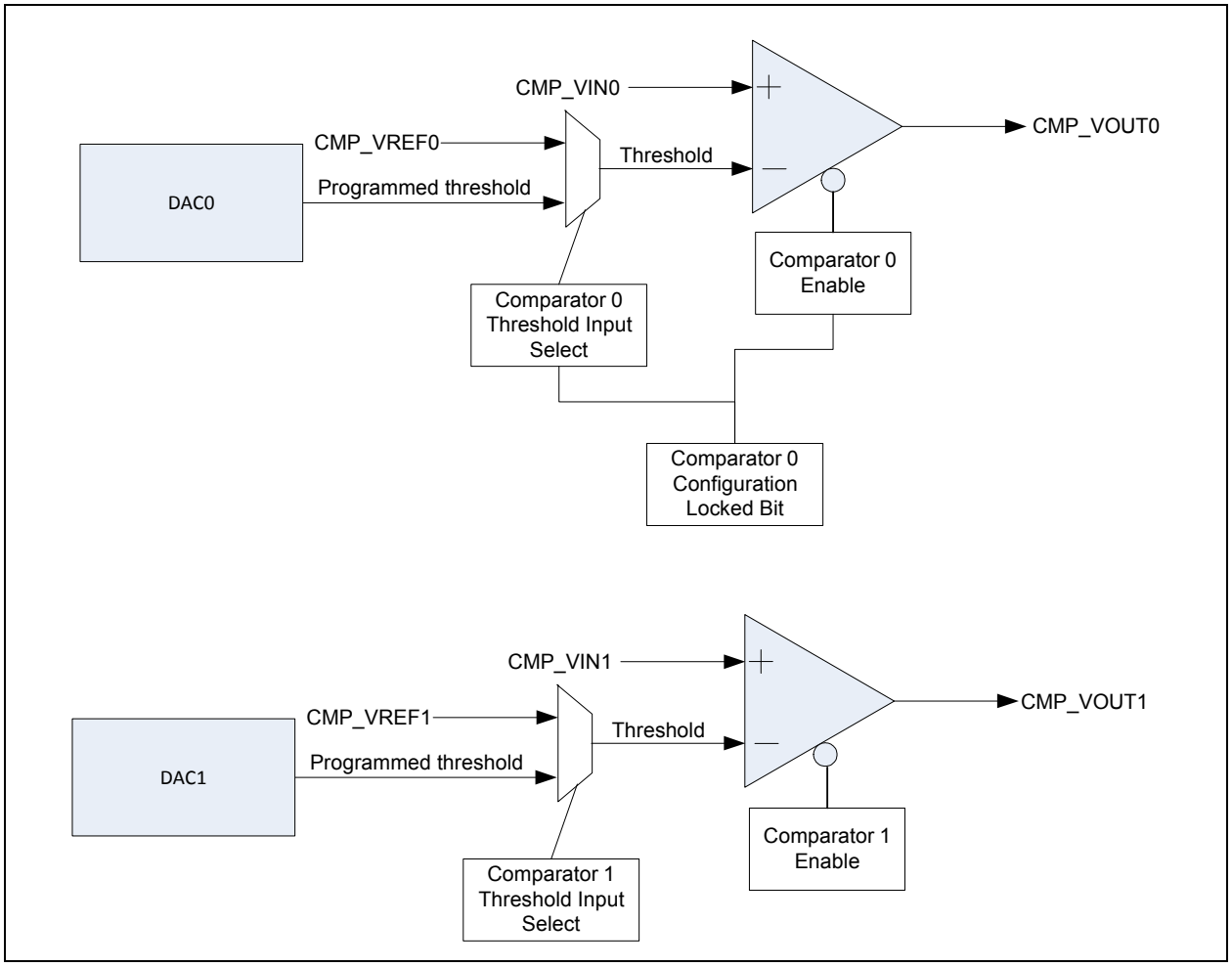
Note: The DAC Configuration register can only be modified when the DACON bit in the DAC Control Register is zero.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	Reserved	R	-	-
2	DAC_VREF SLEEP_CONTROL 1=The DAC responds to its Sleep_Enable input. This DAC output is tristated when the chip is sleeping. **Note:** If it is not desired to have the DAC start operating following a wake event, then it must be disabled prior going to sleep. 0=DAC ignores its Sleep_Enable input. The DAC output is remains unchanged when the chip is sleeping.	R/W	0h	RESET_DAC

40.10 Description

The Analog Comparator compares the analog voltage on an input pin to a reference voltage and generates an output that indicates the result of the comparison. The reference voltage can be derived either from an external pin or from the internal Digital Analog Converter.

FIGURE 40-2: COMPARATOR BLOCK DIAGRAM



The Analog Comparator compares the analog voltage on an input pin to a reference voltage and generates an output that indicates the result of the comparison. The reference voltage is derived either from an external source, on the CMP_VREFx input, or from the internal DAC, as configured by the COMPARATOR x THRESHOLD INPUT SELECT bit in the Comparator Control register.

The GPIO that shares a pin with the CMP_VOUT signal can be used to generate an interrupt to the EC when the pin multiplexer is configured for CMP_VOUT. The GPIO Pin Control Register is configured for the desired interrupt behavior (level or edge). Changes in the CMP_VOUT output signal will be reflected in the Interrupt Status register field for the GPIO, as configured in the GPIO Pin Control Register.

The control bits for Comparator 0 can be locked. The COMPARATOR 0 THRESHOLD INPUT SELECT and COMPARATOR 0 ENABLE bits are locked if the LOCK bit for Comparator 0 is set. Once the LOCK bit is set, neither COMPARATOR 0 THRESHOLD INPUT SELECT or COMPARATOR 0 ENABLE can be modified until the device is power cycled.

40.11 Comparator Registers

Control and status for both comparators are located in one register in the EC Subsystem register bank. See Section 34.8.2, "Comparator Control".

TABLE 44-1: REGISTER MEMORY MAP (CONTINUED)

Addr. (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name	Size (Bytes)
1FFFC 124	JTVIC	0	JTVIC Registers	GIRQ26 Enable Set Register	4
1FFFC 128	JTVIC	0	JTVIC Registers	GIRQ26 Enable Clear Register	4
1FFFC 12C	JTVIC	0	JTVIC Registers	GIRQ26 Result Register	4
1FFFC 200	JTVIC	0	JTVIC Registers	GIRQ8 Aggregator Control Register	4
1FFFC 204	JTVIC	0	JTVIC Registers	GIRQ9 Aggregator Control Register	4
1FFFC 208	JTVIC	0	JTVIC Registers	GIRQ10 Aggregator Control Register	4
1FFFC 20C	JTVIC	0	JTVIC Registers	GIRQ11 Aggregator Control Register	4
1FFFC 210	JTVIC	0	JTVIC Registers	GIRQ12 Aggregator Control Register	4
1FFFC 214	JTVIC	0	JTVIC Registers	GIRQ13 Aggregator Control Register	4
1FFFC 218	JTVIC	0	JTVIC Registers	GIRQ14 Aggregator Control Register	4
1FFFC 21C	JTVIC	0	JTVIC Registers	GIRQ15 Aggregator Control Register	4
1FFFC 220	JTVIC	0	JTVIC Registers	GIRQ16 Aggregator Control Register	4
1FFFC 224	JTVIC	0	JTVIC Registers	GIRQ17 Aggregator Control Register	4
1FFFC 228	JTVIC	0	JTVIC Registers	GIRQ18 Aggregator Control Register	4
1FFFC 22C	JTVIC	0	JTVIC Registers	GIRQ19 Aggregator Control Register	4
1FFFC 230	JTVIC	0	JTVIC Registers	GIRQ20 Aggregator Control Register	4
1FFFC 234	JTVIC	0	JTVIC Registers	GIRQ21 Aggregator Control Register	4
1FFFC 238	JTVIC	0	JTVIC Registers	GIRQ22 Aggregator Control Register	4
1FFFC 23C	JTVIC	0	JTVIC Registers	GIRQ23 Aggregator Control Register	4
1FFFC 240	JTVIC	0	JTVIC Registers	GIRQ24 Aggregator Control Register	4
1FFFC 244	JTVIC	0	JTVIC Registers	GIRQ25 Aggregator Control Register	4
1FFFC 248	JTVIC	0	JTVIC Registers	GIRQ26 Aggregator Control Register	4
1FFFC 300	JTVIC	0	JTVIC Registers	GIRQ8 [7:0] Interrupt Priority Register	4