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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	123
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	PG-BGA-416-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/ft1796256f150ebcnp

General Device Information

Table 2 Pin Definitions and Functions

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
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External Bus Interface Lines (EBU)

D[31:0] I/O B1 V_{DDEBU}

EBU Data Bus Lines

The EBU Data Bus Lines D[31:0] serve as external data bus.

D0	T26	I/O			Data bus line 0
D1	T24	I/O			Data bus line 1
D2	U26	I/O			Data bus line 2
D3	T25	I/O			Data bus line 3
D4	V26	I/O			Data bus line 4
D5	U25	I/O			Data bus line 5
D6	U23	I/O			Data bus line 6
D7	W26	I/O			Data bus line 7
D8	V25	I/O			Data bus line 8
D9	U24	I/O			Data bus line 9
D10	Y26	I/O			
D11	AA26	I/O			
D12	W25	I/O			
D13	V24	I/O			
D14	Y25	I/O			
D15	AB26	I/O			
D16	W24	I/O			
D17	AA25	I/O			
D18	Y24	I/O			
D19	AA23	I/O			
D20	AB25	I/O			
D21	AB24	I/O			
D22	AA24	I/O			
D23	AC26	I/O			
D24	AD26	I/O			
D25	AC25	I/O			
D26	AE26	I/O			
D27	AD25	I/O			
D28	AC24	I/O			
D29	AE25	I/O			
D30	AE24	I/O			
D31	AD24	I/O			

General Device Information

Analog Inputs

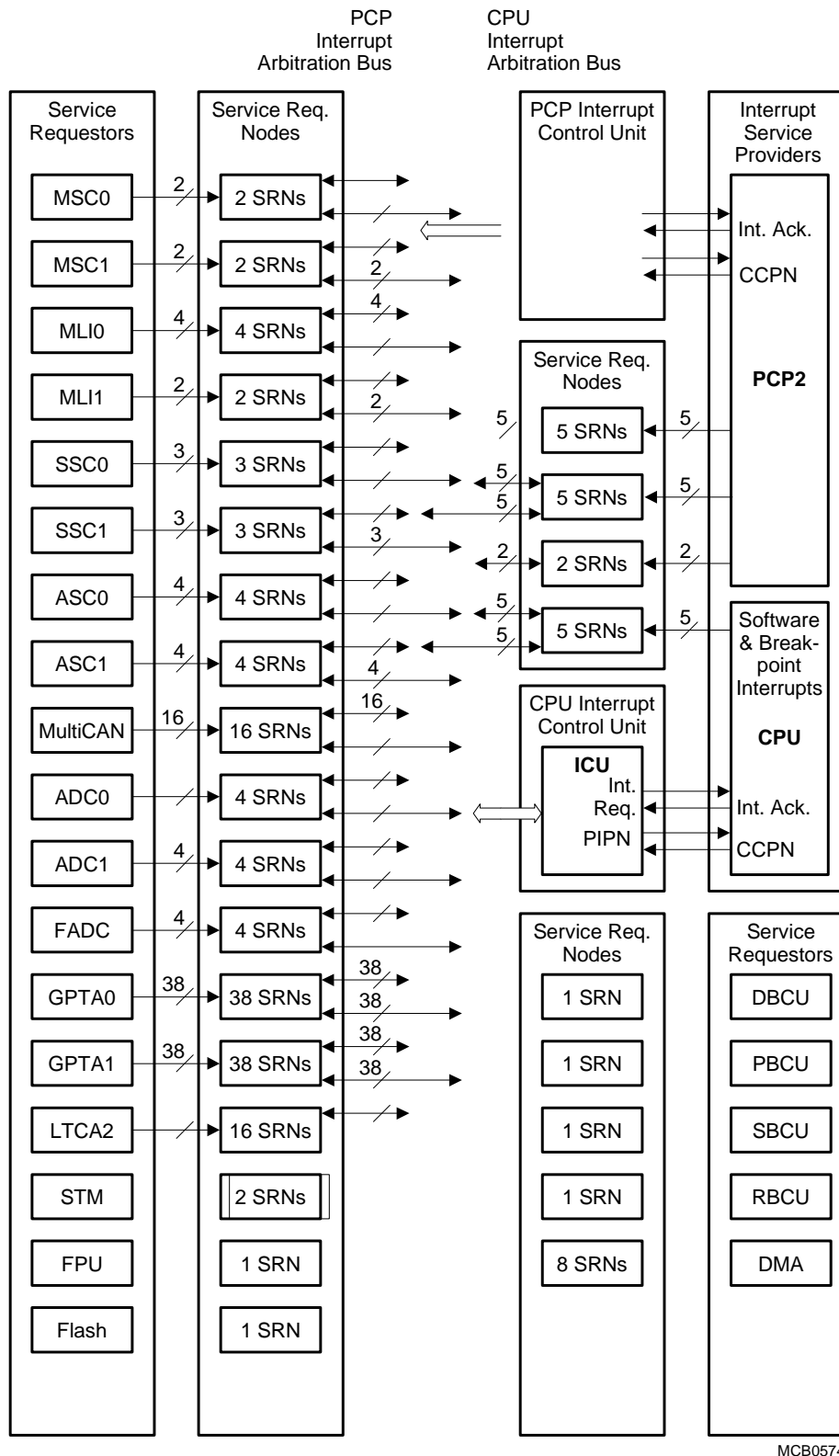
AN[43:0] I D –

ADC Analog Input Port

The ADC Analog Input Port provides 44 analog input lines for the A/D converters

AN0	AE1	I
AN1	AD2	I
AN2	AA4	I
AN3	AB3	I
AN4	AC2	I
AN5	AA3	I
AN6	AD1	I
AN7	AB4	I
AN8	AC1	I
AN9	AB2	I
AN10	Y3	I
AN11	AA2	I
AN12	AB1	I
AN13	W3	I
AN14	Y2	I
AN15	AA1	I
AN16	V4	I
AN17	W2	I
AN18	Y1	I
AN19	V3	I
AN20	W1	I
AN21	V2	I
AN22	V1	I
AN23	U1	I
AN24	AC8	I
AN25	AD8	I
AN26	AC7	I
AN27	AD7	I
AN28	AE6	I
AN29	AF6	I
AN30	AE7	I
AN31	AF7	I

Functional Description



MCB05742

Figure 7 Block Diagram of the TC1796 Interrupt System

Functional Description

3.14 General Purpose Timer Array

The GPTA provides a set of timer, compare and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms needed in other industrial applications.

The TC1796 contains two General Purpose Timer Arrays (GPTA0 and GPTA1) with identical functionality, plus an additional Local Timer Cell Array (LTCA2). **Figure 14** shows a global view of the GPTA modules.

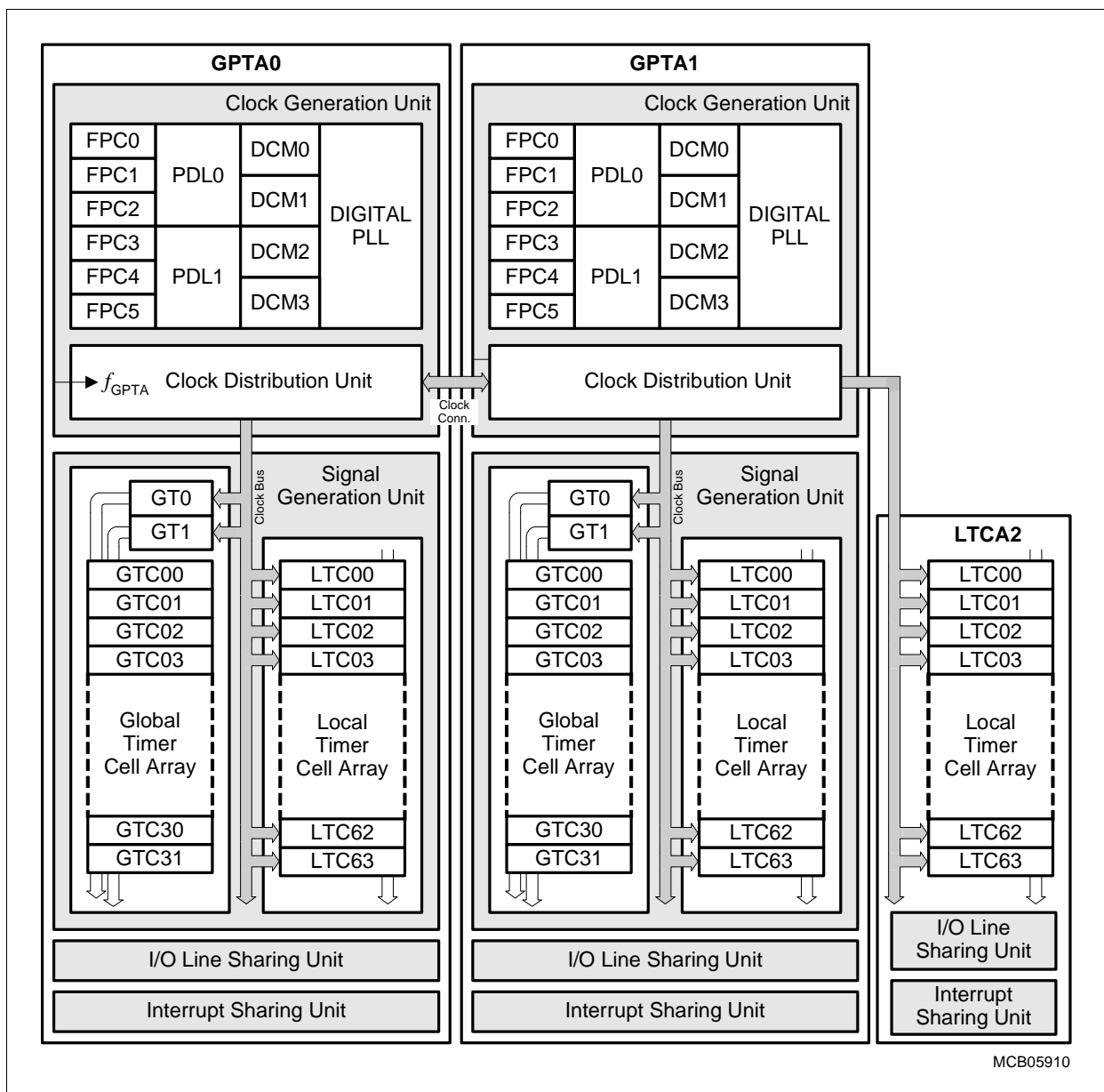


Figure 14 Block Diagram of the GPTA Modules

Functional Description

Figure 17 shows an overview on the System Timer with the options for reading parts of STM contents.

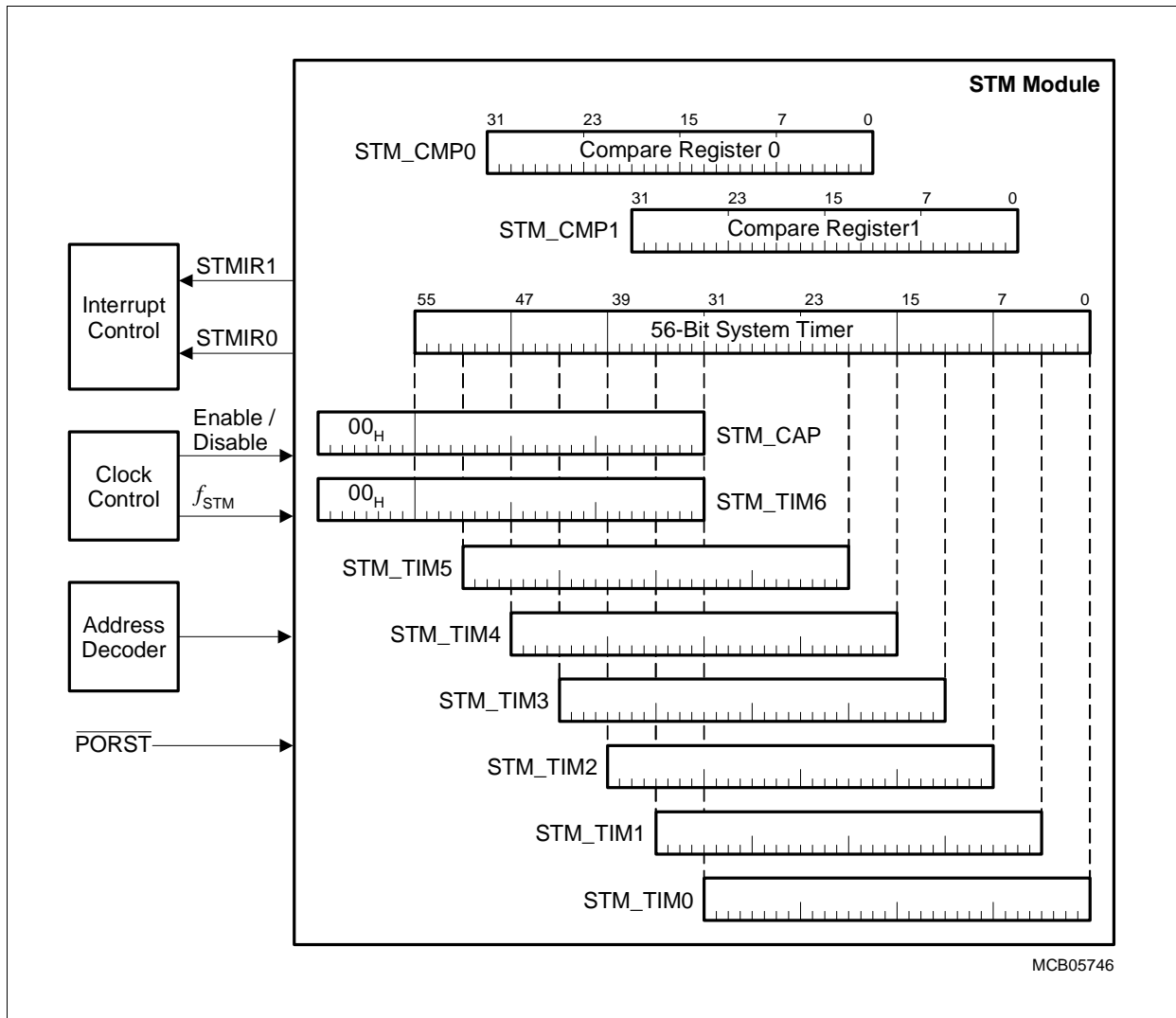


Figure 17 General Block Diagram of the STM Module Registers



TC1796

Functional Description



TC1796

Functional Description

Electrical Parameters



TC1796

Electrical Parameters

Electrical Parameters

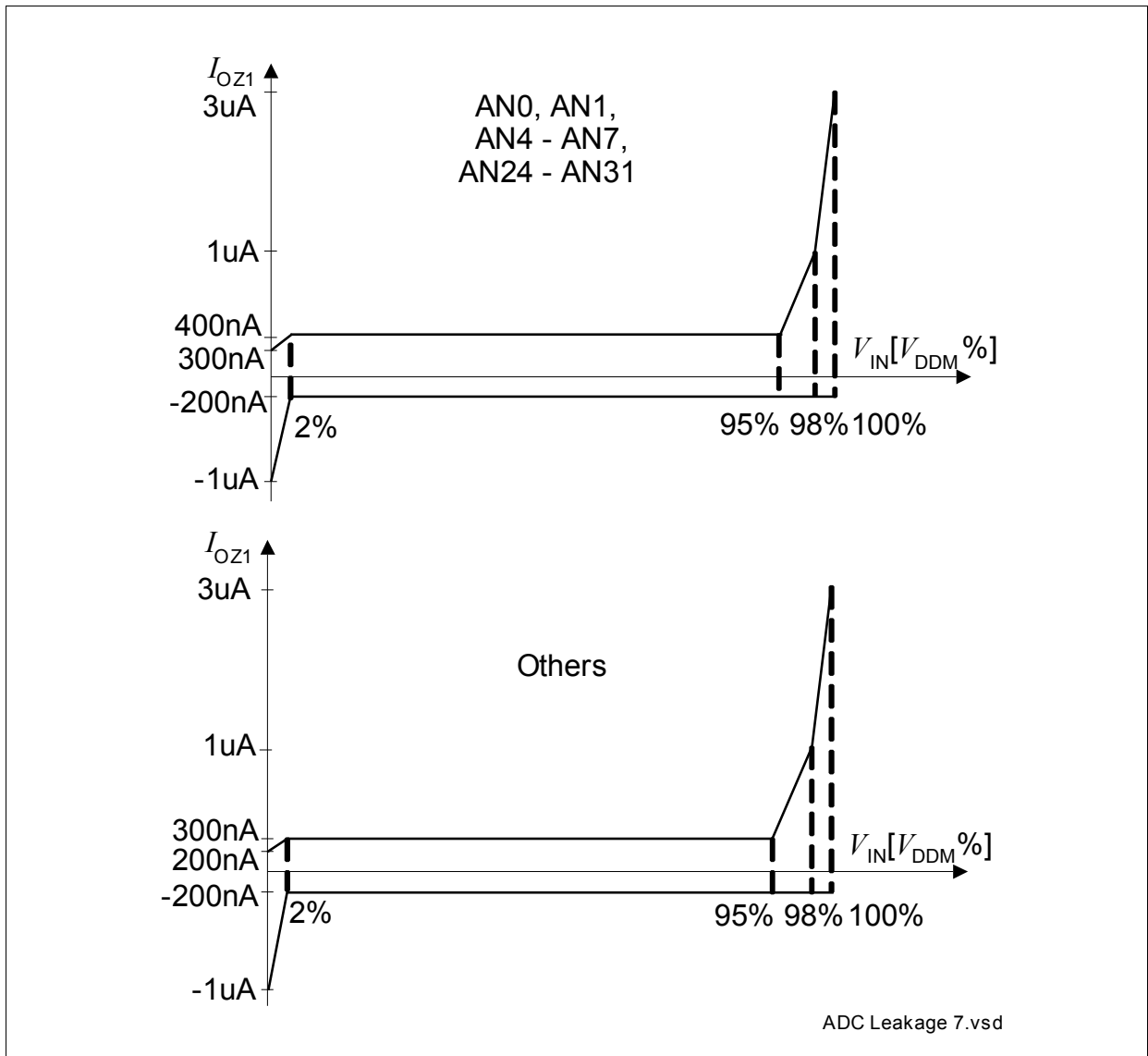


Figure 24 **ADC0/ADC1 Analog Inputs Leakage**

4.3.7 Debug Trace Timing

$V_{SS} = 0\text{ V}$;

4.3.9.2 Demultiplexed Write Timing

Figure 39 EBU Demultiplexed Write Timing

Electrical Parameters

4.3.11 EBU Arbitration Signal Timing

$V_{SS} = 0\text{ V}$; $V_{DD} = 1.5\text{ V} \pm 5\%$; $V_{DDEBU} = 2.5\text{ V} \pm 5\%$ and $3.3\text{ V} \pm 5\%$, Class B pins;
 $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$; $C_L = 35\text{ pF}$;

Table 31 EBU Arbitration Signal Timing Parameters¹⁾

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from CLKOUT rising edge	t_{27}	CC	–	–	3	ns	–
Data setup to CLKOUT falling edge	t_{28}	SR	8	–	–	ns	–
Data hold from CLKOUT falling edge	t_{29}	SR	2	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

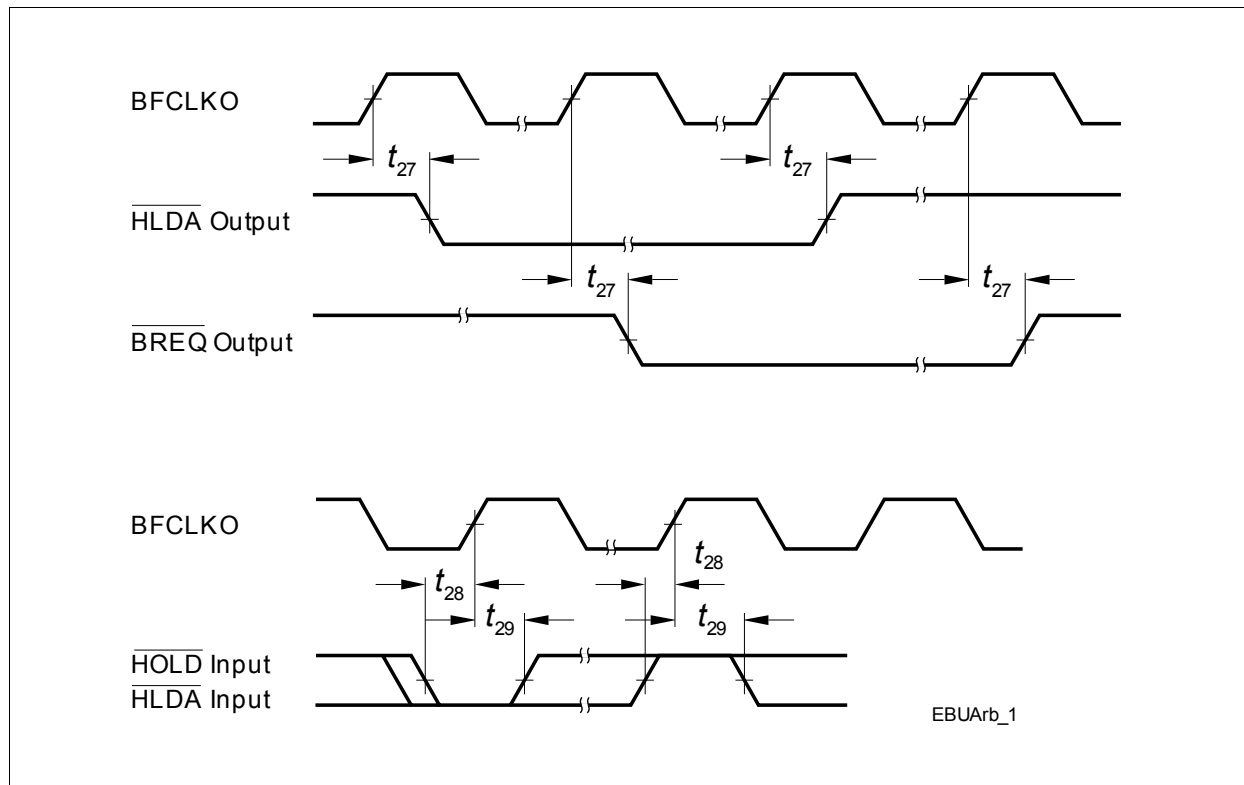


Figure 41 EBU Arbitration Signal Timing

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